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Automated module placement and wire routeing according to a structured biplanar scheme in printed boards

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Heuristic procedures are proposed for solving the module placement and the wire routeing problems in printed boards with the primary objective of reducing the area covered by the conductor paths. A structured biplanar scheme has been adopted, into which the modules are placed on the nodes of an array and the conductor paths are realized by means of horizontal and vertical connections, printed on the different sides of the card and electrically connected via holes. The proposed method is well suited for implementation on a small computer.

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1. INTRODUCTION

This paper deals with the problem of the design automation of logical circuits. Specifically, the two problems considered are the placement of the modules on a printed card and the laying out of the wire among the module terminals.

A biplanar scheme has been fixed, into which the modules are placed in the nodes of a matrix, and the conductor paths are decomposed in horizontal (i.e. parallel to the rows) and vertical segments. Horizontal and vertical segments are printed on different sides of the card.

Heuristic procedures for solving the above mentioned problems are proposed, whose primary object is the reduction of the total area covered by the conductor paths and, indirectly, the total conductor path length. These procedures require very limited resources for implementation and are relatively fast, when compared to the alternative approaches discussed in the literature. The major results in the whole field of logical design automation are discussed in a survey paper[1] and in a number of specific papers dealing with the placement problem[2,3], the wire list determination[4–7] and the wire layout definition[8–10].

The reduced complexity of the approach proposed in this paper originates from:

1. The assumption of a fixed scheme for positioning and connecting the modules.
2. The decomposition of the classic placement and wiring problems into several cascaded subproblems.

Although by applying such constraints the degree of optimality of the result is generally smaller than would otherwise be possible, nevertheless in most cases the quality of the result is satisfactory and adequate in view of the limited cost of the method.

2. GENERAL DESCRIPTION OF THE WIRING LAYOUT SCHEME

It is assumed that the circuit to be realized consists of a number of interconnected multiterminal integrated modules that are to be placed on a printed card. The problem of decomposing a large network into minimally interconnected subcircuits, such that each subcircuit is realizable by a printed card, has been discussed in the literature and is not reconsidered here.

In the proposed scheme, the modules are placed on a printed card according to an array configuration, as shown in Figure 1. The modules occupy the nodes of the array (the number of the modules is assumed not to exceed the number of the nodes). For ease of discussion, assume that the terminals of each module are vertically aligned and that their number is the same for each module. The connections are realized by means of horizontal and vertical segments, printed on the first and the second faces of the card, respectively. Horizontal and vertical segments of the same conductor path are connected via holes (plated-through). The horizontal or vertical segments are localized in the strips between adjacent pairs of rows or columns. Different strips are allowed to have different widths, according to the number of segments they include.

Any conductor path between terminals of modules assigned to the same column (e.g. the one denoted by (a) in Figure 1) consists of a vertical segment connected to the proper terminals by means of horizontal connections, which are called 'terminal extensions'. The vertical segments are placed in the vertical strip on the right side of the column under consideration.

Any conductor path connecting modules assigned to different columns (e.g. the one denoted by (b) in Figure 1) consists of a horizontal segment and two or more vertical segments, each vertical segment connecting the subset of modules belonging to the same column. Each horizontal segment is realized in a horizontal strip between two appropriate adjacent rows.

Subcircuits realized in different cards communicate through the connector. In each card, the connector terminals are assumed to be aligned on the top side of the card, parallel to the rows. Any connection between a module and the connector is realized by means of a vertical segment.

It is easily seen that any arbitrary set of connections is always realizable according to the scheme in Figure 1, no matter how the modules are positioned on the card. In the proposed scheme the wire layout problem always has a solution, without any wire crossing, while the success of the classical approaches, e.g. the Lee's[8] or Akers's[9] algorithms, is not guaranteed. However, the degree of optimality of the solution to the wire layout problem is dependent upon the positioning of the modules.

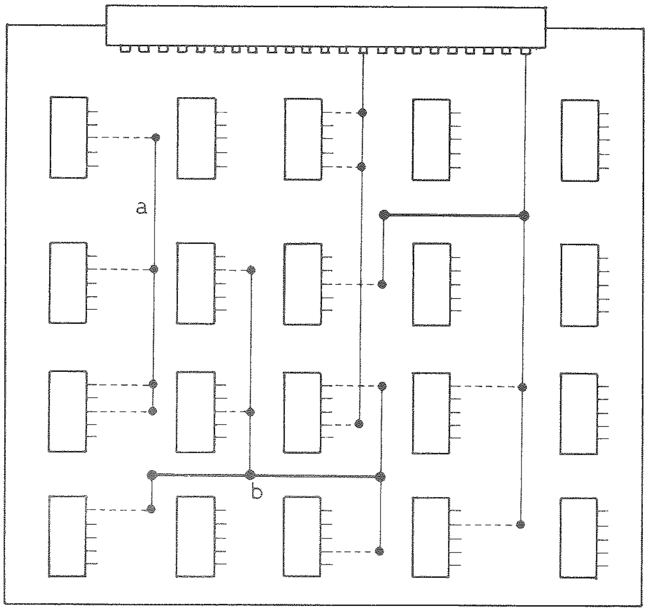

FIGURE 1. Module position and wiring layout scheme.

Therefore, the procedures being presented are divided into two successive steps, which will be described in detail in the following sections. The first step solves the module placement problem, while the second deals with the wire layout problem on the assumption that the placement of the modules is assigned.

The objective of the optimization process in both the above mentioned steps is the minimization of the area covered by the conductor paths. As an indirect result the mean wire length is also generally reduced. Because of the nature of the scheme the number of holes is not considered as an optimization object.

3. PLACEMENT OF THE MODULES ON THE CARD

The placement problem consists of assigning each module in the given set to an array node, such that the widths of the horizontal and vertical strips, and consequently the conductor path area, are minimized. In order to reduce the complexity of the optimization process, the problem has been divided into three subproblems;

1. Partitioning of the given set of modules in subsets to be assigned to columns.
2. Ordering of the modules assigned to each column.
3. Ordering of the columns.

The above mentioned steps will be discussed in some detail in this section.

3.1 Assignment of the modules to the columns

The modules in the given set are partitioned into minimally, or almost minimally, interconnected subsets. The modules in each subset will be assigned to a column of the array. The number of the subsets and their maximum cardinality are given, and coincide with the number of columns and rows, respectively, in the array. By such partitioning, the number of horizontal segments in the horizontal strips is reduced and the conductor paths are concentrated in the vertical strips. This choice is justified by the following arguments:

1. The efficiency of the procedure in reducing the area occupied by the segments belonging to a given strip increases as their number increases.
2. In each vertical strip there are vertical segments connecting modules to the connector. Two of these vertical segments cannot be printed in the same vertical line. Therefore, there exists a lower boundary for the width of the strip and the addition of vertical segments may not cause the width to increase.
3. The length of conductor paths connecting modules is likely to be smaller if the modules are assigned to the same column.
4. If the number of the horizontal segments is small, the incompatibilities arising in the area where horizontal and vertical strips cross are more easily resolved (see Section 4).

Since procedures for partitioning a set of modules in minimally interconnected subsets known from the literature[11] are quite complex, the assignment of the modules to the columns has been carried out by means of a simple algorithm, yielding a partition which is optimal with respect to the change of position of any two modules. This level of optimality is well suited to our aims, as explained later. The heuristic procedure assigning the modules to the columns, first determines a partition in the set of the given modules, whose blocks are ordered and in which the elements belonging to the same block are ordered. This partition defines an initial configuration of the modules on the card, each block corresponding to a column, and the elements of each block to the positions in the column. In order to define the partition, the columns are filled sequentially through successive steps, each step adding a module to the current column. The module to be added is selected according to a criterion of 'maximum conjunction, minimal disjunction', used in most similar problems[12]. The procedures may be formalized in the following way.

Define the following:

- M — the set of the modules $M_1, M_2, \ldots, M_m$ to be placed on the card, and M' a subset of M;
- M_0 — the connector;
- M^* — the set $M \cup M_0$;
- C — the ordered set of the columns $C_1, C_2, \ldots, C_c$ in the card;
- S_i — (*signal*) the set of the terminals $t_1, t_2, \ldots, t_{hi}$ connected by the same conductor path;
- S — the set $\{S_1, S_2, \ldots, S_s\}$ of the signals;
- W — (*connection*) a pair of terminals in a signal, $w_i = \{t_j, t_k\} \subseteq S_h$.

Moreover, if $X = \{X_1, X_2, \ldots, X_n\}$, $\bar{X}_i$ denotes the set of the elements in X, except for the element X_i, and $|X|$ denotes the cardinality of X. Then:

- $c(M_i)$ — is the column to which the module M_i belongs;
- $c^{-1}(C_i)$ — is the set of the modules belonging to the column C_i;
- $s(M_i^*)$ — is the set of signals connecting terminals of M_i^*;
- $s'(M')$ — is the set of the signals connecting modules belonging to M'.

Suppose the assignment of modules to columns C_i $(1 \leqslant i < j)$ has been completed and we are filling column

C_j. Thus

$$M'' = \overline{\bigcup_{i=1\ldots j} c^{-1}(C_i)}$$

is the set of modules not yet placed in any column.

If M_i'' denotes a module in M'':

$$V_1(M_i'', C_j) = |s(M_i'') \cap s'(c^{-1}(C_j))|$$

is the number of the signals connecting M_i'' and the set of the modules already placed in column C_j;

$$V_2(M_i'', M'') = \sum_{M_b'' \in (M'' \cap \overline{M_i''})} |s(M_i'') \cap s(M_b'')|$$

is the number of the connections among M_i'' and the other modules in M'';

$$a = s(M_0)/c$$

is the average of the number of the vertical segments connecting the modules of a column to the connector.

The next module to be assigned to column C_j is selected in M'' according to the "figure of merit" V_3:

$$V_3(M_i'', C_j) = \frac{1 + V_1(M_i'', C_j)}{1 + V_2(M_i'', M'') + a \,.\, b(M_i'', C_j)}$$

where $b(M_i'', C_j) = 1$ if $a < |s'(c^{-1}(C_j) \cup M_i'') \cap s(M_0)|$,
$= 0$ otherwise.

This figure of merit is evaluated for each module in M'', and a module for which V_3 is maximum is selected.

Note that V_3 is an increasing function of V_1 and a decreasing function of V_2. Since two or more modules in M'' connected with M_i'' by the same signal may be assigned to different columns, V_1 represents the increase in the number of connections between columns if M_i'' is not assigned to C_j, while V_2 represents the maximum increase in the number of connections between columns if M_i'' is assigned to C_j. The quantity $a \,.\, b(M_i'', C_j)$ makes V_3 decrease if the number of signals connecting modules of C_j and M_i'' to the connector is greater than the average a. As a consequence, the connections to the connector are distributed with a certain degree of regularity among the vertical strips, and the reduction of the vertical strip width becomes more efficient. The addition of 1 to the denominator prevents the division by zero; while the same addition to the numerator draws a distinction between modules for which $V_1 = 0$.

The process of assigning modules to column C_j stops when $|c^{-1}(C_j)|$ equals the number of rows; then column C_{j+1} is filled by using the same procedure. The assignment algorithm terminates when M'' is void.

In order to improve the initial partition yielded by this procedure, a "simple replacement" algorithm[14] has also been defined, in which the connections between columns are further reduced. The partition determined by such an algorithm is an optimal configuration with respect to the change of position of any two modules belonging to different columns. The consideration of some simple properties of the circuit scheme allows the simple replacement algorithm to be implemented without actually attempting all possible replacement of modules. In fact, with the previous notations.

$$V_4(M_i) = |s(M_i) \cap s'(\overline{c^{-1}(c(M_i))})|$$

is the number of signals connecting the module M_i to modules belonging to other columns, and

$$V_5(M_i) = |s(M_i) \cap s'(\overline{M_i} \cap c^{-1}(c(M_i)))|$$

is the number of signals connecting the module M_i to modules in the same column.

The number N of the connections between columns is defined as:

$$N = \sum_{M_i \in M} V_4(M_i) - \Big| \bigcup_{M_i \in M} [s(M_i) \cap s'(\overline{c^{-1}(c(M_i))})] \Big|.$$

As a first step in the algorithm, the number N evaluated for the initial partition of the set M is denoted by N_0; then:

1. The number

   $$V_6(M_i) = V_4(M_i) - V_5(M_i)$$

   is computed for each module $M_i \in M$, and the subset $M^0 \subset M$ is defined, such that the inequality $V_6(M_i) > 0$ holds for each $M_i \in M^0$. Then:
2. If $M^0 = \phi$, the procedure stops. In fact from definitions of V_4 and V_5, it immediately follows that, if $V_6(M_{i1}) \leqslant 0$ and $V_6(M_{i2}) \leqslant 0$, N cannot be made to decrease by replacing M_{i1} with M_{i2} and vice versa. If M^0 is non-void. a module $M_i^m \in M^0$, for which $V_6(M_i^m)$ is a maximum, is selected. All simple replacements of M_i^m with modules belonging to other columns are attempted and, for each replacement K_j, the number N is evaluated and denoted by N_j, then:
3. If $N_j - N_0 \geqslant 0$ for each replacement, the subset M^0 is redefined as $M^0 \cap \overline{M_i^m}$, and the procedure is iterated from step 2. Otherwise the replacement K_{j*} yielding a minimum for $N_j - N_0$ is executed. N_0 is redefined as $N_0 = N_{j*}$ and the procedure is iterated from step 1, where the new column partition of the set M is considered in evaluating V_4 and V_5.

3.2 Module ordering

Once the modules have been assigned to columns, they are ordered such that the widths of the vertical strips are minimized. As an example, an optimal arrangement of the modules shown in Figure 2a is illustrated in Figure 2b. Although this problem is very complex, a near optimal solution is quickly determined by the following heuristic procedure. Let us denote by:

- Mt_i — the set of the terminals $t_1, t_2, \ldots, t_l$ of the module M_i, ordered from top to bottom;
- sg_i — (*vertical segment*) the set of the terminals connected by the same conductor path and belonging to modules assigned to the same column and, possibly, a terminal belonging to the connector;
- sg_i^* — a vertical segment including a connector terminal;
- Sg_j — the set of the vertical segments sg_i in column C_j;
- Sg_j^* — the subset of Sg_j including all the vertical segments sg_i^* in column C_j.

Suppose the modules belonging to columns C_i, $1 \leqslant i < j$, have been re-ordered and the modules of C_j are to be re-ordered, then:

- $sm(M_i)$ — is the set of the vertical segments connecting M_i;
- $sm'(M') = \bigcup_{M_i \in M'} sm(M_i)$ — is the set of the vertical segments connecting the modules in M';

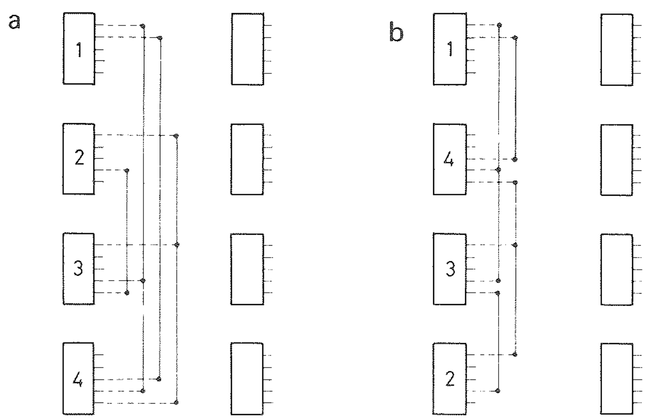

FIGURE 2. (a) Shows an arrangement of modules in a column and (b) an optimal arrangement of the same modules.

$r(C_j)$ is the set of modules of column C_j not yet re-ordered at a given step, and M_b an element of $r(C_j)$;

$r'(C_j)$ is the set of modules of column C_j already re-ordered at a given step.

At a first step $r'(C_j)$ is the empty set, $r(C_j)$ includes all the modules belonging to C_j and a module M_b is to be selected and assigned to the first position in C_j (on the top side of the card). At a given step the modules of $r'(C_j)$ have been already reassigned to the first $|r'(C_j)|$ positions in C_j and a module M_b is to be selected and assigned to the next position in C_j.

In each vertical strip the vertical segments are to be printed along discrete vertical lines. The objective is to reduce the number N_v of such vertical lines. By the previous notations it follows that:

$$S_P(M_b, C_j) = \overline{sm'(r'(C_j))} \cap sm(M_b) \cap sm'(r(C_j) \cap \bar{M}_b)$$

is the set of vertical segments exclusively connecting M_b and modules not yet re-ordered (*starting segments*);

$$S_A(M_b, C_j) = sm'(r'(C_j)) \cap sm(M_b) \cap \overline{sm'(r(C_j) \cap \bar{M}_b)}$$

is the set of vertical segments exclusively connecting M_b and modules already re-assigned (*stopping segments*);

$$S_{PP}(M_b, C_j) = sm'(r'(C_j)) \cap sm(M_b) \cap sm'(r(C_j) \cap \bar{M}_b)$$

is the set of vertical segments connecting M_b and both modules already re-assigned, and modules not yet re-assigned (*crossing segments*);

$$S_I(M_b, C_j) = sm(M_b) \cap \bar{S}_A \cap \bar{S}_P \cap \overline{S_{PP}}$$

is the set of vertical segments connecting terminals of M_b only (*internal segments*);

$$A = \bigcup_{sg_i \in S_A \cup S_I} \max \{sg_i \cap Mt_b\}$$

is the ordered set of terminals of module M_b in which *vertical segments* (either stopping segments or internal segments) *end.* Note that, if a segment ends in a terminal $t_j \in Mt_b$, it is possible to print in the same line a new vertical segment beginning from the next module or from a terminal $t_k \in Mt_b$ following t_j;

$$P = \bigcup_{sg_i \in S_p \cup S_i} \min \{sg_i \cap Mt_b\}$$

is the ordered set of terminals of module M_b in which *vertical segments* (either starting segments or internal segments) *begin.*

Let us denote by:

L the number of vertical lines that at a given step (before re-assigning a new module) are allowed for beginning segments (*allowable lines*);

L_0 the number of lines in which beginning segments of M_b may be printed, to be selected from the allowable lines or the lines corresponding to ending segments.

The new module to be re-assigned is selected in the set $r(C_j)$ according to a figure of merit $V_7(M_b, C_j)$, defined as follows:

$$V_7(M_b, C_j) = V_8(M_b, C_j) + V_9(M_b, C_j)$$

where

$$V_8(M_b, C_j) = |sm'(r'(C_j)) \cap sm(M_b)|$$

is the number of vertical segments connecting M_b to the previously re-assigned modules;

$$V_9(M_b, C_j) = L_0 - L_n,$$

where L_n is the number of vertical lines to be added in order to accommodate the beginning segments. After $V_7(M_b, C_j)$ is evaluated for each module in $r(C_j)$, the module for which V_7 is maximum is re-assigned.

The new value of L to be considered in the next step is given by $(L - L_0 + L_1)$, where L_1 is the number of the vertical lines in which a segment ends, and no new segment begins.

Figure 3 shows the flow-chart of an algorithm for evaluating V_9 and the new value of L for each selected M_b. The beginning vertical segments which can be placed in lines corresponding to ending vertical segments are counted. This is achieved by searching the terminal pairs (T_1, T_2) such that:

1. $T_1 \in A; T_2 \in P$
2. $T_2 = \min \{p_i : p_i > T_1\}$

A search is carried out commencing with the higher terminal belonging to A. Every terminal in A or P can be assigned to a single terminal pair.

In order to select the module that is to be assigned to the first position of C_j, an initial value must be assigned to L. To this end the vertical strip width W_0 is calculated assuming that:

1. The length of each vertical line is proportional to the number of modules in each column;
2. The length of a vertical segment is proportional to the number of terminals connected by the segment.

Therefore,

$$W_0 = \left(\sum_{sg_i \in sm'(c^{-1}(C_j))} |sg_i| - |sg_j^*| \right) \Big/ |c^{-1}(C_j)|.$$

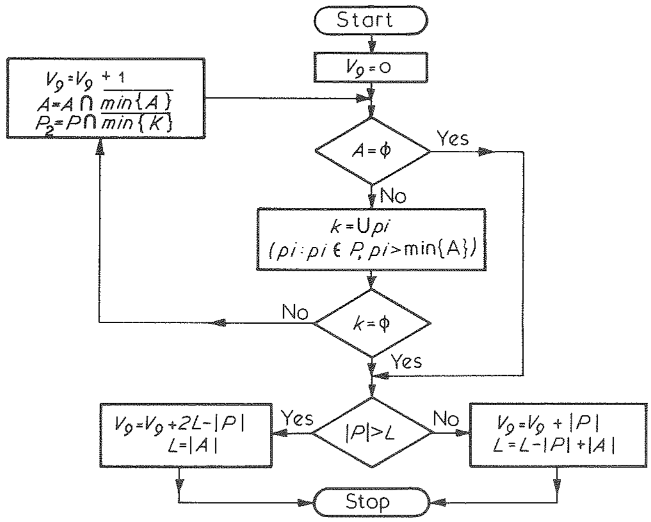

FIGURE 3. The flow-chart for the algorithm evaluating V_9 and L.

This number approximates to the minimum strip width W^m, and in most cases is smaller than W^m.

On the other hand, the minimum strip width W^m must be greater than or equal to the number of vertical segments connecting a connector terminal. Thus, we assume that the initial strip width is

$$W_1 = \max \{W_0, |Sg_j^*|\}$$

and consequently the initial value of L is given by

$$L_i = \max \{W_1 - |Sg_j^*|, 0\}.$$

After the modules in each column are ordered, the second step in the module placement procedure is completed. Note that the vertical conductors necessary to connect vertical segments to horizontal segments (*vertical extensions*) have not yet been considered. In fact, this further step must necessarily follow the assignment of horizontal segments to the horizontal strips, and its discussion is postponed to Section 4.

3.3 Column ordering

The final step in the module placement procedure deals with the column ordering. According to the original assumptions concerning the objective of the module placement procedure, the column ordering algorithm should minimize the widths of the horizontal strips. However, since the change of position of any column affects all the horizontal strip widths, in this hypothesis all the horizontal strips should be considered at the same time and the computational complexity of the algorithm would be considerable. Experience has shown that a reasonable reduction of the width of horizontal strips may be obtained by means of a simpler heuristic procedure whose objective is the minimization of the lengths of the horizontal segments. To describe this procedure the following notations are used. Let

- si_i (*horizontal segment*) be the set of all the vertical segments to be interconnected by the same conductor path;
- Si be the set of the horizontal segments;
- C^0 be the ordered set of columns already ordered at a given step.

Then

- $q(C_j)$ is the set of the horizontal segments connecting modules belonging to C_j;
- $q'(C')$ is the set of the horizontal segments connecting modules belonging to a column in a subset C' of C.

At any intermediate step, when the columns in C^0 have already been ordered, the column for which a figure of merit $V_{10}(C_j, C^0)$ is a maximum is selected for assignment; where

$$V_{10}(C_j, C^0) = q'(C^0) \cap q(C_j)$$

represents the number of interconnections between C_j and the columns already ordered. The selected column C_j^* is placed adjacent to the columns in C^0, on the left or the right side, according to whether or not $V_{11} < V_{12}$, where

$$V_{11} = |q(C_j^*) \cap q(C_1^0)| + 2\,|q(C_j^*) \cap \overline{q(C_1^0)} \cap q(C_2^0)| + \dots$$
$$\dots + |C^0| \times |q(C_j^*) \cap \overline{q(C_1^0)} \cap \overline{q(C_2^0)} \cap,$$
$$\dots \cap q(C^0_{|C^0|})|;$$

$$V_{12} = |q(C_j^*) \cap q(C^0_{|C^0|})| + 2\,|q(C_j^*) \cap \overline{q(C^0_{|C^0|})} \cap$$
$$\cap\, q(C^0_{|C^0|-1}) \dots + |C^0| \times |q(C_j^*) \cap \overline{q(C^0_{|C^0|})} \cap$$
$$\cap\, \overline{q(C^0_{|C^0|-1})} \cap \dots \cap q(C_1^0)|$$

Assuming the length of a horizontal connection to be proportional to the number of vertical strips crossed by the connection, V_{11} (V_{12}) represents the total length of the connections between C_j and the columns in C^0, if C_j is placed adjacent to the furthest left (the furthest right) element of C^0. As the initial step, the column C_k, for which $|q(C_k)|$ is maximum, is selected as the first element of C^0.

4 WIRE LAYOUT PROCEDURE

In order to specify the conductor paths, it is necessary

1. To distribute the horizontal segments among the horizontal strips;
2. To assign the horizontal segments to the horizontal lines;
3. To assign the vertical segments to the vertical lines.

The assignments aim at reducing the total number of horizontal and vertical lines.

4.1 Horizontal segment distribution

A horizontal strip is a strip between two adjacent rows. The horizontal segments are distributed so that the total length of vertical extensions is minimized by means of the following algorithm:

Let us denote by

- T the matrix of the terminals of the modules on the card, t_{ij} an element of T and t_i' a row of T;
- sv_i the set of the terminals connected by a vertical segment, ordered from top to bottom;
- St the set of the horizontal strips, ordered from top to bottom, and St_j an element of St.

Then, $p(si_k)$ is the set of the vertical segments connected by si_k, ordered from left to right.

Moreover, we define the operator DIST between an element of T and a row of T, as follows:

$$t_{ij} \text{ DIST } t'_k = i - k.$$

For every horizontal segment si_k, a horizontal strip is selected according to the following figure of merit:

$$V_{13}(si_k, St_j) = \sum_{sv_i \in p(si_k)} \max \left\{0.5 + \min \{sv_i\} \text{ DIST } t'_{l.j}, 0\right\} +$$

$$+ \sum_{sv_i \in p(si_k)} \max \left\{0.5 + t'_{l.j} \text{ DIST } \max \{sv_i\}, 0\right\}$$

where the l is the number of the terminals of each module. The horizontal segment si_k is assigned to the strip for which V_{13} is minimum. In fact, V_{13} represents the length of the vertical extensions required to connect si_k. This is true if;

1. The distance between a terminal and the next is assumed unitary.
2. The strip St_j is supposed to have zero width and to be placed in the mid-position between the last terminal of a module and the first terminal of the next module.

Note that, once the procedure for horizontal distribution is completed, the "wire list" problem[4–6] has been uniquely solved.

4.2 Horizontal segment assignment

The assignment of the horizontal segments to the horizontal lines is made complex because incompatibilities may arise in the regions where horizontal and vertical strips cross (*cross area*). These are regions where horizontal segments and vertical extensions are connected via holes. Since neither the horizontal segments nor the vertical extensions have been assigned to the horizontal and vertical lines, respectively, the exact position of the holes is still unknown. If two horizontal segments (vertical extensions) belonging to the same strip are connected to the extremes of two vertical extensions (horizontal segments) which also belong to the same strip, printing them in the same line may be impossible, i.e. an incompatibility may occur, as shown in Figure 4. The incompatibility may possibly be removed by altering the relative position of the vertical extensions (horizontal segments). In Figure 4, a star indicates an element of an incompatible pair, whenever the incompatibility can be removed.

A relatively simple way to remove such an obstacle is to ensure that the horizontal segment assignment systematically precedes both the vertical segment assignment and the vertical extensions assignment. In fact, this choice is justified by the following considerations:

1. Assume that the number of the horizontal segments and, consequently, the number of situations in which incompatibility occurs, is moderate, and that the optimization level does not appreciably decrease if the two assignment steps are cascaded;
2. Suppose that two segments belonging to the same strip must be printed in two different lines α and β as they are elements of an incompatible pair of segments. The probability that in the same strip there exist other segments that can be printed in α and β increases with the number of the segments in the strip. Since the number of horizontal segments in the horizontal strips has been reduced and the conductor paths have been concentrated in the vertical strips, it is advantageous to make horizontal segments compatible whenever necessary.

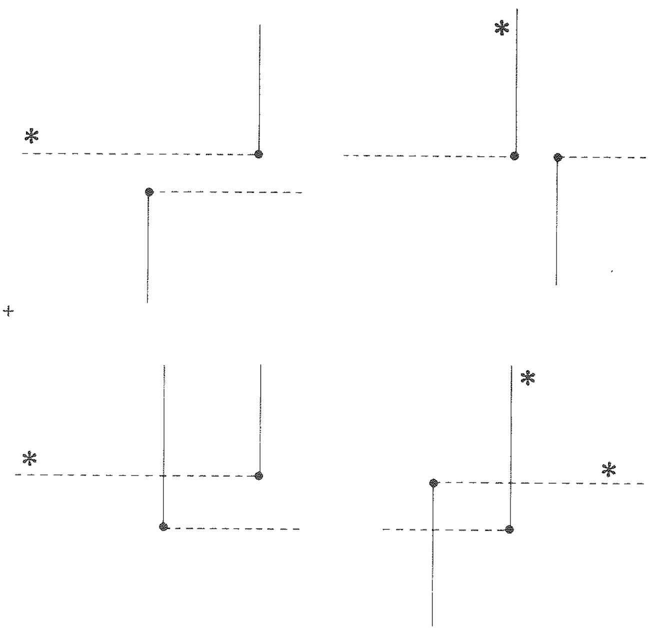

FIGURE 4. Some incompatible pairs of connections. The asterisks indicate an element of an incompatible pair of horizontal segments and/or vertical extensions.

The algorithm for the assignment of the horizontal segments is formalized in the following way.

Let us denote by

- Lz_k — the set of the horizontal lines, belonging to a horizontal strip St_k, ordered from top to bottom;
- I^{aa} — the ordered set consisting of the leading a elements of the ordered set I.

Then,

- $h(St_k)$ — is the set of the horizontal segments assigned to the horizontal strip St_k;
- $z(si_j)$ — is the horizontal line in St_k to which the horizontal segment si_j is assigned;
- $z'(Si')$ — is the set of the horizontal lines in St_k to which the horizontal segments belonging to the subset Si' are assigned.

Define the operator ASS between an ordered set of segments S^* and an ordered set of lines L^*, such that $|S^*| \leqslant |L^*|$, in the following way:

$$S^* \; ASS \; L^*$$

It assigns the elements of S^* to the leading $|S^*|$ elements of L^*, in an ordered way.

Suppose that the horizontal segments belonging to St_k are being assigned to the lines of St_k.

Firstly, the minimum number $|Lz_k|$, of horizontal lines necessary for segment assignment is evaluated. This is performed assuming that two horizontal segments connected to vertical extensions which belong to the same vertical strip can always be assigned to the same horizontal line.

$$|Lz_k| = \max\left\{ \bigcup_{j=1,2,\ldots c-1} |h(St_k) \cap \left(\bigcup_{i=1,2,\ldots j} q(C_i) \right) \cap \cap \left(\bigcup_{i=j+1,\ldots,c} q(C_i) \right)| \right\}$$

is the maximum number of horizontal segments crossing a column.

The elements of the set $h(St_k)$ are then ordered according to the increasing value of "centre of gravity", denoted by $B(si_i)$, of the extreme terminals of the vertical segments connected (through vertical extensions, where necessary) to the same horizontal segment si_i. That is,

$$B(si_i) = \frac{1}{2\,|p(si_i)|} \sum_{sg_i \in p(si_i)} (\max \{sg_i\} \text{ DIST } t_1' + \min \{sg_i\} \text{ DIST } t_1')$$

The horizontal segments in $h(St_k)$ are assigned to the lines in an ordered way, starting from the horizontal segments connected by vertical segments and/or vertical extensions to modules belonging to C_1 (that is, connected to C_1).

By the previous definitions it follows that:

$$OP(St_k, C_j) = h(St_k) \cap q(C_j) \cap \overline{q'\left(\bigcup_{i=1\ldots j-1} C_i \right)}$$

is the ordered set of the horizontal segments in St_k connected to both C_j and to columns on the right of C_j only (*starting horizontal segments*);

$$OF(St_k, C_j) = h(St_k) \cap q(C_j) \cap \overline{q'\left(\bigcup_{i=j+1\ldots c} C_i \right)}$$

is the ordered set of the horizontal segments in St_k connected to C_j and to columns on the left side of C_j only (*stopping horizontal segments*);

$$OT(St_k, C_j) = h(St_k) \cap q'\left(\bigcup_{i=1\ldots j-1} C_i \right) \cap q'\left(\bigcup_{i=j+1\ldots c} C_i \right)$$

is the ordered set of the horizontal segments in St_k connecting columns on the right and on the left side of C_j.

Suppose that the horizontal segments connected to columns on the left side of C_j have already been assigned to the horizontal lines and that the horizontal segments starting from C_j are to be assigned to the horizontal lines. If the number of the starting horizontal segments is not larger than the number of the allowable horizontal lines, that is if

$$|OP| \leqslant \overline{|z'(OF) \cup z'(OT)|}$$

then the assignment of the segments of OP is simply performed as follows:

$$OP\ ASS\ \overline{z'(OF) \cup z'(OT)};$$

Otherwise

$$OP\ ASS\ \overline{(z'(OF) \cup z'(OT) \cup z'(OF)^{ll})},$$

where

$$l = |OP| - \overline{|z'(OF) \cup z'(OT)|};$$

That is, it is assumed that l horizontal segment pairs in ST_k are made compatible. In the assignment of horizontal segments starting from every column, all the horizontal segments belonging to St_k are assigned to the lines in St_k, and are ordered, where possible, according to the "centre of gravity".

If the above described algorithm is iterated for each horizontal strip, the horizontal segment assignment algorithm is completed.

4.3 Vertical segment assignment

Vertical segments are assigned to the vertical lines for each vertical strip such that the number of vertical lines is minimized.

Assume that the number of vertical lines in the vertical strip Stv_j is to be minimized, and denote by

tv_i	(*new terminal*) a terminal of a module belonging to C_j, or a terminal of the connector, or a horizontal line connected by a vertical extension in Stv_j;
tv	the set of all the tv_i, ordered from top to bottom;
Sv_i	(*new vertical segment*) the ordered set of the tv_i interconnected by the same vertical conductor path;
Sv	the set of the Sv_i in Stv_j;
Sa	the set of the Sv_i in Stv_j not yet assigned at a given step;
Lv	the set of the vertical lines in Stv_j, ordered from left to right.

Then,

$p^{-1}(Sv_i)$ is the horizontal segment connected to Sv_i, if this exists; otherwise ϕ,

$sl(Sv_i)$ is the last element of tv connected by Sv_i.

Define the operator SEL between a set Sv and a terminal tv_k, in the following way:

$Sv\ SEL\ tv_k$ | is the Sv_i^* such that:

1. $\min \{Sv_i^*\} > tv_k$
2. There exists no element Sv_i^0 belonging to $Sv \cap \overline{Sv_i^*}$ such that $\min \{Sv_i^*\} \geqslant \min \{Sv_i^0\} > tv_k$

The vertical lines in Stv_j are filled one at a time in an ordered way, starting from the left. Suppose the line Lv_h is being filled and the maximum terminal of the last Sv_i assigned is tv_k. The next Sv_i^* to be assigned to Lv_h is selected by the SEL operator applied to the set Sa, by excluding every new vertical segment satisfying the following two conditions:

1. It is connected to a starting horizontal segment si_i^*;
2. There exists an Sv_i in Sv, not yet assigned and connected to a stopping horizontal segment assigned to the same horizontal line as Si_i^*.

An algorithm for selecting the next new vertical segment Sv_i^* is represented by the flow-chart in Figure 5.

The new vertical segment assignment in Stv_j terminates if $Sa = \phi$.

5 FINAL REMARKS

The procedures described in this paper have been implemented in APL[13] and run on an IBM 360/67 computer in order

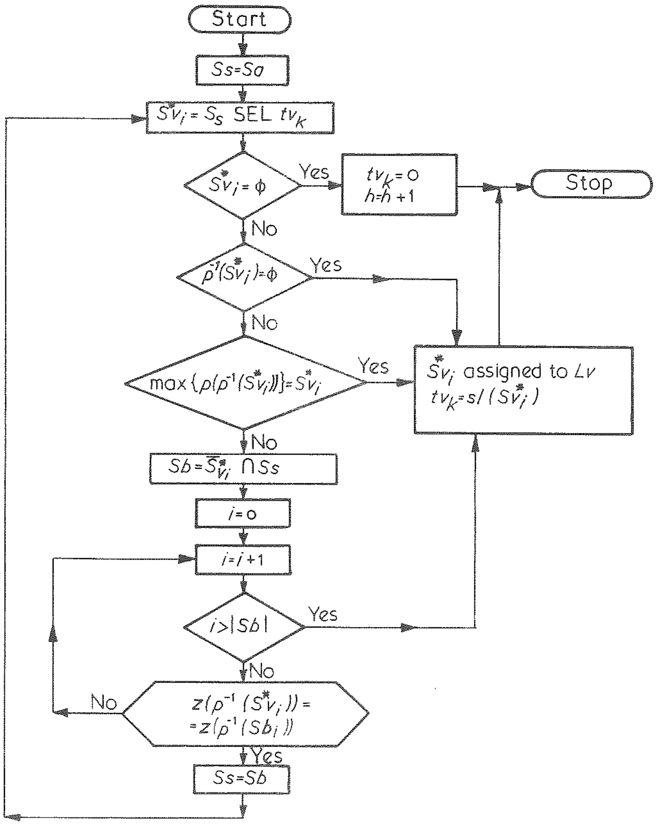

FIGURE 5. The flow-chart for the algorithm that selects Sv_i^*.

to obtain a first, rough evaluation. In the implementation, the major emphasis has been placed upon reducing the memory requirements, rather than the computation time, in order to verify the assumption that the procedures are suitable for running on a small computer, such as the Hewlett-Packard 2100 with a memory size of 32 k words. According to this choice, most figures of merit defined in the procedures have been evaluated by the use of incremental techniques, thus reducing the memory space required, with a moderate increase in the computation time.

Some printed boards have been designed, starting either from circuit diagrams from the Istituto di Elaborazione della Informazione (I.E.I.) of the Consiglio Nazionale delle Ricerche, or from pseudo-random diagrams. The execution time and the memory space requirements of a pseudo-random circuit with 42 14-terminal modules partitioned in 6 rows, are shown in Table 1.

Note that the computation times in the Table 1 refer to the APL programs. Note, in Table 1, that the simple replacement algorithm is the most time-consuming in the procedure. On the other hand, the number of horizontal segments suppressed by the algorithm is very small, and is of the order of a few percent in the example considered. This fact implies that the partition yielded by the assignment algorithm is near optimal and therefore, the simple replacement algorithm may be omitted in most cases, thus considerably reducing the total computation time.

TABLE 1. The execution time and memory requirements of a pseudo-random circuit with 42 14-terminal modules partitioned in 6 rows

Step of the whole procedure	min	sec	1/60 sec
Assignment to the columns	3	36	0
Simple replacement algorithm	30	1	21
Module ordering	3	50	44
Column ordering	1	10	35
Horizontal segment distribution	0	34	24
Horizontal segment assignment	0	39	29
Vertical segment assignment	2	46	57
Number of bytes required by programs		18 000	
Number of words required by operands		2 000	

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