A Simulation Study of Analogue and Logic Circuits with CNTFETs

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In this paper we have implemented the semi-empirical compact model for CNTFETs already proposed by us to simulate typical analogue circuits and logic blocks both in SPICE, using ABM library, and in Verilog-A. The obtained results have been the same in static simulations and comparable in dynamic simulations. However using Verilog-A the simulation run time has been much shorter and the software has been much more concise and clear than schemes using ABM blocks in SPICE.

Introduction

Prediction through modeling forms the basis of engineering design. Engineers need models which relate to their design area and are adaptable to new design concepts. They also need efficient and friendly ways of presenting, viewing and transmitting the data associated with their models.

With reference to Carbon Nanotube Field Effect Transistors (CNTFETs), which are regarded as an important contending device to replace conventional silicon transistors (1), most of their models available in literature are numerical and make use of self-consistency and therefore they do not allow an easy implementation in circuit simulators, such as SPICE, Verilog or VHDL-AMS, which instead must be the main characteristic in the field of Computer Aided Design (CAD).

As a general rule, the modelling of these new devices implies the solution of a set of partial differential equations. In this case the way to obtain correct results is to write a program written *ad hoc* for mathematical computation software (like Octave, Matlab), which allows in short time to obtain current-voltage characteristics of the simple device.

However, when we must simulate real complex circuits, we require the help of graphical interfaces to acquire circuit schemes and translated them in equations systems, which are typical tools of electronic simulations software. In particular, when the device behaviour can be expressed as a set of equations non involving PDE, using a compact model, it is possible to utilize some of the most useful tools available in electronic simulation software, having the component libraries and the graphic interface for the schematic drawing to obtain circuit netlist and circuit equations automatically. These both functions are the key point to reduce processing times, since, when circuits become complex, it is very difficult to solve and to check, one by one, a large system of integral-differential non linear coupled equations using, for example, Octave or Matlab. For this reason an electronic simulation software requires that the device should be described in an hardware description language.

In (2-8) we have already proposed a compact, semi-empirical model of CNTFET, in which we introduced some improvements to allow an easy implementation in SPICE, using ABM library.
In this paper we implement our CNTFET model to simulate typical analogue circuits and logic blocks both in SPICE and in Verilog-A in order to compare them.
The obtained results have been the same in static simulations and comparable in dynamic simulations, in which the differences are due to the better implementation in Verilog-A of the intrinsic capacitance model.
The presentation is organized as follows. At first we briefly describe our compact, semi-empirical model of CNTFET, with reference to the main equations on which the CNTFET model is based. A description of the Verilog-A and SPICE implementation is given, together with the discussion of relative results and conclusions.

Model description

I-V model

An exhaustive description of our model is in (2-3). In this Section we just describe the main equations on which is based our model.
When a positive voltage is applied between drain-source ($V_{DS} > 0$ V), the hypothesis of ballistic transport allows to assert that the current is constant along the CNT and therefore it can be calculated at the beginning of the channel, near the source, at the maximum of conduction band, where electrons from the source take up energy levels related to states with positive wave number, while the electrons from the drain take up energy levels related to states with negative wave number.
When a positive voltage is applied between gate-source ($V_{GS} > 0$ V), the conduction band at the channel beginning decreases by qV_{CNT}, where V_{CNT} is the surface potential and q is the electron charge. With the hypothesis that each sub-band decreases by the same quantity along the whole channel length, the drain current for every single sub-band can be calculated using the Landauer formula (9):

$$I_{DSp} = \frac{4qkT}{h}\left[\ln\left(1+\exp\xi_{Sp}\right)-\ln\left(1+\exp\xi_{Dp}\right)\right] \qquad [1]$$

where k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, p is the number of sub-bands, while ξ_{Sp} and ξ_{Dp} have the following expressions:

$$\xi_{Sp} = \frac{qV_{CNT} - E_{Cp}}{kT} \quad \text{and} \quad \xi_{Dp} = \frac{qV_{CNT} - E_{Cp} - qV_{DS}}{kT} \qquad [2]$$

being E_{Cp} the sub-bands conduction minima.
Therefore the total drain current can be expressed as:

$$I_{DS} = \frac{4qkT}{h}\sum_{p}\left[\ln\left(1+\exp\xi_{Sp}\right)-\ln\left(1+\exp\xi_{Dp}\right)\right] \qquad [3]$$

The surface potential, V_{CNT}, is evaluated by the following approximation:

$$V_{CNT} = \begin{cases} V_{GS} & \text{for } V_{GS} < \dfrac{E_C}{q} \\ V_{GS} - \alpha\left(V_{GS} - \dfrac{E_C}{q} \right) & \text{for } V_{GS} \geq \dfrac{E_C}{q} \end{cases} \quad [4]$$

where E_C is the conduction band minimum for the first sub-band.
The parameter α depends on the V_{DS} voltage and has the following expression:

$$\alpha = \alpha_0 + \alpha_1 V_{DS} + \alpha_2 V_{DS}^2 \quad [5]$$

where α_0, α_1 and α_2, functions of both CNTFET diameter (d) and gate oxide capacitance C_{ox}, must be extracted from the experimental device characteristics (2-3).

C-V model
An exhaustive description of our C-V model is widely described in our Ref. (2) and therefore the reader is requested to consult it. In this sub-section we just describe the main equations on which is based our C-V model.
To determine the quantum capacitances C_{GS} and C_{GD}, it is necessary to know the total channel charge Q_{CNT}, having the following expression:

$$Q_{CNT} = q\sum_p \left(n_{Sp} + n_{Dp} \right) \quad [6]$$

where n_{Sp} and n_{Dp} are electron concentrations by the source and the drain respectively in the p-th sub-band. Having:

$$N_0 = \frac{4kT}{3\pi a_0 |\gamma|} \quad [7]$$

where a_0 is the carbon-carbon (C-C) bonding distance ($\approx$ 0.142 nm) and γ the C-C bonding energy ($\approx$ 3 eV), the number of carrier n_{ip} (i = S or D), which increases almost linearly as ξ_{ip} greater or equal than zero and falls off exponentially as ξ_{ip} becomes negative, can be derived from the following relationship (10):

$$n_{ip} = N_0 \begin{cases} A_p \exp \xi_{ip} & \text{for } \xi_{ip} < 0 \\ B_p \xi_{ip} + A_p & \text{for } \xi_{ip} \geq 0 \end{cases} \qquad i = S, D \quad [8]$$

where the parameters A_p and B_p, depending on E_{Cp}, for $E_{Cp} < 0.5\,eV$, have the following empirical expressions (10):

$$\begin{cases} A_p = -5.3E_{Cp}^2 + 10E_{Cp} + 1 \\ B_p = 0.34E_{Cp} + 1 \end{cases} \quad [9]$$

Therefore the quantum capacitances C_{GD} and C_{GS} are given by:

$$\begin{cases} C_{GD} = q\sum_{p} \frac{\partial n_{Dp}}{\partial V_{GS}} = q\sum_{p} \frac{\partial n_{Dp}}{\partial \xi_{Dp}} \frac{\partial \xi_{Dp}}{\partial V_{CNT}} \frac{\partial V_{CNT}}{\partial V_{GS}} \\ C_{GS} = q\sum_{p} \frac{\partial n_{Sp}}{\partial V_{GS}} = q\sum_{p} \frac{\partial n_{Sp}}{\partial \xi_{Sp}} \frac{\partial \xi_{Sp}}{\partial V_{CNT}} \frac{\partial V_{CNT}}{\partial V_{GS}} \end{cases} \quad [10]$$

The flow-chart to evaluate the drain current and the quantum capacitances is shown in Fig. **1**.

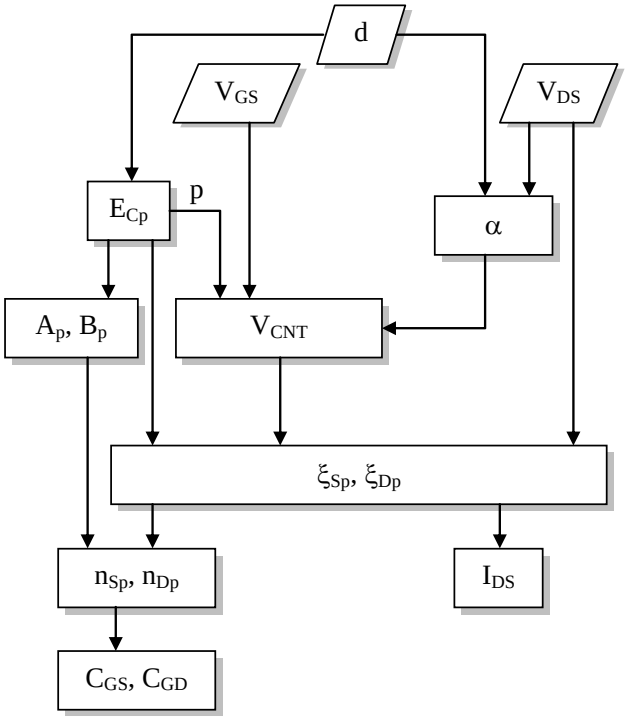

Figure 1. Flow-chart to evaluate the drain current and the quantum capacitances.

The CNTFET equivalent circuit, reported in Fig. **2**, is similar to a common MOSFET one and is characterized by the generator V_{FB}, for accounting the flat band voltage, and the resistors R_D and R_S, in which the parasitic effect due to the electrodes are also included.

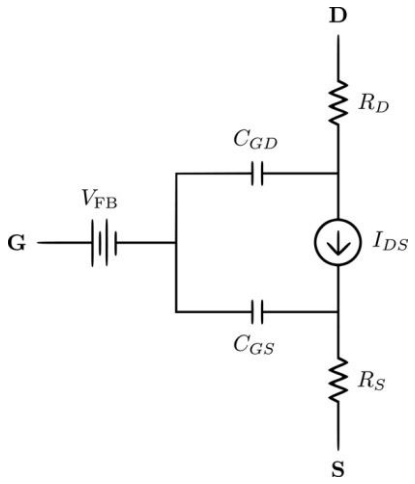

Figure 2. Equivalent circuit of a n-type CNTFET.

Model implementation both in SPICE and Verilog-A

The most common simulation tool for a designer is SPICE (Simulation Program with Integrated Circuit Emphasis), originally introduced in early 1970s by the University of California, Berkeley.

SPICE model is considered a **compact** model because of the methods used to develop the equations and coefficients used for the electrical representation of the physical behaviour of a device. The word **compact** is used because these equations are simplified based upon several assumptions that are made when developing the model equations. On the other hand the availability of accurate, robust, and efficient compact models is critical to the successful utilization of any circuit simulation tool.

We have used SPICE as implemented in ORCAD, working in graphic mode. However, since the expressions describing our device are not compatible with those of devices available in the SPICE models, the model (Fig. **2**) could not be described by an equivalent circuit including simple devices as resistances, inductances, capacitances, diodes and transistors. Therefore we have used the ABM library, one of ORCAD libraries, which implements many non linear expressions: in this way we are able to characterize our model with the correct drain current equations and the correct capacitance effects depend on bias voltages. Using ABM library, all expressions can be written as electrical circuits and therefore, during SPICE simulation, all intermediate results are expressed in voltages or currents.

Moreover, the most interesting aspect of ABM library use is to have the formula displayed in the schematics and to have some useful blocks like SOFTLIM which implements a smooth step function obtained by using hyperbolic tangent, as we have illustrated in our References (2-3), where we have reported the simulated $I_{DS} - V_{DS}$ and $I_{DS} - V_{GS}$ characteristics and the experimental ones (11), showing a good agreement between simulation and experimental results, particularly in the saturation region, where the relative error is practically negligible.

In the SPICE simulations, however, we have found several problems:

1) any voltage over 10^9 V triggers an overflow error by SPICE and therefore all model expressions must be scaled to avoid overcoming this limit in any connection;
2) the gate-drain and gate-source capacitances, depend on bias voltages, can be

obtained either as integral of current or as derivative of voltage. In the first case we introduce integration errors because of very small values of currents and time steps, while, in the second case, we introduce noise coming from derivative calculation;

3) the schematic used to simulate the CNTFET model was so large that we have decided to use the capacitances dependent only on the first band, which is the dominant component of capacitances at low voltages;
4) Debugging of formulae, expressed with schematics, has been very difficult.

The previous problems have led us to utilize Verilog-A language (12), which is a part of Verilog-AMS, a high level description language for Analogue and Mixed Signal circuits.
For model developers accustomed to working in a standard programming language such as C, the switch to Verilog-A syntax should be straightforward and painless. The language is relatively succinct and compact, and is well-suited to analog model development. Nowadays several academic and industrial model development groups use Verilog-A as a key part of their development methodology.
Verilog-A language has a syntax that recalls in many aspects that of C and, for the numerical expressions, it has a mathematical library very similar to that of C. However one of the main difference from C syntax is the "*contribution operator*" (<+), which is used to accumulate currents or voltages. Moreover, in our case, an important element of Verilog-A syntax has been the presence of "*parameter*" which could be set at run time: in this way we set nanotube diameter, length, number of electronic bands (to be accounted for current) and the kind of doping.
For example, for doping, the instruction line is:

```
parameter real doping = +1       from [-1,+1] ;   // +1 p-
type, -1 n-type
```

This last parameter was used avoiding, in this way, to duplicate code for n-type and p-type CNTFET.
In our work we use Verilog-A to describe the CNTFET in the ADS environment, while the rest of circuit was drawn with standard ADS libraries. After compiling the Verilog-A source, during the simulation, ADS calls the Verilog-A program to obtain values for the circuital equations.
This organization of the work has presented the following advantages:

1) the model source code is independent of the simulator and it can be used on any simulator which has a Verilog-A compiler and interface;
2) the values of the device voltages or currents are computed by expression which are calculated using the mathematical library with high precision and in a very short time;
3) since we have no more the model expressions split in a graph of several elemental analogue blocks as with ABM in SPICE, the number of equations to be solved at each simulation step is widely reduced with important gain in speed and precision of the simulation;
4) the mathematical computation works in standard double precision, overflow errors are those standard to double precision, and there is no need to rescale variables;
5) during the simulation it is possible to trace the behaviour of intermediate expression in the Verilog-A program as it was possible with SPICE, but in Verilog-A it is also possible to obtain code controlled messages and to dedicate more space to the debugging code;

6) the complexity of the code is tiny compared to the complexity of the schemes used to reproduce expression with ABM blocks in SPICE and this allows us to implement the complete model in all details. The code results more clear and well organized and the programming errors are widely reduced;
7) since the code is simple and fast, there is space to implement also some mathematical optimizations to enhance the numerical precision. In the model we have implemented several times expressions of the form ln[1+exp(x)] which suffers of a progressive lost of precision for x < -13, so we implemented the following code based on the Taylor approximation:

```
if (x < -13)
    begin
         ex = exp(x) ;
         f = ex*(1-ex/2) ;
    end
 else
    f = ln(1+exp(x)) ;
```

8) the gate-drain and gate-source capacitances, controlled in voltage, are implemented only in a couple of lines of code:

```
icgs = ddt(cgs*vgs) ;
icgd = ddt(cgd*vgd) ;
```

9) we obtain a speed gain up to 100 compared to our model on ABM SPICE library, since any simulation requests few seconds unlike the SPICE version, in which several minutes are necessary for simulation.

Fig. **3a** compares the $I_{DS} - V_{DS}$ characteristics (denoted by continuous lines) of numerical simulations with Verilog-A language and the experimental ones (11) (denoted by ●), in which we have assumed the same values for V_{FB}, CNT diameter, R_D and R_S reported in Ref. (11), while Fig. **3b** compares the same with SPICE.

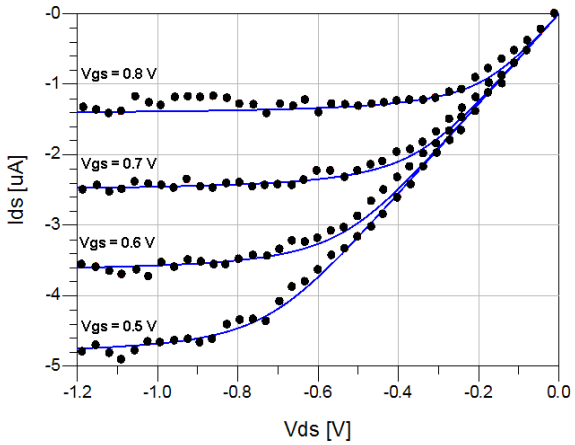

Figure 3a. Simulated $I_{DS} - V_{DS}$ characteristics (denoted by continuous lines) with Verilog-A and experimental $I_{DS} - V_{DS}$ characteristics (11) (denoted by ●).

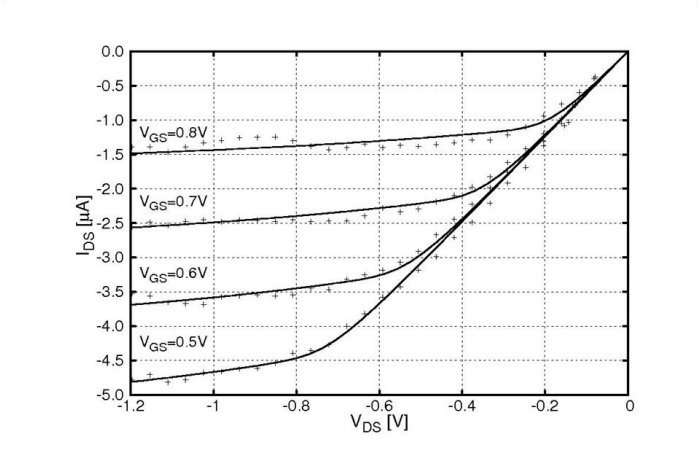

Figure 3b. Simulated $I_{DS} - V_{DS}$ characteristics (denoted by continuous lines) with SPICE and experimental $I_{DS} - V_{DS}$ characteristics (11) (denoted by +).

It is easy to see that the obtained results are practically the same in static simulations. In particular the small difference around the knees of the I-V characteristics is due to the implementation issues, because in SPICE we have implemented a simplified formula using SOFTLIM block from the ABM library, unlike Verilog-A.

However the implementation of the gate-drain and gate-source capacitances has been different in SPICE and in Verilog-A, because in SPICE only one band in the capacitance model has been considered.

Figures **4a** and **4b** show the implementation of the gate-drain and gate-source capacitances respectively using our C-V model in Verilog-A language, in which we have assumed $V_{FB} = 0$ V, CNT diameter d = 1.4 nm, $R_D = R_S = 0\ \Omega$ and $C_{ox} = 3.8$ pF/cm.

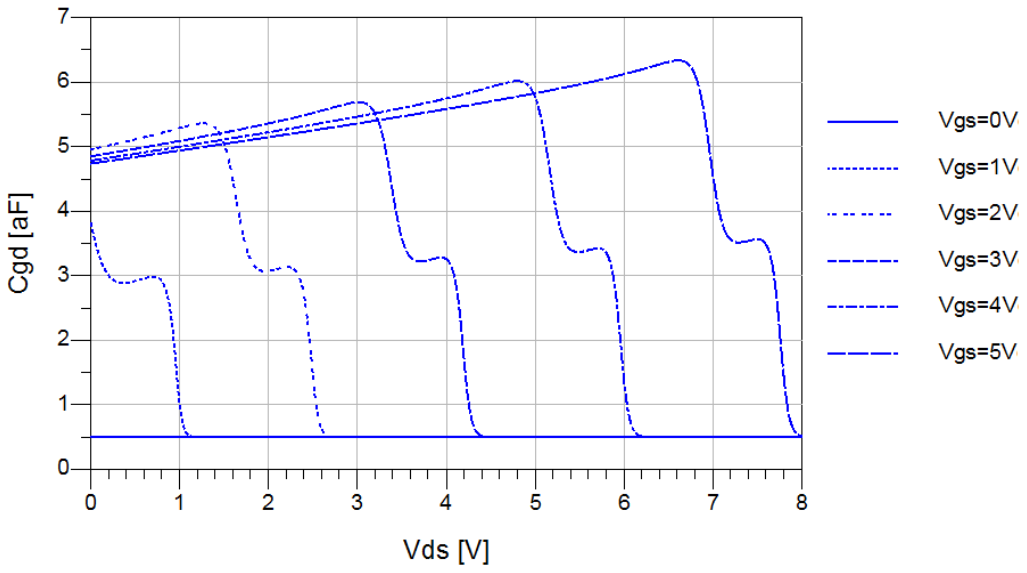

Figure 4a. Simulations of C_{GD} vs V_{DS} for different values of V_{GS} in Verilog-A.

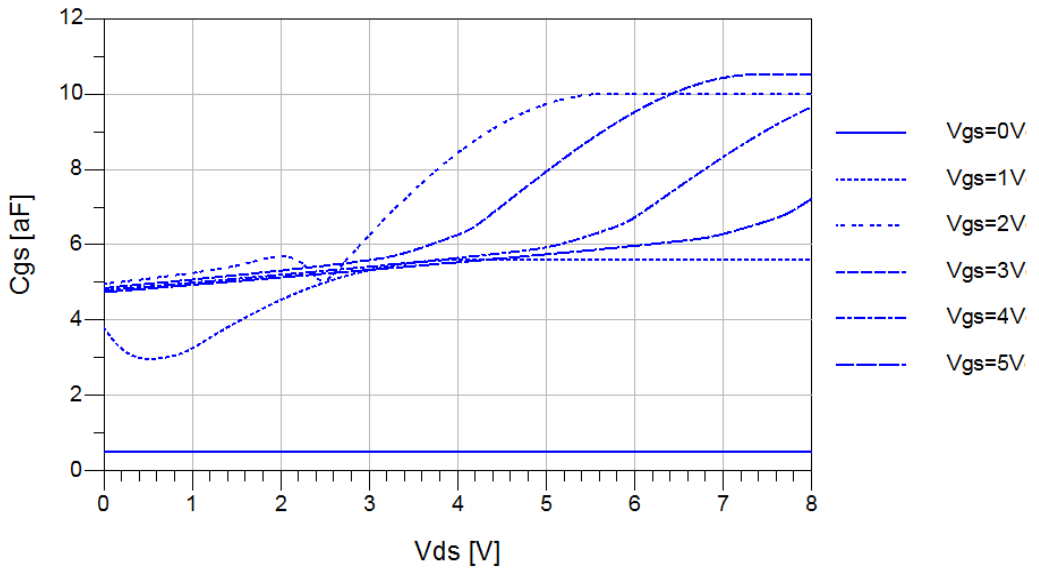

Figure 4b. Simulations of C_{GS} vs V_{DS} for different values of V_{GS} in Verilog-A.

The implementation of the same capacitances in SPICE has been reported in (2-3), where we have obtained different values of gate-drain and gate-source capacitances, because in SPICE only one band in the capacitance model has been considered.
In particular, the difference between the capacitance models comes from some simplifications we have adopted in our SPICE model (2-3), in order to do not weigh down the software further, unlike Verilog-A implementation.
However these differences have no influence on I-V characteristics, which are practically the same, as illustrated previously.

Discussion of circuit simulation examples

In all following simulations we have considered CNTFETs having a diameter of 1.42 nm, length of 100 nm and quantum capacitances depending on polarization voltages.

An example of analogue circuit simulation

In Fig. **5** we show a phase-shift oscillator, which includes three identical RC networks.

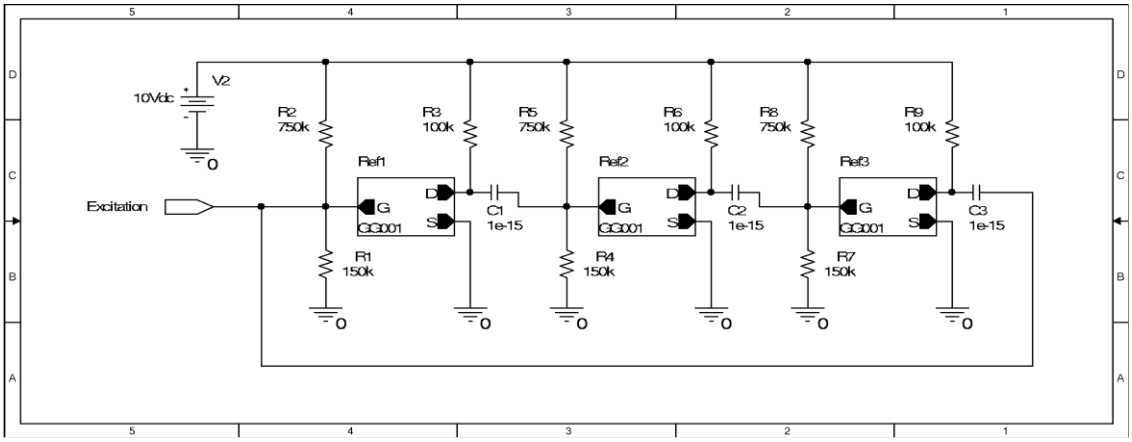

Figure 5. Phase-shift oscillator employed three CNTFETs.

In Fig. **6** we have reported the output voltage of Verilog-A simulation, while in Fig. **7** the same obtained with SPICE.

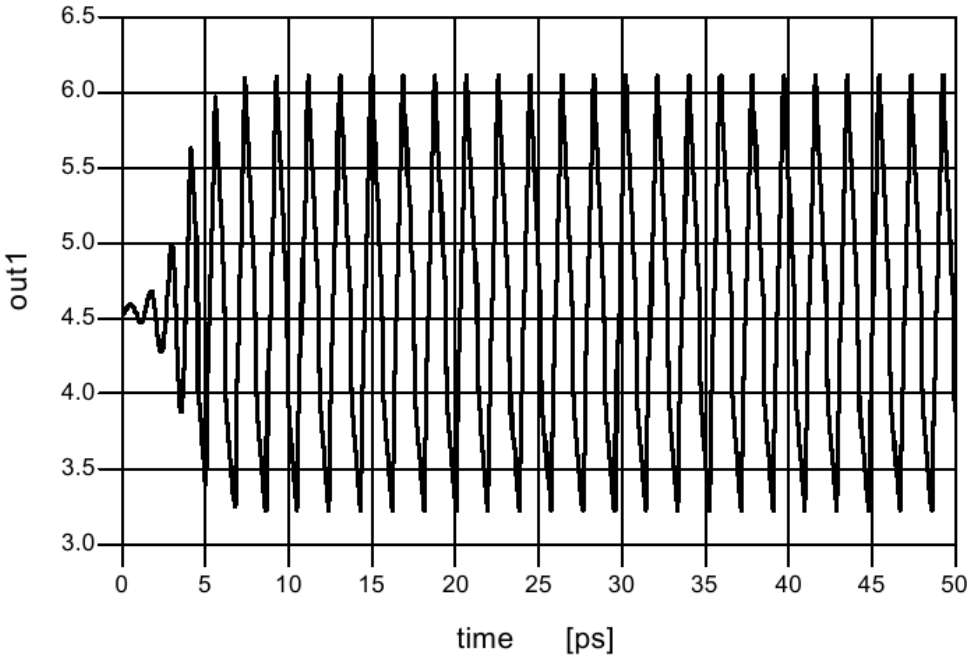

Figure 6. Output voltage of Verilog-A simulation for the phase-shift oscillator.

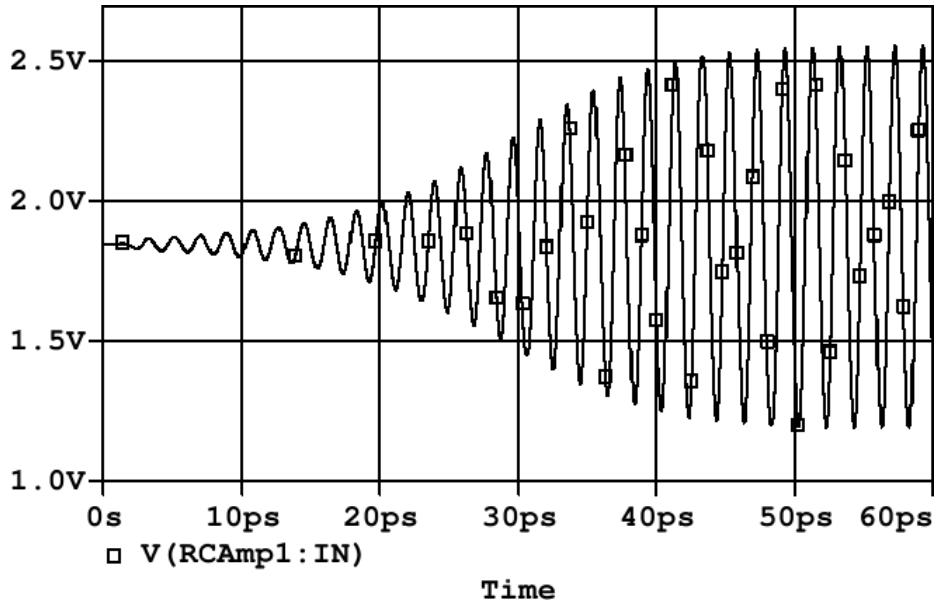

Figure 7. Output voltage of SPICE simulation for the phase-shift oscillator.

This simulation shows a small differences for the oscillation frequency (0.5 THz for SPICE (2-3), 0.53 THz for Verilog-A) and a larger difference in amplitude (1.3 V for SPICE, 2.9 V for Verilog-A). We think that these differences are mainly due to the fact that in the SPICE implementation it has been considered only one sub-band for the capacitance model in order to do not weigh down the software further, while in our Verilog-A implementation the number of sub-bands p can be defined as a parameter

settable by the user. In particular we have set p equal to 3. Moreover in Verilog-A it has been necessary to reduce the supply voltage, and therefore to modify the circuit, in order to reduce the parasitic gate source capacitances, while, since under SPICE the oscillator was pushed to the highest frequency, the circuit became very sensible to the model parameter variations.

An example of digital circuit simulation

As example of digital circuit, we have studied NAND gates in a five stage chain, as shown in Fig. **8**.

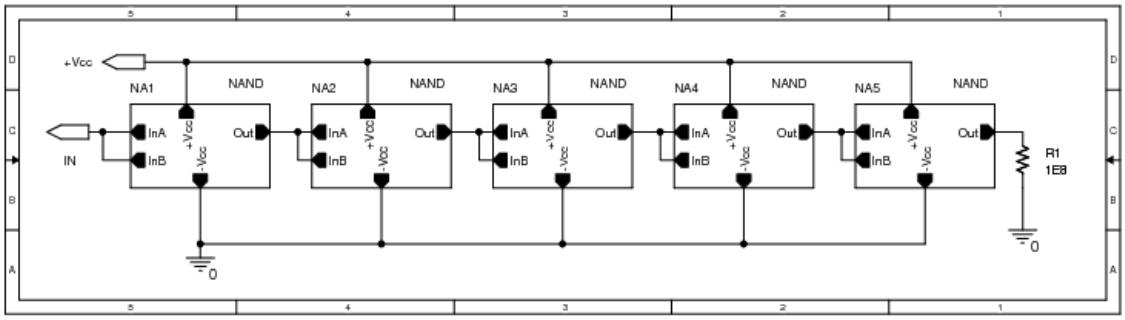

Figure 8. Schematic of the circuit used to simulate the behaviour of the NAND gate.

The result of the transient simulation in Verilog-A is shown in Fig. **9**, while Fig. **10** shows the same in SPICE.

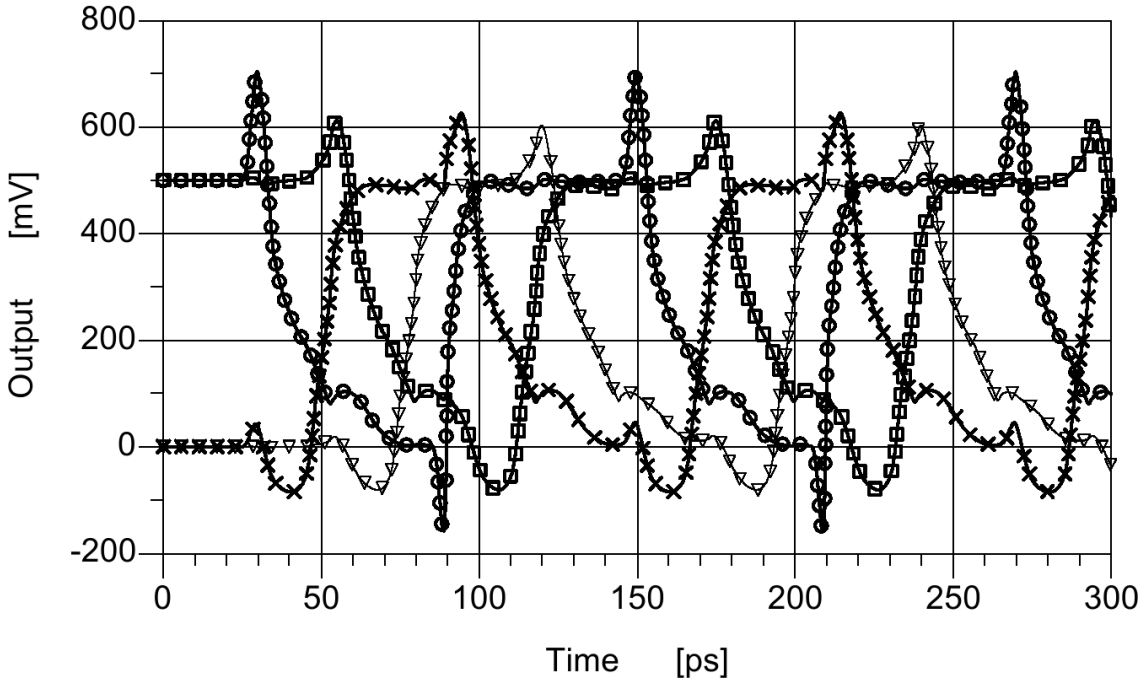

Figure 9. Transfer function of the circuit shown in Fig. **8** with Verilog-A, measured at the gate of first, second, third and fourth NAND, marked with circles, crosses, squares and triangles respectively.

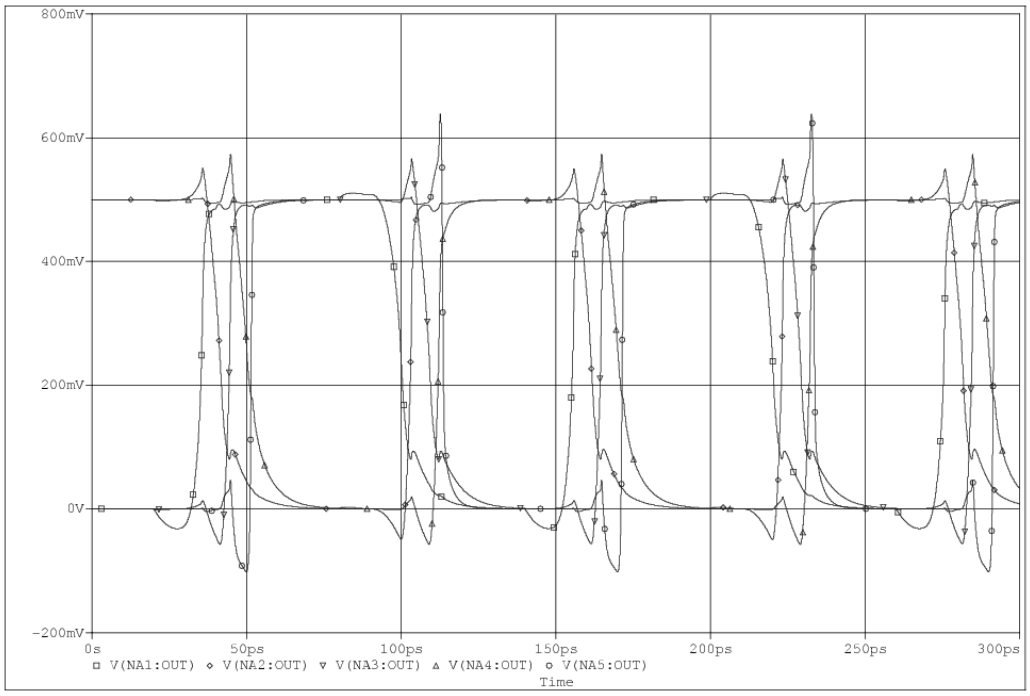

Figure 10. Transfer function of the circuit shown in Fig. **8** with SPICE.

The difference between the two implementations comes from the incomplete implementation of intrinsic capacitance model in SPICE and this also explains the different voltage levels in the widths and eights of the bumps present before the transitions start. In fact, the number of sub-bands p, also in this case, in our SPICE code has been considered equal to 1 to do not weigh down the software further, while in our Verilog-A implementation, as we have already explained, p can be defined as a parameter settable by the user (in our Verilog-A simulations p is equal to 3). Moreover, compared to the oscillator, the NAND circuit, much less sensible to the model differences, is the same both in SPICE and in Verilog-A.

Conclusions

In this paper we have implemented the semi-empirical compact model for CNTFETs already proposed by us to simulate typical analogue circuits and logic blocks both in SPICE, using ABM library, and in Verilog-A. The obtained results have been the same in static simulations and comparable in dynamic simulations. However using Verilog-A the simulation run time has been much shorter and the software has been much more concise and clear than schemes using ABM blocks in SPICE.

Although SPICE has still an huge importance in the electronic design. since a great number of commercial devices are described by SPICE models and major chip producer distribute their simulation libraries for SPICE, we think that Verilog-A is an useful tool to help circuit designers to devise these very new nascent architectures, although its diffusion is still very limited and nowadays most of its libraries are dedicated to RF (13).

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