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Interfacial charge doping effect in C8-DNTT/PDIF-CN₂ heterojunction field-effect transistors

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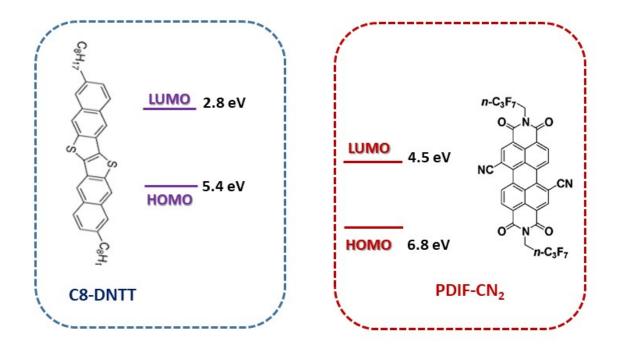


Figure S1 Molecular structures of C8-DNTT and PDIF-CN $_2$ with the corresponding HOMO and LUMO levels.

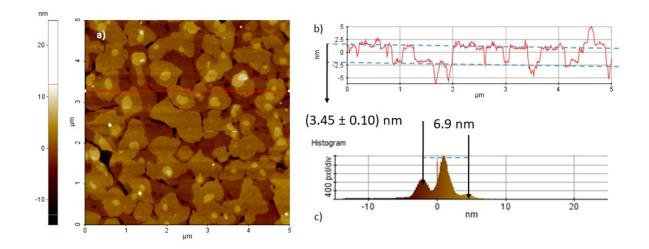


Figure S2 a) AFM image ($5x5 \ \mu m^2$) of a 15 nm thick C8-DNTT film grown on HMDS-functionalized SiO₂; b) acquired profile at line 335 (see red line in the image), an average of the terrace steps evidenced with the dashed blue lines, measured line by line is (3.45 ± 0.10) nm; c) histogram of the height distribution referred to the whole image in (a).

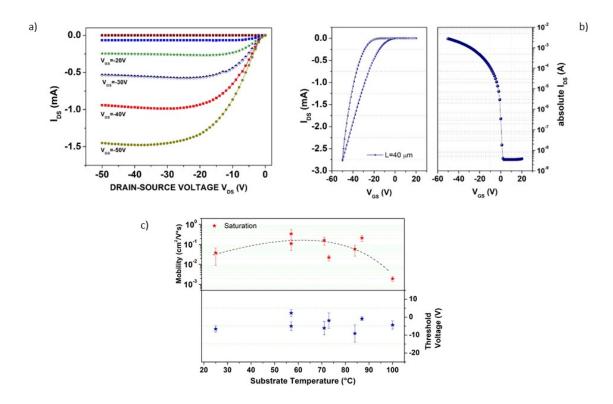


Figure S3 Electrical response of bottom-contact C8-DNTT transistors: a) output curves and b) transfer-curves measured for a device with channel length L=40 μ m; c) mobility and threshold voltage values extracted in the saturation regime (V_{DS} =-50 V) as a function of the substrate temperature (T_{sub}) held during the C8-DNTT evaporation.

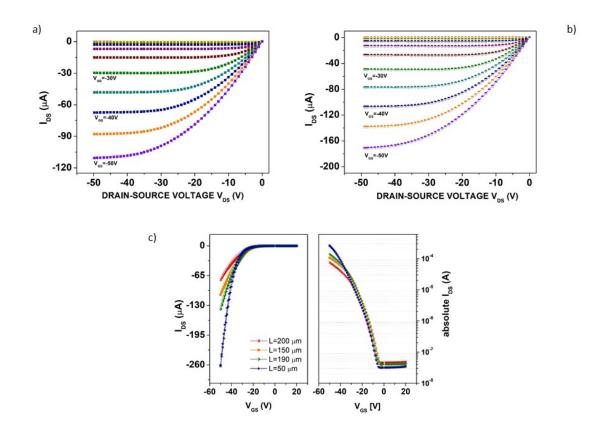


Figure S4 Electrical response of top-contact C8-DNTTsingle-layer transistors with 15 nm thick active channels deposited at T_{sub} =85 °C: output curves of devices with channel length (a) *L*=100 and (b) 150 μ m; c) transfer-curves measured in the saturation regime (V_{DS} =-50 V) for devices having different channel length.

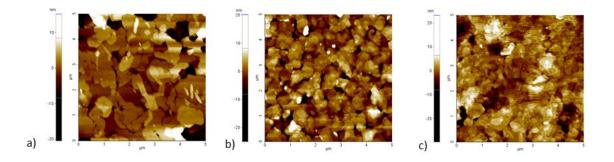


Figure S5 AFM images (5x5 μ m²): a) surface of a 15 nm thick C8-DNTT film grown on HMDS-treated SiO₂; b) and c) surfaces of a 20 nm thick PDIF-CN₂ film grown on HMDS-treated SiO₂ and C8-DNTT bottom layer, respectively. C8-DNTT and PDIF-CN₂ were sequentially deposited with the substrate temperature held at T_{sub} =85 °C and T_{sub} =100 °C, respectively.

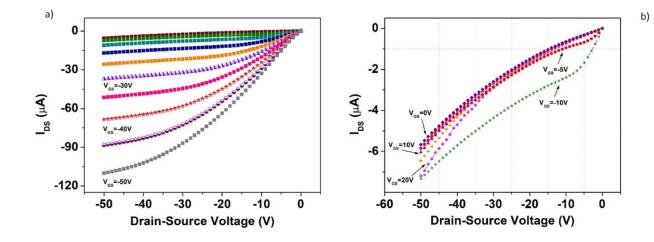


Figure S6 a) Output curves measured in the hole accumulation region for a C8-DNTT (15 nm) /PDIF-CN₂ (20 nm) heterojunction transistor with active channel deposited at T_{sub} =85 °C and channel length L=100 µm; b) zoomed view of the output curves shown in (a) and recorded for V_{GS} voltages between 20 and -10 V.

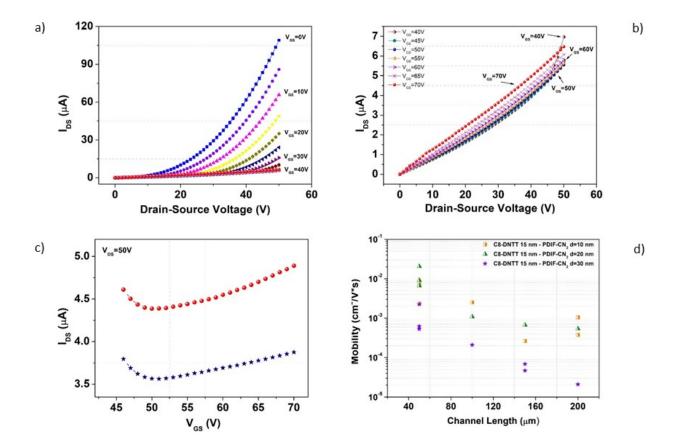
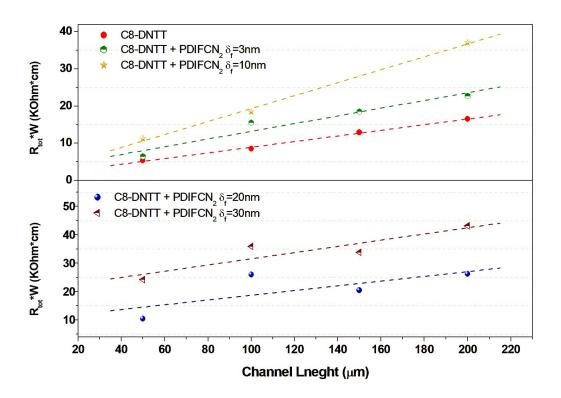
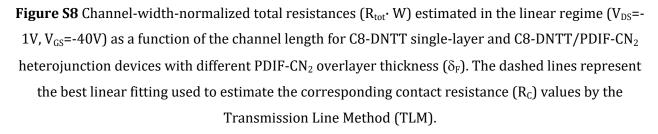


Figure S7 a) Output curves measured in the electron accumulation region for a C8-DNTT (15 nm) /PDIF-CN₂ (20 nm) heterojunction transistor with active channel deposited at T_{sub} =85 °C and channel length *L*=100 µm; b) zoomed view of the output curves recorded in (a) for V_{GS} voltages ranging between 40 and 70 V; c) typical transfer-curves recorded in the electron accumulation region (V_{DS} =50V); d) a set of mobility values extracted in the electron accumulation region as a function of the transistor channel length.





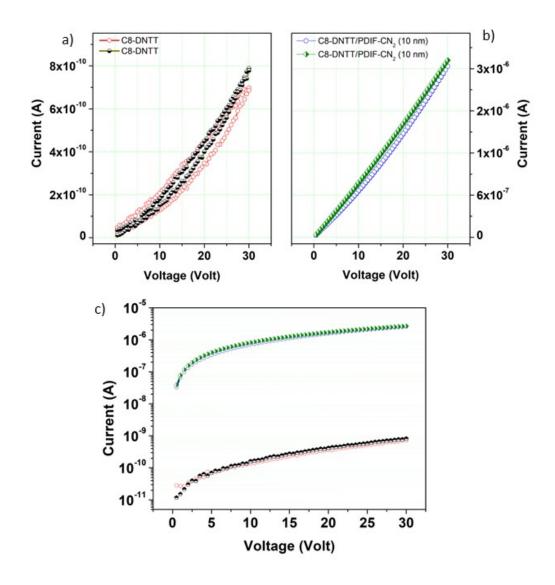


Figure S9 IV curves measured for (a) C8-DNTT (15 nm) and (b) C8-DNTT (15 nm)/PDIF-CN₂ (10 nm) films deposited at T_{sub} =85 °C on glass substrates. c) The same curves are reported in a semi-log plot. The width and length of the active channels were 500 µm and 200 µm, respectively.

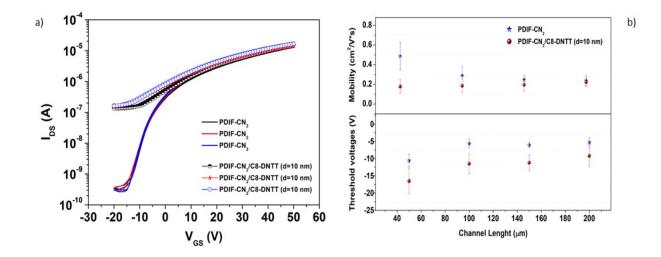


Figure S10 a) Transfer curves in semi-log plot measured in the saturation regime (V_{DS} =50 V) for PDIF-CN₂ (15 nm) single-layer and PDIF-CN₂ (15 nm)/C8-DNTT (10 nm) heterojunction transistors with active channel *L*= 200 µm; b) comparison between mobility (top) and threshold voltage (bottom) values extracted, for the electron accumulation region, in the saturation regime as a function of the channel length. Here, PDIF-CN₂ and C8-DNTT films were sequentially deposited at T_{sub} =100 °C and 85 °C, respectively.