Ripple Minimization in a Quadratic Boost Converter: Software vs. Hardware solutions

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Abstract. In this work, the authors have studied a quadratic boost DC-DC converter to reduce its ripple in the output voltage and the input current. This aim has been obtained by implementing two different solutions: the hardware solution consists on the use of coupled inductors and a notch output filter, the software solution is based on a random PWM and uses uncoupled inductors. The two solutions show a different impact on the output voltage and in the input current ripple. The performance of proposed solutions is evaluated and compared by simulation analysis both in time and frequency domain.

Key words. Quadratic boost converter, ripple reduction, random modulation, filtering.

1. Introduction

The DC-DC switching converters are widely used as power electronic interfaces in renewable energy sources (RESs), as photovoltaic PV and fuel cells (FCs) systems. These sources represent a significant solution compared to the non-renewable energy ones because they do not pollute the air and the water, like way burning fossil fuels does. On the other hand, in general, these sources deliver low voltage, and a DC-DC converter is required for boosting this voltage to a suitable value. Besides, the input current and output voltage of the DC-DC converters are not pure DC quantities but exhibit a superimposed high-frequency ripple because of the inherent characteristic of switching operation of power devices. This ripple decreases the accuracy of the maximum power point tracking algorithm (MMPT) used in FCs and PV systems [1], reduces the FCs life-time and the output power available, increases the hydrogen consumption and can force the FCs to work in regions characterized by excessive losses and overheating [2-3]. The presence of the ripple makes DC-DC converter a source of electromagnetic interference (EMI) that can disturb nearby electric/electronic devices and deteriorate their normal operating conditions. The switching operation generates, in fact, high dv/dt and di/dt that cause both conducted and radiated EMI [4-5]. To mitigate these issues, the DC-DC converter must reduce as much as possible the ripple output voltage and the input current. Several methods to reduce the input current ripple have been widely researched [6-11]. Passive solutions, such as filters and electromagnetics shielding, have been used to suppress EMI, but these methods have drawbacks in terms of weight, volume, cost, and efficiency [12]. In general, mitigation techniques of the ripple are effective only on the input or on the output. In particular, the DC-DC converters works in high-frequency range and, then, the EMI cannot be filtered by using passive filters. Other solutions, called spread spectrum methods, are based on the idea to spread the spectrum of the converter, such that the power at specific frequencies is reduced to conform to the EMI standards without any additional filters. In recent years, the application of spread spectrum techniques in power converters has been widely studied and implemented [13-17]. In this work, the authors have studied the low input current ripple DC-DC quadratic boost converter topologies proposed in [8] and [9]. Differently, here, the aim is to reduce the ripple both on input current and output voltage and, then, to mitigate the EMI disturbances of the converters comparing different solutions. In particular, [8] proposes the converter topology with uncoupled inductors, whereas in [9], the effect of coupled inductor is analysed and optimized. In this paper, the authors have implemented two solutions: the first is based on a band stop notch filter placed in the output of the DC-DC converter with coupled inductors and the latter consists on a software solution based on a random pwm spread spectrum technique to drive the same topology of the converter without coupled inductors. In this way, a comparison between hardware-based and software-based solution is performed. Simulation models of the two solutions have been obtained using Matlab/Simulink, and their performance characteristics are compared and discussed. The planning of the paper is the following. Section 2 outlines the operation of the DC-DC converter under study with and without coupled inductors. Both a hardware and software ripple reduction technique are proposed in Section 3. In Section 4, case studies are carried out, and corresponding simulation results are presented. Finally, Section 4 deals with the comparison of the results.

2. Power Converters Topology under study

The topology of the circuits under study is shown in Figure 1 and Figure 2. They differ for the coupling inductor. In the following, only the fundamental of the operation are given; further details can be found in ref. [8] and [9].
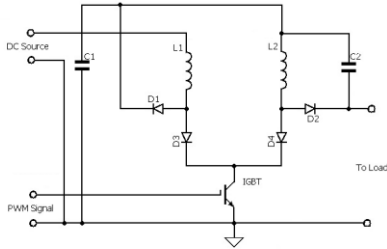

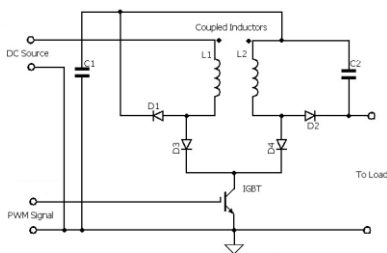Fig.1. Circuit scheme of the quadratic converter topology with uncoupled inductors.

Fig.2. Circuit scheme of the quadratic converter topology with coupled inductors.

A. Operation of the quadratic converter with uncoupled inductors.

In this analysis, all components are considered as ideal. It means that the on-state resistance $R_{DS(ON)}$ and all parasitic capacitors of the switch S are neglected, the forward voltage drop of the diodes D1-D4 are ignored, and that capacitors C1 and C2 are sufficiently large so that the voltage across C1 and C2 remains constant during one switching period.

The operation, within a switching period, T, is the following:

- Mode 1 - ON state $[t_0; t_{on}]$: in this time range, the switch S, the diodes D_4 and D_3 are turned on, whereas the diodes and D_1 and D_2 are turned off. The input voltage source is connected to the inductor L_1 and the energy of the source is transferred to this inductor. In this stage, the capacitors C_1 and C_2 supply energy to the output load, and a part of the energy, stored in C_2, supplies the inductor L_2 as well.
- Mode 2- OFF state $[t_{on}; T]$: in this time range, the switch S, the diodes D_4, and D_3 are turned off and D_1 and D_2 are turned on. The inductors L_1 and L_2 deliver their energy to the load and to the capacitors C_2 and C_1, respectively.

The average value of the two currents, $\bar{I}_{L1}$ and $\bar{I}_{L2}$, as derived in [8] are given by:

$$\bar{I}_{L1} = \frac{P_{in}}{V_{in}} \qquad \bar{I}_{L2} = \frac{V_{in}}{R(1-D)^3} \qquad (1)$$

$$V_{C1} = V_{in}\frac{D}{(1-D)^2} \qquad V_{C2} = \frac{V_{in}}{(1-D)} \qquad (2)$$

$$G = \frac{V_o}{V_{in}} = \frac{V_{C1} + V_{C2}}{V_{in}} = \frac{1}{(1-D)^2} \qquad (3)$$

where V_{in} is the input voltage, P_{in} is the maximum rated power, D is the duty cycle and R the output resistive load.

B. Operation of the Quadratic converter with coupled inductors.

In the converter topology with coupled inductors, the inductors L_1 and L_2 are coupled in opposite winding orientation, with mutual inductance, M [9]. To analyse the operating principle of this converter, the topology can be represented by an equivalent circuit with two, it can be represented by an equivalent circuit with two uncoupled inductors L_{1eq} and L_{2eq} given by [9]:

$$L_{1eq} = \frac{L_1 n(1-D)(1-k^2)}{n(1-D)+k} \qquad L_{2eq} = \frac{L_2(1-k^2)}{1-nk(1-D)} \qquad (4)$$

$$k = \frac{M}{\sqrt{L_1 L_2}} \qquad n = \sqrt{\frac{L_2}{L_1}} \qquad (5)$$

the analysis of the operating modes, within a period T, of the coupled inductors converter becomes the same of the uncoupled inductors converter with, (see figure 1), $L_1 = L_{1eq}$, $L_2 = L_{2eq}$ and M=0. For the quadratic converter topology, the inductor currents i_{L1} and i_{L2} are obtained by the superimposition of the ripple component i_1 and i_2 over the dc component, i_{L1min} and i_{L2min}, respectively, it represents the initial and final values of inductor currents in each switching interval [9]:

$$i_{L1} = i_1 + i_{L1min} \qquad i_{L2} = i_2 + i_{L2min} \qquad (6)$$

$$i_{L1}(t) = \frac{V_{in}}{L_1}\frac{n(1-D)+k}{n(1-D)(1-k^2)}t + i_{1Lmin} \qquad (7)$$

$$i_{L2}(t) = \frac{nk(1-D)+1}{(1-D)(1-k^2)}t + i_{2Lmin} \qquad (8)$$

$$i_{L1min} = \frac{P_{in}}{V_{in}} - \frac{V_{in}DT}{2L_{1eq}} \qquad (9)$$

$$i_{L2min} = \frac{V_{in}}{R(1-D)}\left[\frac{1}{(1-D)^2} - \frac{DRT}{2L_{2eq}}\right] \qquad (10)$$

Moreover, the ripple of the inductors currents, ΔI_{L1} and ΔI_{L2}, is:

$$\Delta I_{L1} = i_{L1(DT)} - i_{L1min} = \frac{V_{in}}{L_1}\frac{n(1-D)+K}{n(1-D)(1-k^2)}DT = \frac{1}{L_{1eq}}V_{in}DT \quad (11)$$

$$\Delta I_{L2} = i_{L2(DT)} - i_{L2min} = \frac{V_{in}}{L_2}\frac{1-nk(1-D)}{(1-D)(1-k^2)}DT = \frac{1}{L_{2eq}}\frac{V_{in}}{(1-D)}DT \quad (12)$$

For k=0, eq. (7) - (12) give the related values in the converter with uncoupled inductors ($L_{1eq} = L_1$ and $L_{2eq} = L_2$, M=0). In [9] it has been demonstrated that the output voltage gain equation is the same for the two topologies of the quadratic converter (eq. 3).

Equation (11) shows that the ripple on the input current depends on three design parameters: D, k, and n.

Therefore, for a given value of k and n, a value of duty ratio, D_{zero}, that ensure the free ripple input current condition, i.e., $\Delta i_{L1} = 0$, can be calculated as:

$$D_{zero} = 1 + \frac{k}{n} \qquad \text{where} \qquad 0 \leq D_{zero} \leq 1 \qquad (13)$$

the equation (11) shows that, once defined the value of $D_{desidered}$ and $n_{desidered}$ during the design step, it is possible to compute a specific value of the coupling coefficient, k^*, that assures an input free ripple condition ($D_{desired} = D_{zero}$):

$$k^* = \left| \frac{(1 - \sqrt{(1 + 8 \cdot n^2 \cdot (1-D)^2}}{2 \cdot n \cdot (1-D)} \right| \qquad (14)$$

$$\Delta_{iL1coupl} \leq \Delta_{iL1uncoupl} \qquad k \leq k* \qquad (15)$$

The input current ripple vs duty ratio for several value of k and fixed n is shown on figure 3. It can be noted that the choice of k allows the ripple to be reduced.
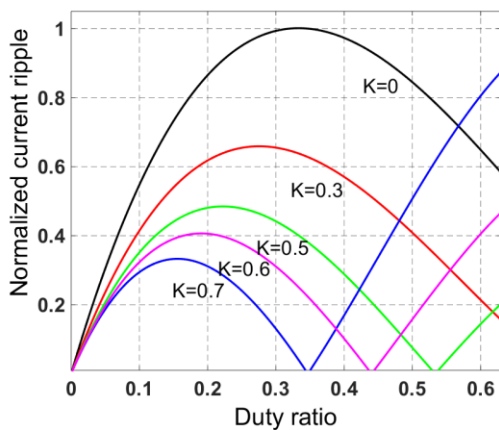

Fig.3. Input current ripple vs duty ratio for several value of k and fixed n.

3. Ripple Reduction Techniques of a Quadratic DC-DC Converter

This work aims to compare two different solutions to reduce the output voltage ripple and the input current ripple of a quadratic DC-DC converter. In particular, the authors have designed a software solution based on the random PWM technique to drive the uncoupled quadratic converter and a hardware solution based on a modification of the coupled quadratic converter controlled by a classic PWM. The performance of the two solutions is evaluated and compared.

A. Random PWM Technique

The random switching techniques are widely applied to power converter to reduce electromagnetic interferences (EMI). The random PWM (RPWM) techniques spread the power spectral density (PSD) of the conducted disturbances over a wide frequency range, reducing its amplitude respect to the classic PWM scheme. The algorithm proposed in this paper allows obtaining a PWM signal with random frequency f, where the duty cycle D is constant, and the frequency changes casually after a

number of a fixed number of pulses N (see figure 6). In figure 4 is shown the logic diagram of the proposed algorithm to generate the random PWM. A random generator gives a value of the frequency f* of a sawtooth signal randomly chosen in the range f_{min}-f_{max}. The duty cycle value of the RPWM is fixed; it defines the reference value u* gives to the comparator. This one outputs a high logical level when the amplitude of the sawtooth signal is higher than u*, otherwise, a low logical level is given (see figure 5). In this way, the comparator outputs a PWM signal with duty cycle D and a frequency f*. A pulse counter counts the number of pulses n of the RPWM signal and this number is compared whit the value N. The random generator gives a new value of the random frequency when n is equal to N. Moreover, a signal is generated to reset the pulse counter to obtain a PWM signal whit fixed duty cycle D and a frequency that changes casually after every N pulses. Figure 6 shows the RPWM generated by the proposed algorithm.
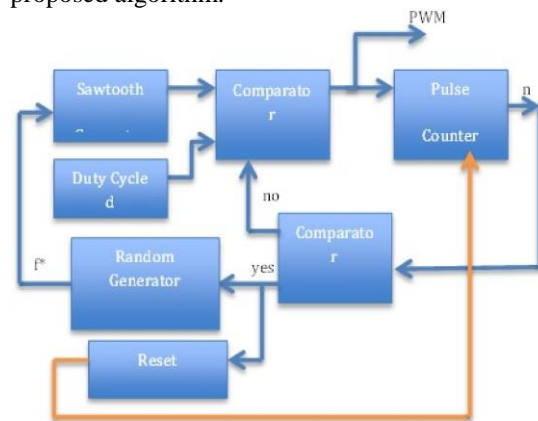

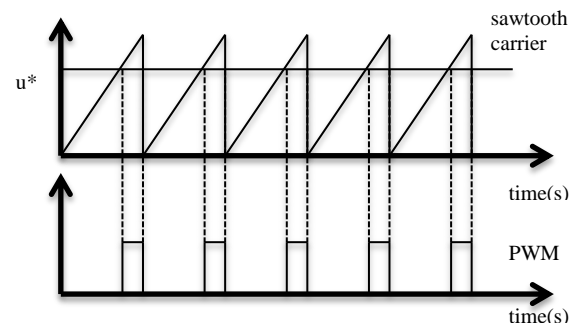Fig.4. Logic Diagram of the Random PWM algorithm.
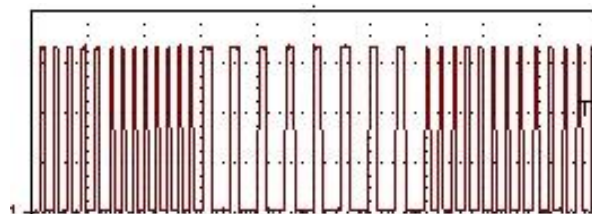

Fig.5. PWM generation method

Fig.6. Random PWM segnal proposed.

B. Hardware solution to reduce the input and output ripple.

The quadratic converter with coupled inductors, shown in figure 2 allows deleting the input ripple current when the

free ripple conditions (eq. 14 and 15) is verified [8] but it does not reduce the voltage output ripple. Following the hardware approach, a notch filter connected in parallel to the load of the converter has been designed to reduce the effect of the switching frequency in the output voltage. It is shown in figure 8. This selective filter is tuned on the first harmonic corresponding to the switching frequency since exhibits the higher amplitude.
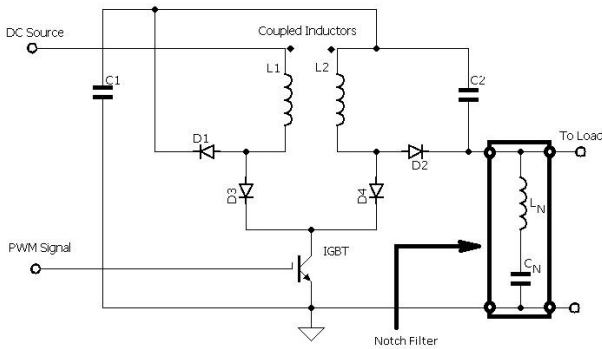

Fig.8. Circuit scheme of the quadratic converter topology with coupled inductors and notch filter.

In fact, the output voltage ripple mainly depends on the amplitude of the spectrum line at the switching frequency. The notch filter is a pass-band filter that allows a cheap realization since only a slight current at the switching frequency will flow through it, limiting the power loss. This hardware solution represents a good solution for the proposed DC-DC converter, which is characterized by low power and small size. In this application, a solution based on an active compensator is not suitable for cost and size [18]. To reduce the converter output voltage ripple, the notch filter is designed according to the following condition at the switching frequency f_s:

$$\omega_s L_n = \frac{1}{\omega_s C_n} \qquad \omega_s = \frac{1}{\sqrt{L_n C_n}} \qquad (16)$$

$$Z_{notch}(j\omega) = R_s + j\left(\omega L_n - \frac{1}{\omega C_n}\right) \qquad (17)$$

$$Z_{notch}(j\omega_s) = R_s; \; Bandwidth = B = \frac{f_s}{Q} = \frac{R_s}{2\pi L} \qquad (18)$$

where the notch impedance Z_{notch} is equal to the parasitic resistance R_s of the filter components L_n and C_n in non-ideal conditions ($R_s \neq 0$). For this reason the ac converter output voltage is not equal to zero at the switching frequency and its reduction depends on the value of the notch parasitic resistance R_s. Furthermore, the value of the filter bandwidth B depends on the value of this resistance and it is very narrow if R_s is very little. Therefore, the notch filter components L_n and C_n have to be chosen suitably in order to have a notch filter with a parasitic resistance R_s that offers a good trade-off between the filter bandwidth value and a enough reduction of the output voltage ripple. The commercial values of the components adopted for the notch filter are:

$$Ln=1.2 \text{ μH} \qquad Cn=50\text{μF} \qquad (19)$$

4. Simulation Results

The simulation models of the ripple reduction methods for the DC-DC converters studied have been created using Matlab/Simulink. Therefore, the performances of these solutions are verified and discussed. The simulations have been made considering four different scenarios: a) the converter without coupled inductors driven by classical PWM, b) the converter with coupled inductors driven by classical PWM, c) the converter with coupled inductors and notch filter driven by classical PWM, and d) the converter without coupled inductors driven by random PWM. The simulation results allow comparing the several solutions proposed by the authors in terms of input current ripple, output voltage ripple, and EMI disturbances. The electrical parameters of the DC-DC converter topologies implemented are shown in Table I.

Figures 9,10,11 and 13 show the input current and output voltage waveforms of the DC-DC converter topologies under study in the different scenarios. In particular, figure a shows the input current and the output voltage versus time and b and c the frequency spectrums of these waveforms. Figure 12 shows the pulsation of PWM signal implemented randomly variable. Table II summarizes the performance of the different scenarios in terms of input current-output voltage ripple, and the amplitude of the input current-output voltage at the switching frequency (20 KHz).

As can be seen, a very low input current ripple characterizes the two DC-DC converter topologies studied. In particular, the coupled inductors allow reducing more of the current ripple. The simulated scenarios with the DC-DC converter with coupled and uncoupled inductors driven by a classical PWM show that the output voltage ripple is comparable. The proposed solutions with coupled inductors using the notch filter driven by a classical PWM reduces the voltage ripple to a value equal about to one half. It should be remarked that the values of ΔV_{out_pp} and ΔI_{in_pp} are calculated as the difference between the maximum and the minimum value. They correspond to the ripple only in the first three cases, whereas for random modulation, it gives only the maximum variation since the variation of the switching frequency makes the ripple variable.

It is also of interest the comparison of the power calculated by the integral of the spectral power density (SPD) of the obtained waveforms. The SPD is calculated based on the Discrete Fourier Transform; the power density considers the square of the voltage and of the current The resulting power takes into account the contributions in the whole range of frequency. It has to be remarked that since the results are referred to a conventional load of 1Ω, they are meaningful in comparison. Results are summarized in table III where the percent variation, compared to the traditional PWM with uncoupled inductor topology, is calculated as well. Only the random modulation reduces the whole power on the output voltage significantly; on the contrary, the coupled inductors lessen the power associated with the input current independently of the notch filter. It requires hence a further EMI suppression at high frequencies.

(a)
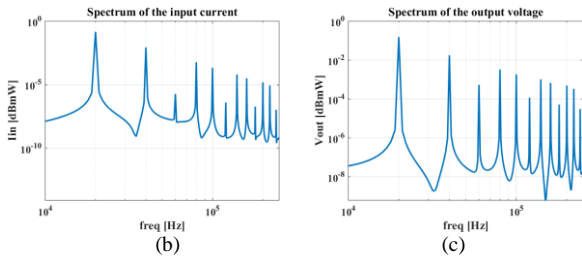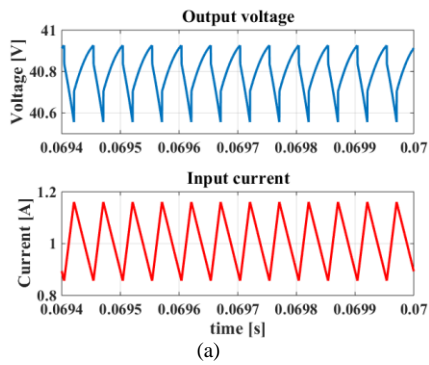

(b)   (c)

Fig.9. Input current and output voltage waveforms of the converter without coupled inductor with classical PWM.

(a)

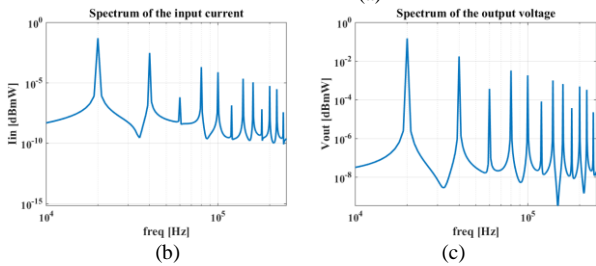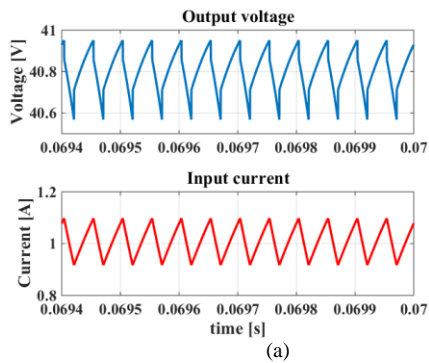(b)   (c)

Fig.10. Input current and output voltage waveforms of the Converter with coupled inductor with classical PWM.

(a)

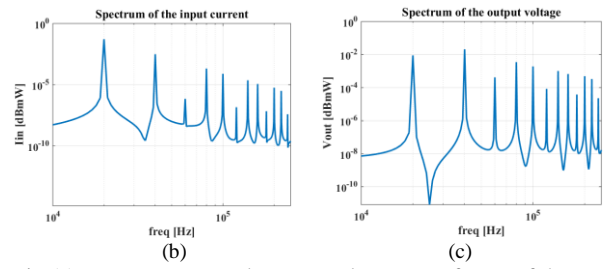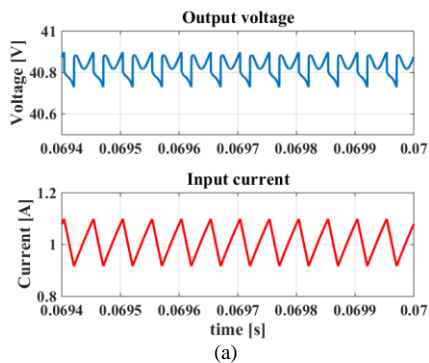(b)   (c)

Fig.11. Input current and output voltage waveforms of the Converter with coupled inductor and notch filter with classical PWM.

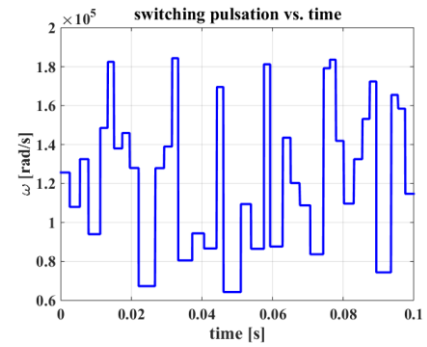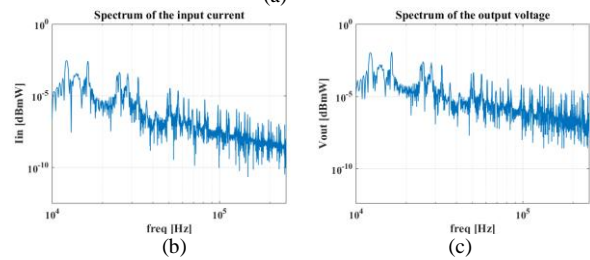Fig.12 Variation of the switching pulsation due to the Random PWM

(a)

(b)   (c)

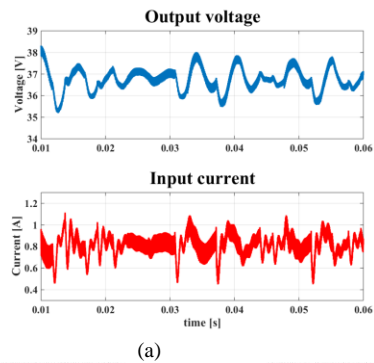Fig.13 Input current and output voltage waveforms of the Converter without coupled inductor with random PWM.

Table I. DC-DC converter parameters.

Input Voltage V_{in}	20 V
Switching frequency f_s	20 KHz
Duty Cycle	0.30
L_{1dis}	1mH
L_{1dis}	1mH
C_1	100µF
C_2	100µF
Rc_{1s}	0.05Ω
Rc_{2s}	0.05Ω
Coupling coefficient k	0.82
R_{Load}	92Ω

Table II. Comparison of the proposed solutions.

	ΔVout_pp [V]	ΔIin_pp [A]	Vout(20KHz) [dBmW]	Iin(20KHz) [dBmW]
Decoupled inductors	0.371	0.304	0.153	0.145
Coupled inductors	0.384	0.182	0.152	0.052
Notch filter	0.169	0.182	0.021	0.052
Random mod.	2.5492*	0.6408*	0.3066	0.0233

Table III: Power calculated by Spectral Power density

	Vout	ΔVout/V	Iin	ΔIin/I
Decoupled inductors	$8.3457 \cdot 10^6$	-	$2.4434 \cdot 10^4$	-
Coupled inductors	$8.3457 \cdot 10^6$	0	$1.1994 \cdot 10^4$	-51%
Notch filter	$8.3420 \cdot 10^6$	-0.044%	$1.2070 \cdot 10^4$	-51%
Random mod.	$5.7191 \cdot 10^5$	-93%	$2.0956 \cdot 10^4$	-14%

4. Conclusion

A quadratic boost converter has been analysed to highlight the reduction of the ripple in the output voltage and in the input current by different solutions based on a hardware and software approach, respectively. In particular, hardware solution employs coupled inductors and an output notch filter with a fixed frequency PWM. In contrast, the software solution exploits a random modulation algorithm to spread the spectrum lines.

The traditional quadratic converter with decoupled inductor has been compared with the same topology but considering the inductor coupled. Then a notch filter has been placed at the output to suppress the harmonic at the switching frequency and finally, a random PWM modulation has been tested.

Results show that the output voltage ripple is minimized only by the notch filter, instead the input current ripple is reduced by the presence of the coupled inductor. The random modulation exhibits a higher difference between maximum and minimum ripple both of the current and on the voltage since the ripple varies with the switching frequency but reduces drastically the power associated with the whole spectrum.

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Future developments: the results are going to be verified experimentally by a test rig on a prototype of the converter under construction.

Authors' contributions:
G. Marsala and G. Vitale conceived and designed the analysis, wrote the paper.
V. Presti conceived the random algorithm, implemented the circuits for simulation and wrote the paper.
S. G. Scordato and A. Sauro arranged the hardware for simulations, prepared a circuit prototype with the devices tested in simulation for experimental verification.