Consiglio Nazionale delle ricerche

ISTITUTO DI ELABORAZIONE DELLA INFORMAZIONE

PISA

Progetto e realizzazione di una scheda general purpose

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PROGETTO E REALIZZAZIONE DI UNA SCHEDA GENERAL PURPOSE.

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* SICEI Pisa, fino a marzo 1988 CTP presso IEI.

Introduzione

Nella realizzazione di strumentazione ad uso specifico si ha spesso la necessita' di disporre di una scheda "multipurpose" basata su di un microprocessore che possa essere rapidamente adattato alle diverse applicazioni sperimentali. Poiche' il mercato non soddisfa ancora pienamente questa necessita' si e' progettato e costruito la scheda General Purpose GP_Z80 basata sul micro Z80.

La scelta dei componenti della serie Z80 e' stata influenzata dalla facile ed economica reperibilita' sul mercato di tali componenti, dalla potenza del set di istruzioni di questo microprocessore a 8 bit e dal software disponibile per tale famiglia.

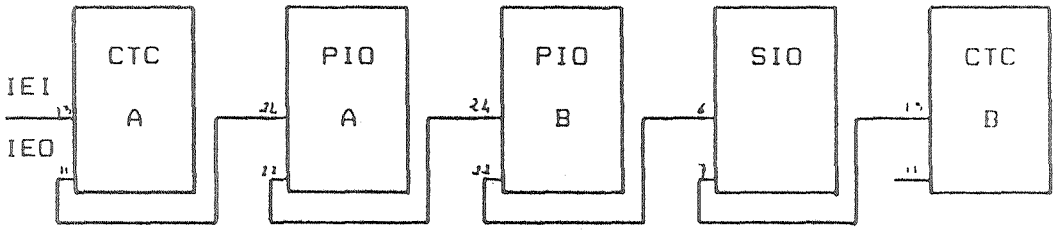
La scheda e' costituita da una quantita' variabile di memoria ROM+RAM, due porte parallele [PIO], una porta seriale [SIO] di cui un canale e' collegato con i driver per interfacciamento completo secondo lo standard EIA RS232-C, due contatori/temporizzatori [CTC], un convertitore A/D con multiplexer di ingresso a 16 canali e due convertitori D/A dotati di buffer di uscita.

La scheda utilizza come supporto una piastra "Doppia Europa " sulla quale e' stata riservata un'area per l'inserimento di zoccoli per montaggi sperimentali.

Descrizione

In fig.1 e' riportato lo schema a blocchi: si distingue la sezione riguardante il microprocessore con i circuiti di decodifica, il blocco di memoria espandibile, le porte parallele per il controllo del mondo esterno, la porta seriale per il collegamento con altri calcolatori, il blocco di temporizzazione e conteggio e quello relativo al convertitore A/D in ingresso ed ai convertitori D/A in uscita.

Nella figura sottostante sono indicati i collegamenti dei vari dispositivi della daisy chain. Se non vengono montati tutti i dispositivi e' necessario ponticellare i piedini relativi a IEI e IEO di quelli mancanti.



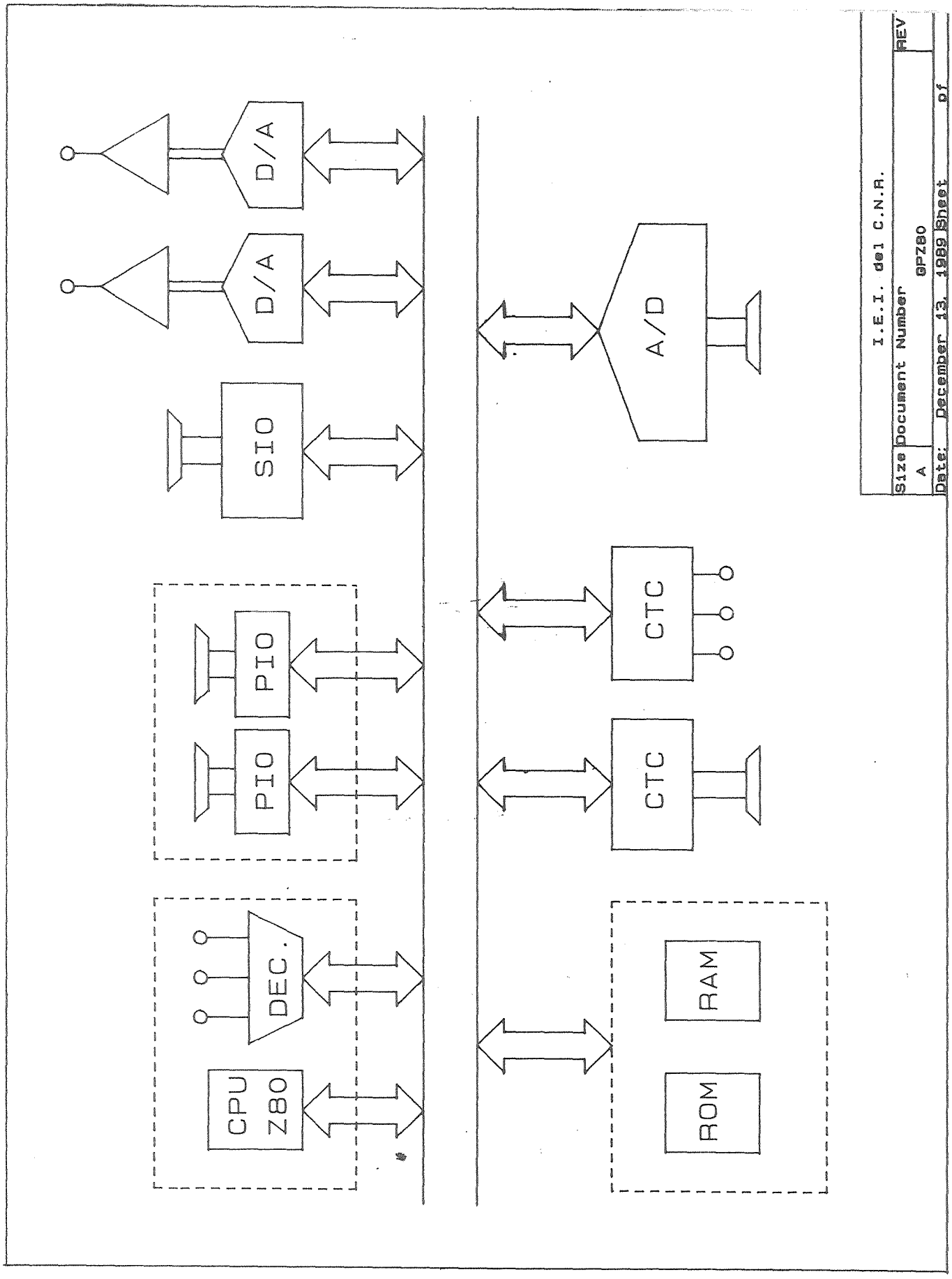


Fig.1 Schema a blocchi

In fig.2 e' riportata la circuiteria relativa alla CPU (Z80 montato sullo zoccolo U5) ed ai circuiti di decodifica, (LS138, LS139, LS02 montati rispettivamente sullo zoccolo U7, U9, U10); tramite questi ultimi a seconda dell'indirizzo fornito dalla CPU nelle operazioni di I/O si puo' rendere attivo il bit di CE (attivo basso) di ogni periferica secondo quanto mostrato nella tabella 1.

A7	A6	A5	A4	A3	A2	A1	A0	Int	zoc.n.
0	0	0	1	1	X	X	X	A/D	12
0	0	1	X	X	X	B/A	C/D	PIOA	13
0	1	0	X	X	X	B/A	C/D	PIOB	14
0	1	1	X	X	X	A1	A2	D/A	19
1	0	0	X	X	X	A1	A2	D/A	20
1	0	1	X	X	X	CS1	CS2	CTCA	16
1	1	0	X	X	X	CS1	CS2	CTCB	17
1	1	1	X	X	X	C/D	B/A	SIO	15

Tab. 1.

E' previsto un buffer del tipo 74LS244, montato sullo zoccolo U11, per la rigenerazione delle piu' significative linee di controllo. Il circuito di Reset viene attivato al momento dell'accenzione della scheda; e' previsto inoltre un pulsante di Reset S1.

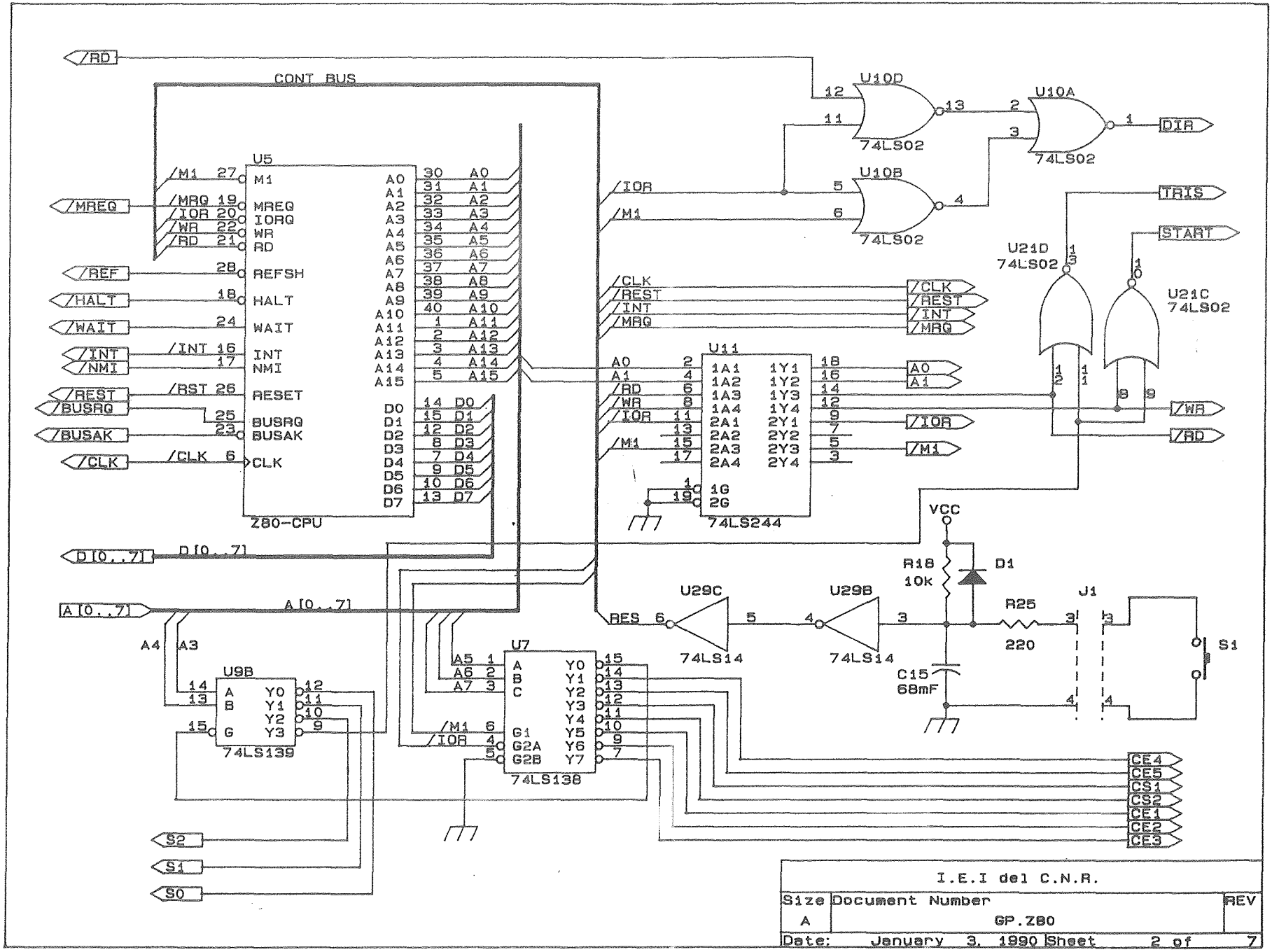


Fig.2 CPU e Decodifica

Con riferimento alla fig.3 si puo' osservare che e' possibile utilizzare fino a 32 Kbyte di memoria RAM-ROM selezionabili attraverso il commutatore S1 e il decodificatore 2/4 montato sullo zoccolo U9B. Sugli zoccoli U1, U2, U3, U4 possono essere inserite sia memorie di tipo ROM che RAM, da 28 o da 24 pin, purche' queste ultime vengano opportunamente inserite come e' indicato in fig.4. Da questa si evince che il piedino (21)-23 puo' assumere diverse funzioni:

- A11 se vengono inserite memorie da 8 Kbyte
- la funzione /WR se vengono usate RAM statiche
- Vpp se vengono usate EPRON da 2 kbyte

La fig.5 mostra la posizione dei ponticelli da effettuare, in funzione del tipo di memoria utilizzata, per soddisfare le funzioni sopra descritte e con la considerazione che anche l'ultima funzione viene soddisfatta perche' durante il ciclo di lettura il segnale /WR rimane a livello alto. Nella figura e' riportato anche l'indicazione per il posizionamento dell'interruttore R che viene ponticellato solo quando si inserisce una RAM dinamica che necessita di refrech; e' inoltre riportata la posizione fisica all'interno della scheda di S ed R. La connessione della scheda con altre apparecchiature o altre schede e' assicurata tramite il connettore J0 sul quale sono riportati oltre che al bus dati, controllo ed indirizzi, anche i segnali piu' significativi presenti sulla scheda.

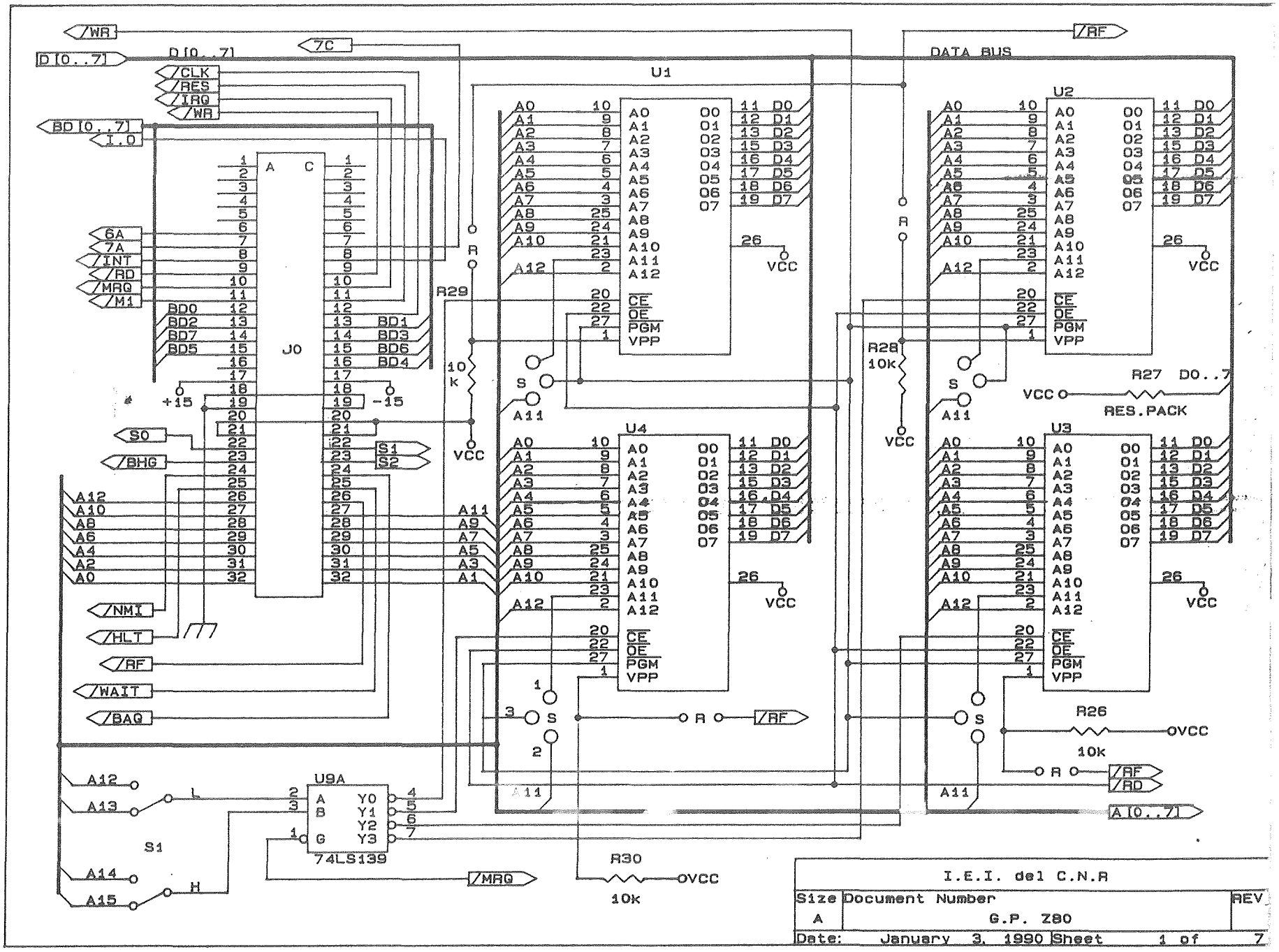


Fig.3 Memorie

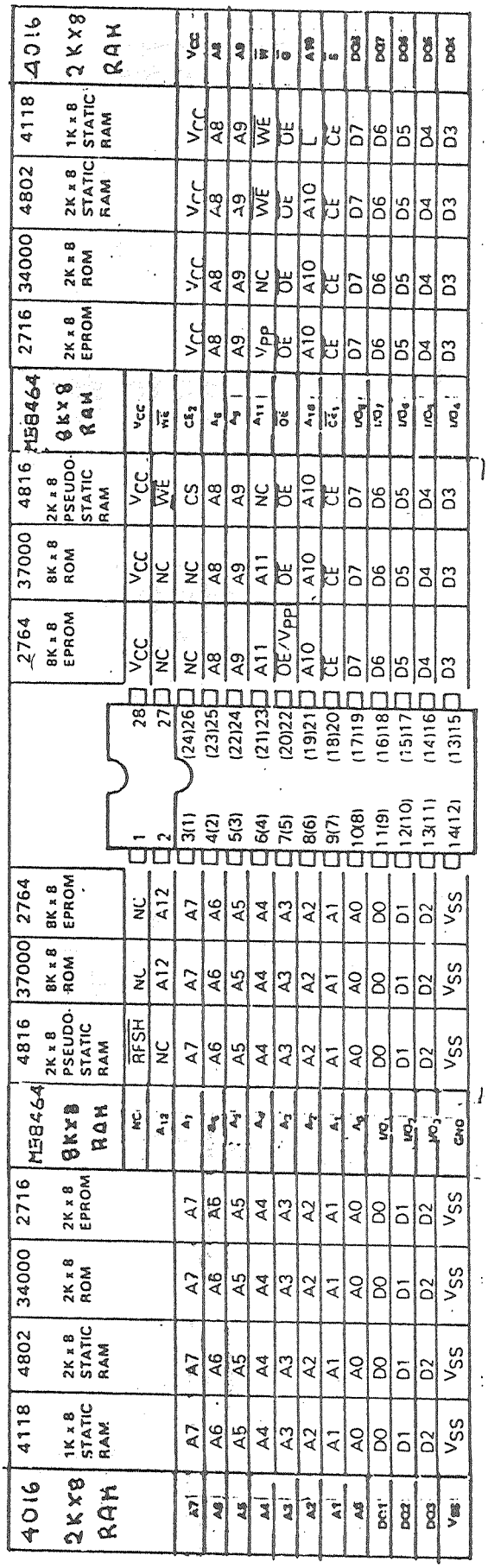
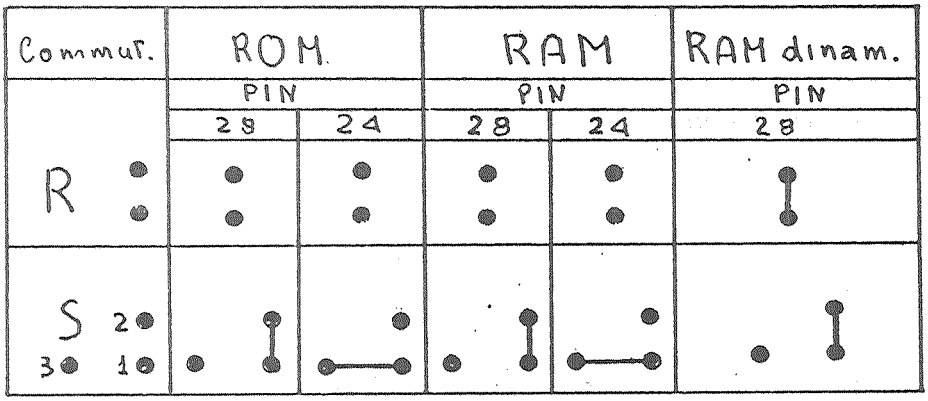


Fig.4 Panoramica dei diversi tipi di memorie



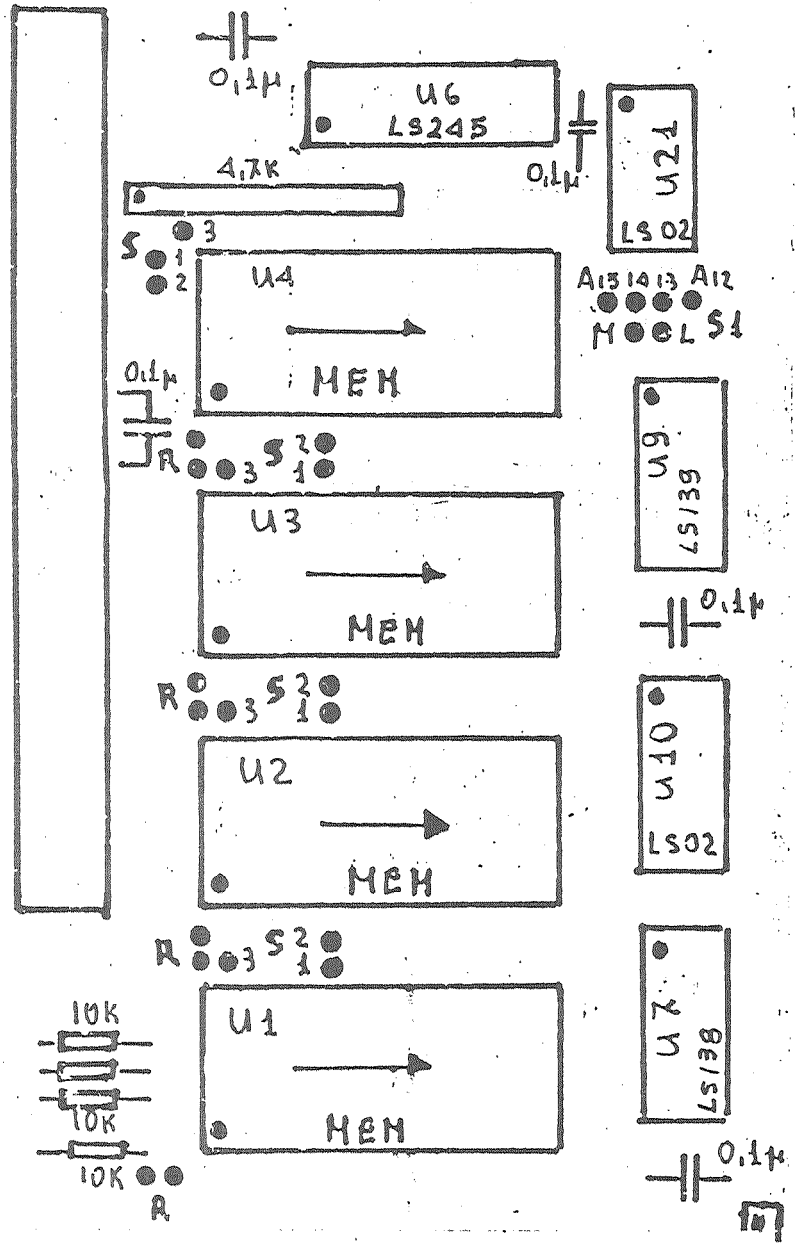


Fig.5 Collegamenti dei commutatori per i diversi tipi di memorie

Con riferimento alla fig.6 si puo' osservare che sugli zoccoli U13, U14 vengono montate le due porte parallele programmabili PIO (tipo MK 3881) che sono collegate con l'esterno tramite i due connettori a 26 contatti J2 e J3. I collegamenti su questi connettori sono tali che su ognuno di essi e' possibile anche inserire due connettori a 10 contatti necessari per collegare indipendentemente ogni canale del PIO.

Il bit 0 del canale A del PIO montato sullo zoccolo U13 non e' portato sul connettore ma e' collegato al convertitore A/D per leggere il segnale di EOC. Per completezza riportiamo per esteso gli indirizzi dei due PIO:

PIO A	Porta A	Porta B
U13	20H dati	22H dati
	21H controllo	23H controllo
PIO B	Porta A	Porta B
U14	40H dati	42H dati
	41H controllo	43H controllo

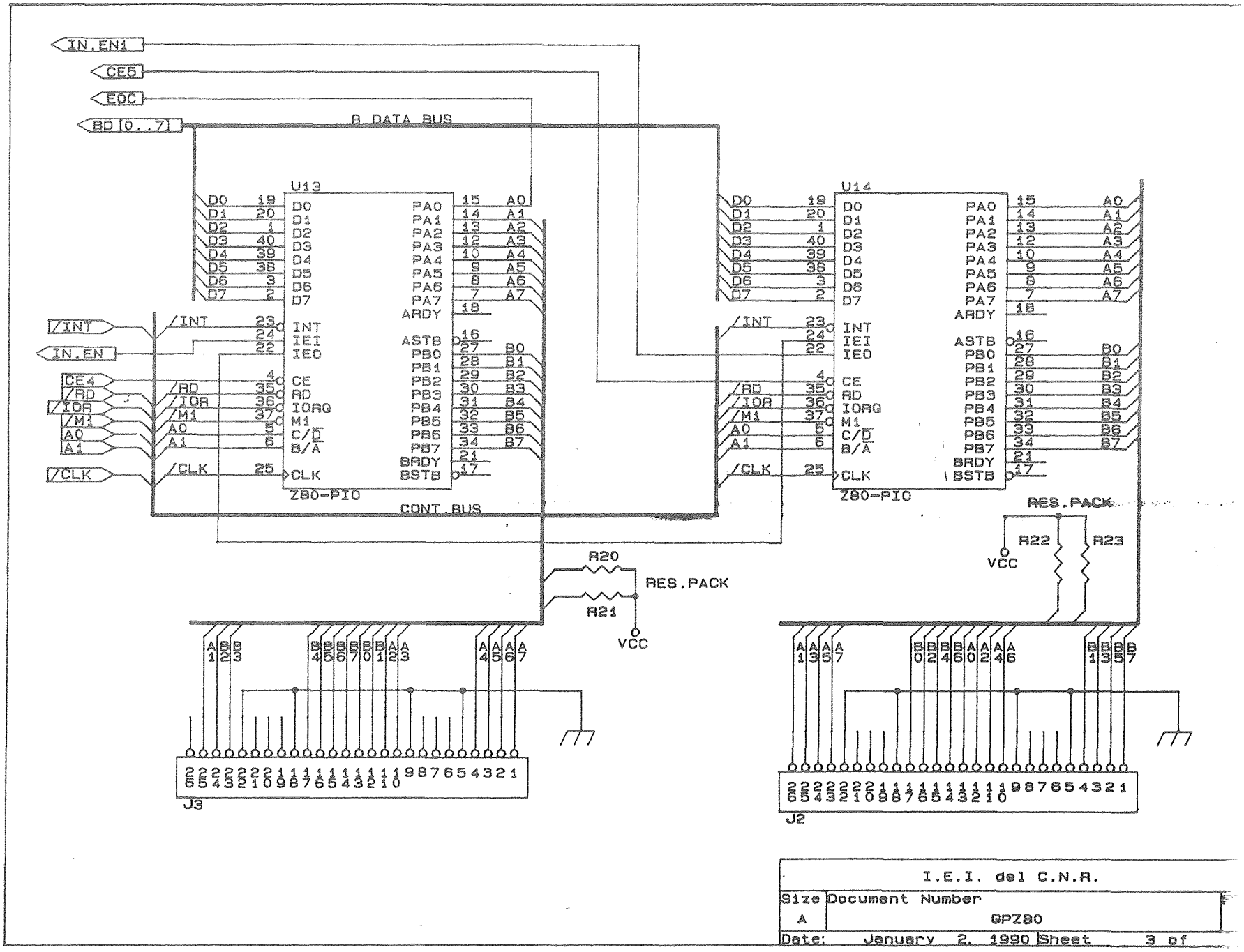


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Fig.6 Porte parallele

La fig.7 mostra che la porta seriale SIO (tipo MK3884) e' montata sullo zoccolo U15 e per quello che riguarda il canale A e' seguita da due linee driver/reciver del tipo 75188 (zoccolo U23) per i segnali di uscita e 75189 (zoccolo U22) per i segnali di ingresso. Comunica con l'esterno tramite il connettore dual-in-line J5, la posizione dei collegamenti sul connettore e' tale che applicando a questo un cavo piatto i collegamenti corrispondono automaticamente a quelli standar EIA RS232 di un connettore a 25 pin, caratteristico dei collegamenti seriali tra apparecchiature. Il clock che utilizza il SIO viene fornito ponticellando il commutatore S2 (di fig.10) in maniera da avere la frequenza utile per una determinata velocita' di trasmissione dati. In particolare riportiamo le velocita' di trasmissione in funzione dei collegamenti su S2:

Piedino	Piedino	Velocita'
13	F	19200
13	C	9600
13	B	4800
13	A	2400
13	G	1200
13	H	600

L'altro canale del SIO non e' bufferizzato e i segnali sono presenti sul connettore J6 a 10 contatti, su tale connettore sono pure presenti le tensioni per alimentare eventuali circuiti sperimentali. Riportiamo qui sotto gli indirizzi di utilizzazione del SIO:

SIO A	Porta A	Porta B
U15	E0H dati	E1H dati
	E2H controllo	E3H controllo

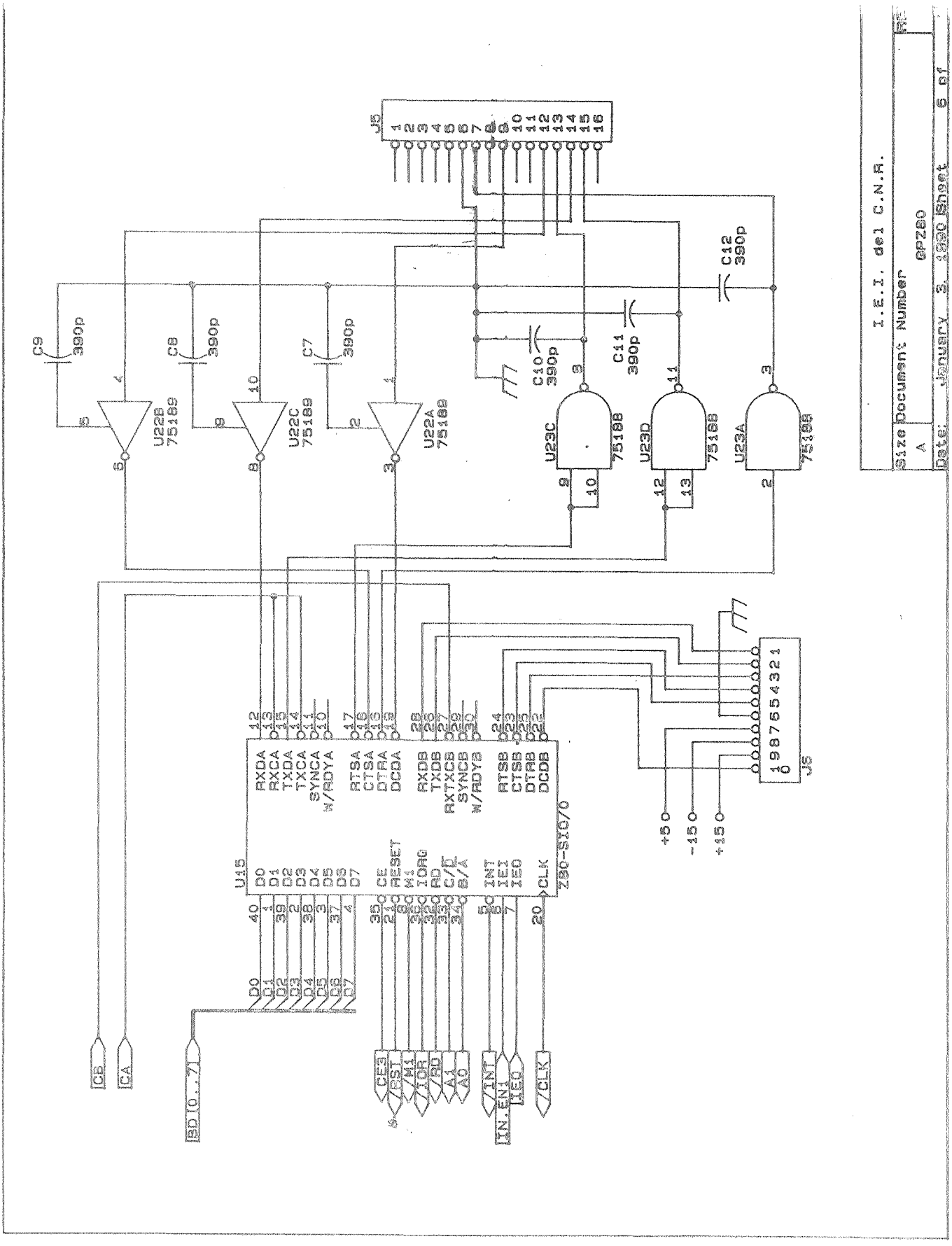

Fig.7 Porta seriale

Riferendoci alla fig.8 si nota che sugli zoccolini U19, U20 sono montati due convertitori D/A del tipo AD7542 a 12 bit di risoluzione. Il bus dati dello Z80 invia le parole a 12 bit che costituiscono gli ingressi dei convertitori suddividendole in blocchi di 4 bit. In particolare per il convertitore montato sullo zoccolo U19 si hanno i seguenti indirizzi di trasferimento: 60H, 61H, 62H e 63H, mentre per quello montato sullo zoccolo U20 gli indirizzi sono 80H, 81H, 82H e 83H. L'uscita del convertitore compresa tra 0 e 5 volt viene riportata sull'intervallo 0 e 12 volt mediante la coppia di amplificatori operazionali del tipo 741 montati sugli zoccoli U25, U26 e U27, U28. Sulla catena di reazione degli amplificatori e' previsto il montaggio di componenti per rendere il circuito particolarmente adatto per il pilotaggio di motori elettrici. Le uscite sono disponibili sul connettore dual-in-line J1 a 16 contatti piedino 15 e piedino 16.

In fig.9 si nota che sullo zoccolino U12 e' montato il convertitore analogico digitale ad approssimazioni successive ADC0816 CMOS, uscita tree-state TTL e CMOS compatibile con multiplexer analogico a 16 canali di ingresso. Tempo di conversione 108 µsec, 8 bit di risoluzione, errore di linearita' <1/2 LSB, errore globale (comprendente dell'errore di quantizzazione) < 1 LSD.

Lo start, che opera solo via software, viene dato con un numero compreso tra 0 e 15, per indicare su quale canale iniziare la conversione, un decodificatore ad 4 bit, interno al convertitore provvedera' a selezionare il canale richiesto, in seguito alla commutazione positiva dell'Addres Latch Enable (ALE). E' da

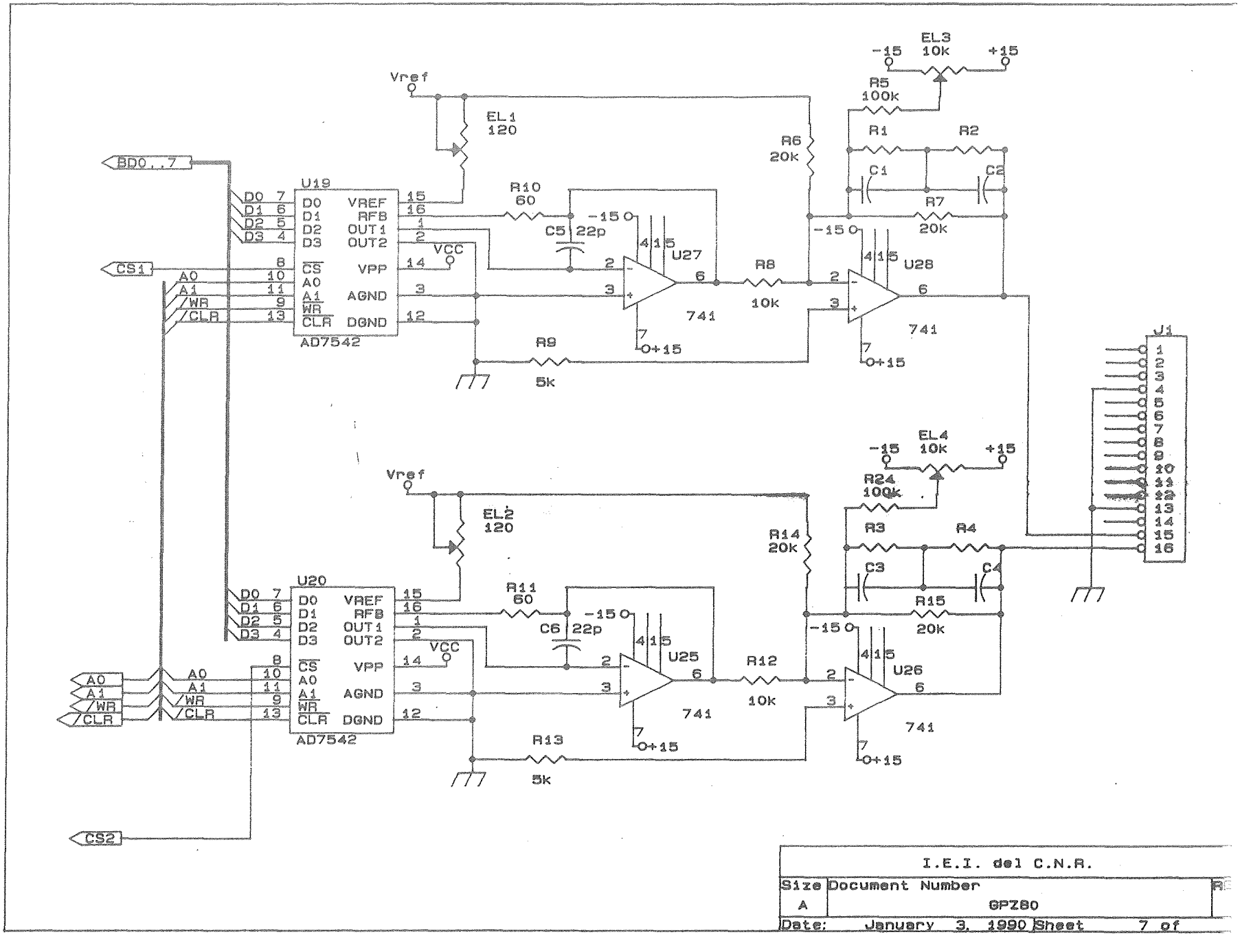

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Fig.8 Convertitori D/A

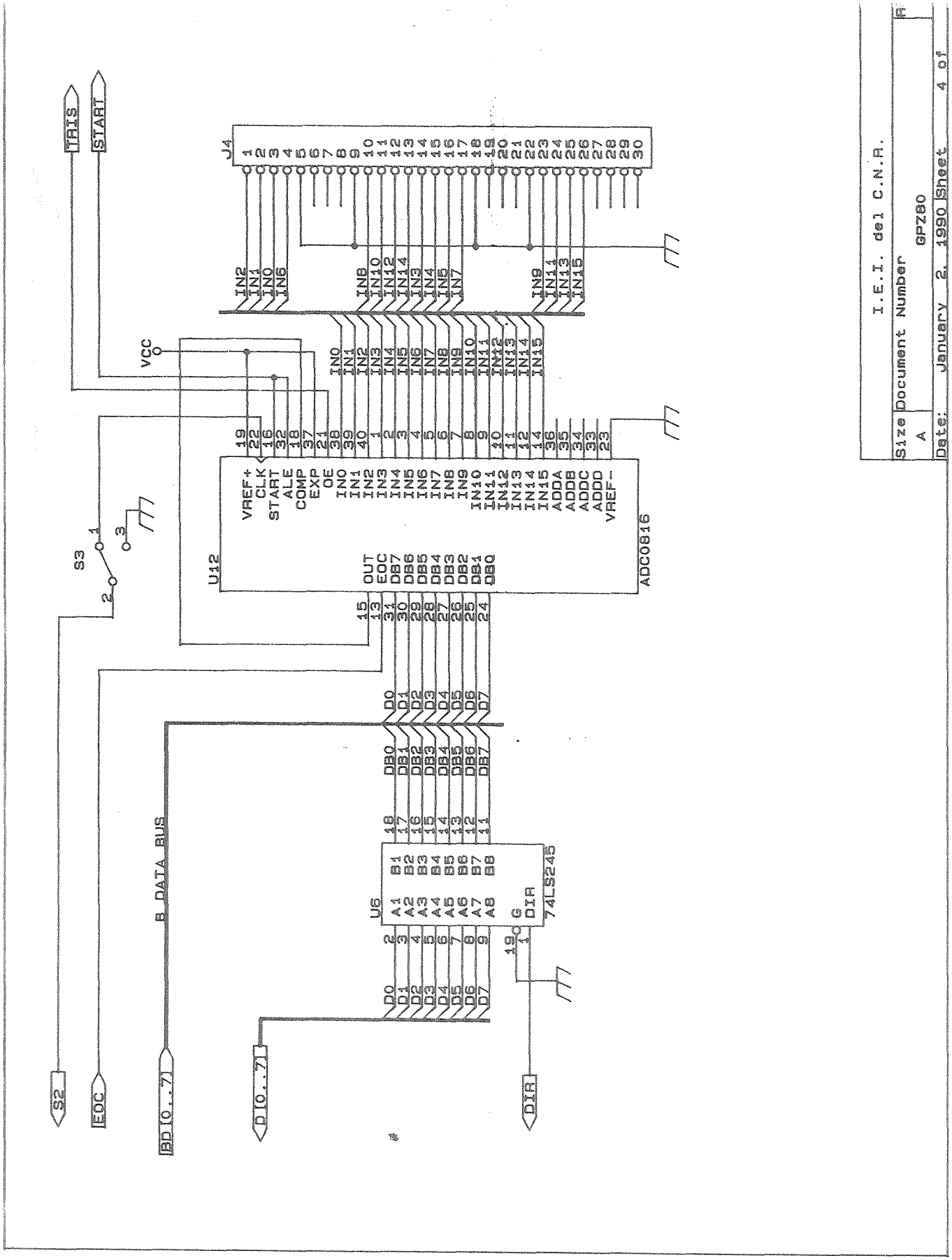

Fig.9 Convertitore A/D

notare che L'Espansion Control (EC) e' stato messo a Vpp per abilitare sempre la selezione di un canale. Collegando i piedini 1 e 2 del commutatore S3 il convertitore opera su clock esterno, mentre collegando i piedini 1-3 esso opera su clock interno (possibilita' offerta dall'A/D converter della mostek ADMK50816). I valori delle frequenze del clock devono essere comprese fra 100 KHz e 1200 KHz con valore consigliato di 640 KHz. Per ottenere una frequenza la piu' vicina possibile a detto valore si utilizza il piedino del selettore S2 che divide per 4 la frequenza del clock di sistema e con riferimento alla fig.10 si collega il piedino E con il piedino 11 avendo naturalmente cura di aver effettuato il collegamento 1-2 sul commutatore S3. Il micrologico 74LS245 montato sullo zoccolo U6 ha la funzione di buffer per il bus di dati. Gli ingressi analogici sono collegati sul connettore J4.
E' stato utilizzato anche il primo bit del canale A della porta parallela Z80-PIO (canale A bit 0) al fine di poter leggere l'End Of Conversion (EOC) dell'A/D converter.

In fig 10 sono mostrati due circuiti CTC montati sugli zoccoli U16 e U17 con funzioni di temporizzazione e conteggio. I piedini disponibili del CTCA caratterizzato per la temporizzazione sono portati al connettore J1 nella posizione indicata dalla figura, mentre quelli relativi al CTCB sono portati al selettore S2 per i collegamenti del caso.
Su detto selettore sono riportate anche le uscite di un divisore di frequenza, micrologico 74LS393 montato sullo zoccolo U18, che divide la frequenza del clock di sistema, secondo la seguente tabella:

D	2
E	4
F	8
C	16
B	32
A	64
G	128
H	256

Per cui su questo selettore si prelevera' la frequenza di clock necessaria per il convertitore A/D, per il SIO, e per il CTC. Sullo zoccolo U24 e' montato il circuito di clock che utilizza un quarzo da 2,457 MHz, tale frequenza e' particolarmente utile per la temporizzazione delle trasmissioni seriali. Per completezza riportiamo per esteso gli indirizzi dei due CTC:

CTC A	Porta 0	Porta 1	Porta 2	Porta3
U16	A0H	A1H	A2H	A3H

CTC B	Porta 0	Porta 1	Porta 2	Porta3
U17	C0H	C1H	C2H	C3H

La fig 11 mostra la posizione dei componenti sulla basetta, il connettore J0 a triplice fila di contatti sul quale sono riportati i segnali piu' significativi per l'inserimento della basetta su di un rack, il connettore J4 per gli ingressi analogici del convertitore A/D, J1 per le uscite dei convertitori D/A e del temporizzatore, i connettori J2 e J3 per le porte parallele, J5 per la porta seriale,

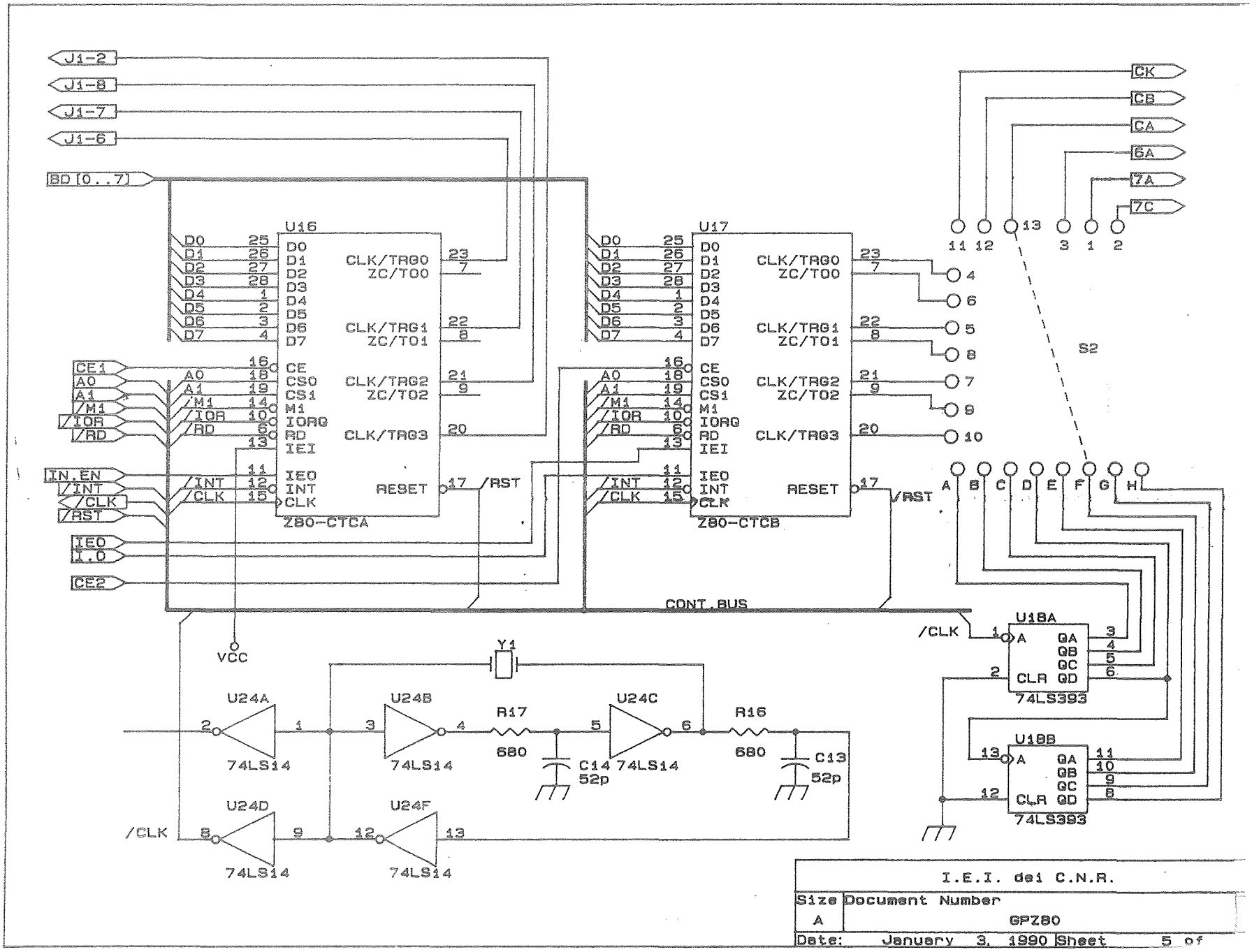

Fig.10 Temporizzatori

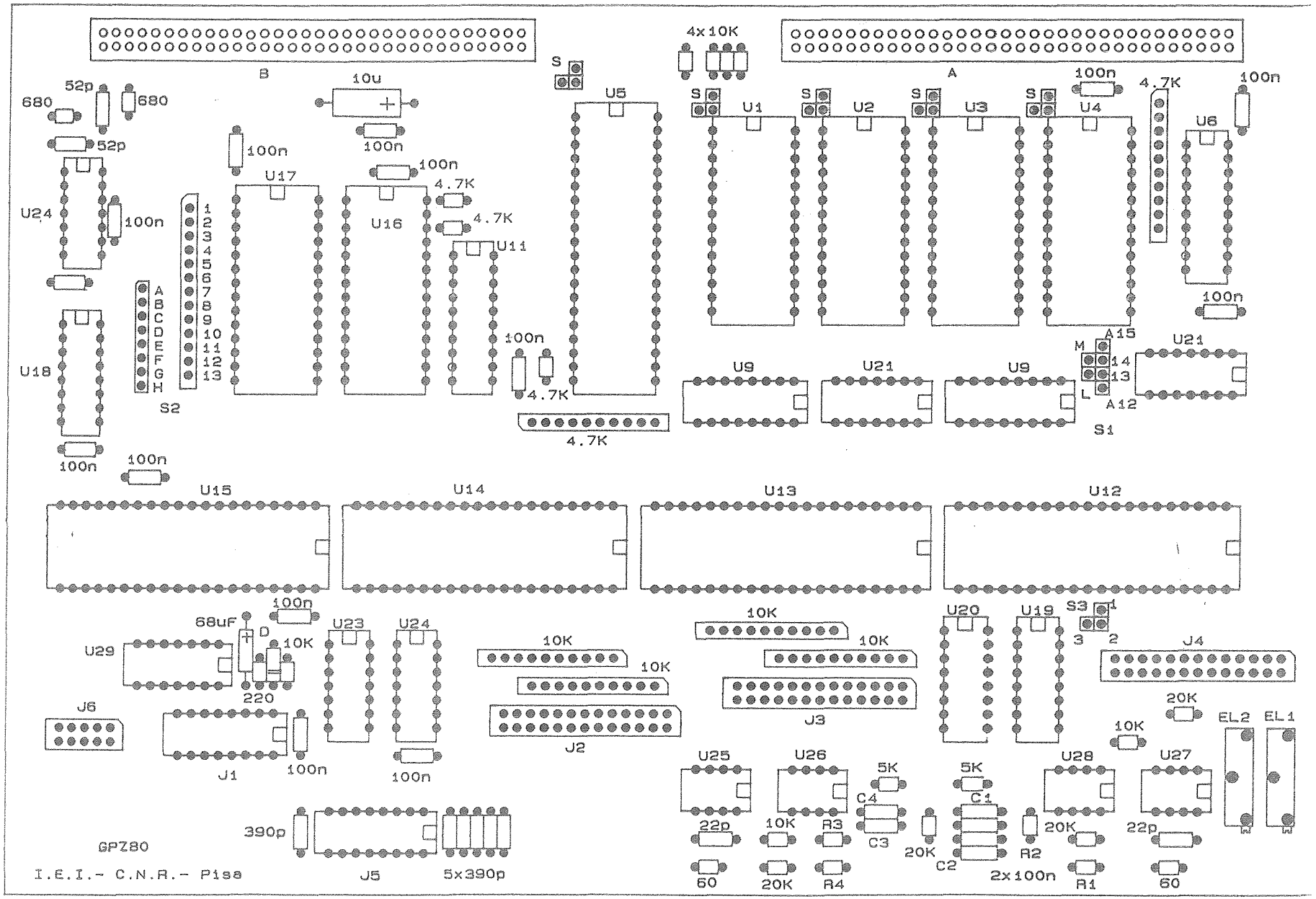

Fig.11 Planimetria della scheda

mentre su J6 e' collegata la porta seriale non adattata e le tensioni di alimentazione per la parte della basetta riservata ad ulteriori espansioni. Su questa parte della scheda la superficie superiore e' collegata alla tensione mentre quella inferiore e' collegata a massa; e' inoltre riportata la posizione dei vari commutatori S, S1, S2, S3 il cui posizionamento e' stato precedentemente descritto.

NB. Prima di utilizzare la scheda occorre togliere il passante tra il piedino 4 e 12 dello zoccolo U5 e montare una resistenza da 10k sul collegamento relativo a /WR.

G.P. Z80 Revised: January 3, 1990
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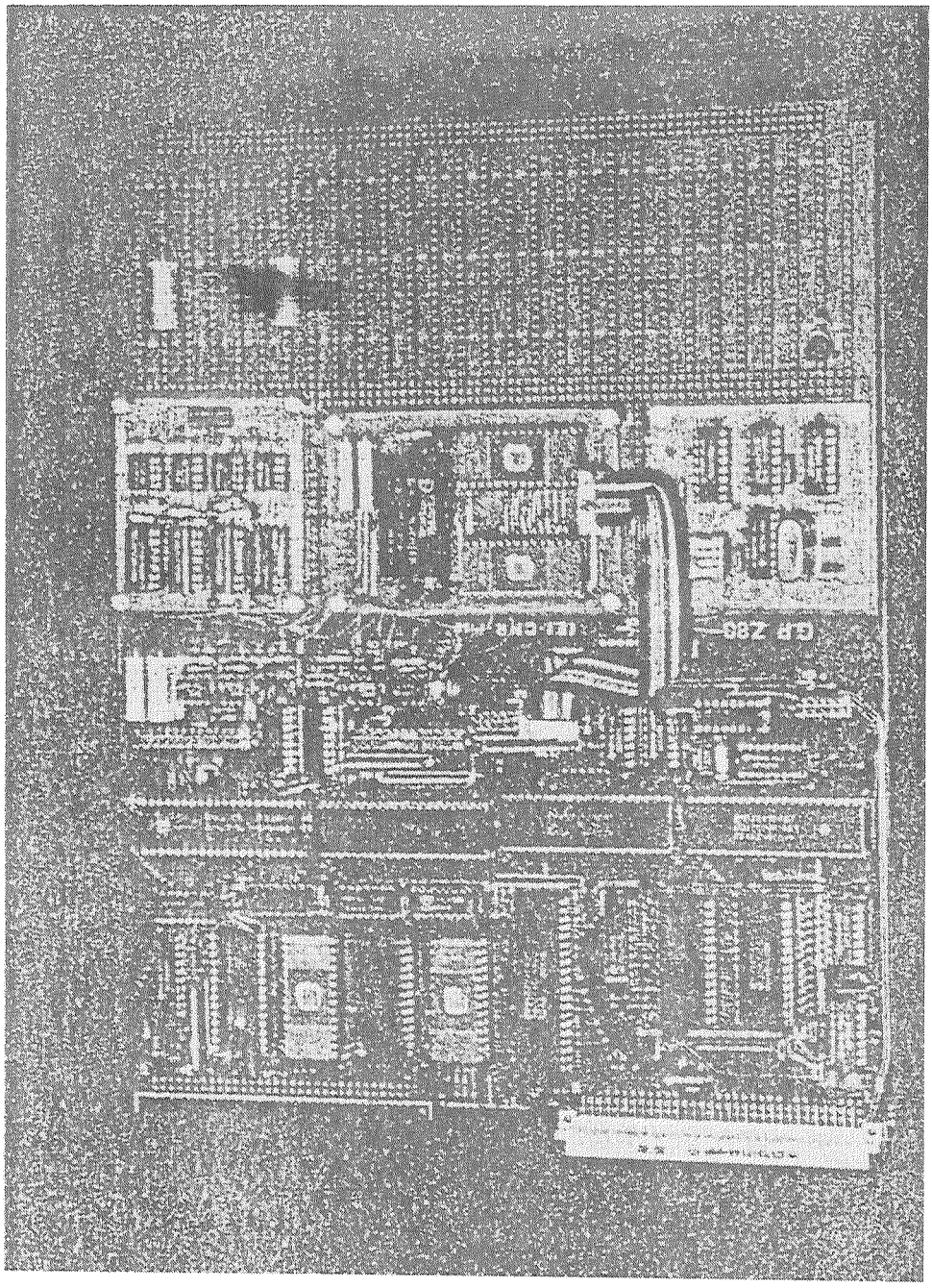
Item	Quantity	Reference	Part
1	21	1,2,3,4,5,6,7,8,9,10,11, 12,13,A,B,C,D,E,F,G,H	piaz.
2	4	C1,C2,C3,C4	CAP
3	2	C5,C6	22p
4	6	C7,C8,C9,C10,C11,C12	390p
5	2	C13,C14	52p
6	1	C15	68mF
7	1	D1	DIODE
8	2	EL1,EL2	120
9	8	EL3,EL4,R0,R12,R18,R26, R28,R30	10k
10	1	J0	EDGE32X2
11	2	J1,J5	HEADER16
12	1	J2	HEADER26x2
13	1	J3	HEADER 26x2
14	1	J4	HEADER30
15	1	J6	HEADER10
16	4	R1,R2,R3,R4	RES.
17	2	R5,R24	100k
18	4	R6,R7,R14,R15	20k
19	2	R8,R17	5k
20	2	R10,R11	60
21	2	R16,R17	680
22	2	R20,R22	4.7K
23	3	R21,R23,R27	RES. PACK
24	1	R25	220
25	1	R29	10K
26	2	S1,S2	SW

Item	Quantity	Reference	Part
27	1	S1	SW-PUSH
28	4	U1, U2, U3, U4	MEMORY
29	1	U5	Z80-CPU
30	1	U6	74LS245
31	1	U7	74LS138
32	1	U9	74LS139
33	2	U10, U21	74LS02
34	1	U11	74LS244
35	1	U12	ADC0816
36	2	U13, U14	Z80-PIO
37	1	U15	Z80-SIO/0
38	1	U16	Z80-CTCA
39	1	U17	Z80-CTCB
40	1	U18	74LS393
41	2	U19, U20	AD7542
42	1	U22	75189
43	1	U23	75188
44	2	U24, U29	74LS14
45	4	U25, U26, U27, U28	741
46	1	Y1	CRYSTALL



La piastra GP/Z80 del controllo programmato CU

MOSTEK®

2048 x 8-BIT EPROM

Electrically Programmable/Ultraviolet Erasable ROM

MK2716 (J)-5/6/7/8

FEATURES

- 16,384 Bit Ultraviolet Erasable, Electrically Programmable ROM, organized as 2048 words by 8 bits
- Single +5 volt power supply during READ operation
- Fast Access Time in READ mode

P/N	ACCESS TIME
MK2716-5	300ns
MK2716-6	350ns
MK2716-7	390ns
MK2716-8	450ns

- Low Power Dissipation: 525mW max active
- Power Down Mode: 132mW max standby
- Three State Output OR-tie capability
- Five modes of operation for greater system flexibility (see Table)
- Single programming requirement: single location programming with one 50msec pulse
- Pin Compatible with Mostek's BYTEWYDE™ Memory Family
- TTL compatible in all operating modes
- Standard 24 pin DIP with transparent lid

ROMS

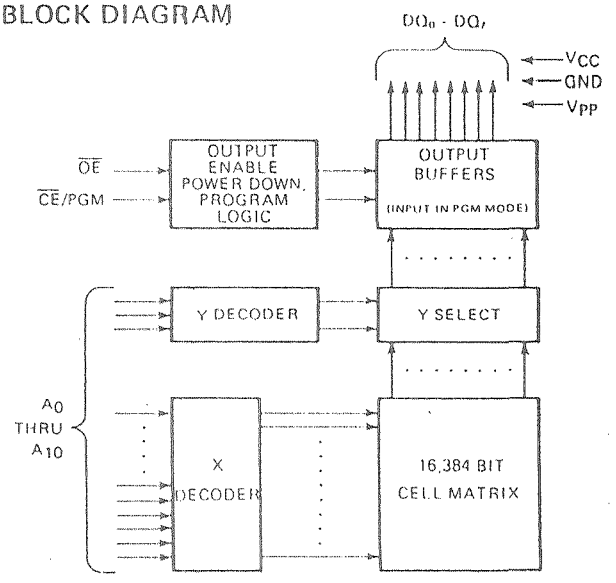
DESCRIPTION

The MK2716 is a 2048 x 8 bit electrically programmable/ultraviolet erasable Read Only Memory. The circuit is fabricated with Mostek's advanced N-channel silicon gate technology for the highest performance and reliability. The MK2716 offers significant advances over

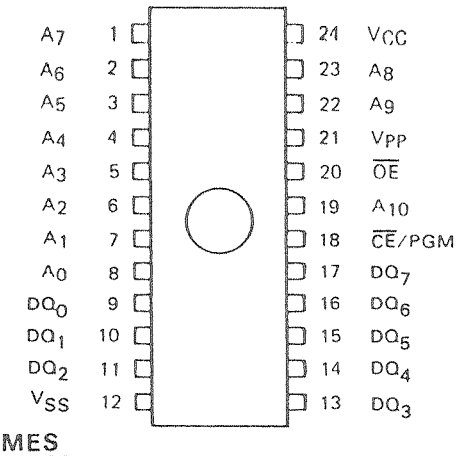
MODE SELECTION

MODE / PIN	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	VPP (21)	OUTPUTS
READ	V_{IL}	V_{IL}	+5	Valid Out
STANDBY	V_{IH}	Don't Care	+5	Open
PROGRAM	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	Input
PROGRAM VERIFY	V_{IL}	V_{IL}	+25	Valid Out
PROGRAM INHIBIT	V_{IL}	V_{IH}	+25	Open
V_{CC}(24) = 5V all modes				

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

A_0-A_{10}	Addresses	DQ_0-DQ_7	Data Outputs*
$\overline{CE}$/PGM	Chip Enable/ Program	$\overline{OE}$	Output Enable
		V_{SS}	Ground

*Inputs in Program Mode

PRELIMINARY

MOSTEK

4K x 1-BIT STATIC RAM

MK2147(J)-55/70/85

FEATURES

- Scaled Poly 5™ technology
- Industry standard 18-pin dip configuration
- High performance

Part Number	Access Time	Cycle Time	Power Supply Current: Max. Active	Power Supply Current: Max. Standby
MK2147-55	55ns	55ns	180mA	30mA
MK2147-70	70ns	70ns	160mA	20mA
MK2147-85	85ns	85ns	160mA	20mA

- Address Activated™ static memory—no clock or timing strobe required
- Access time equal cycle time
- Chip select power down feature
- Single +5V (±10%) power supply
- On-chip substrate bias generator
- All inputs are low capacitance and TTL compatible
- Three-state TTL compatible output

DESCRIPTION

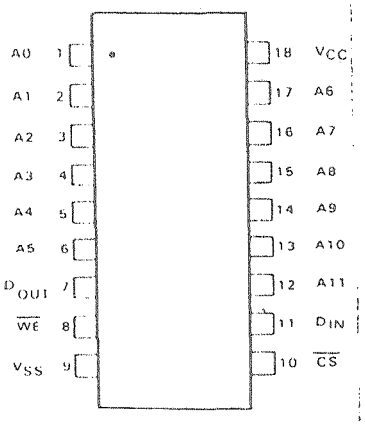
The MK2147 uses MOSTEK's Scaled Poly 5™ process and advanced circuit design techniques to package 4096 words by 1-bit of static RAM on a single chip requiring a single +5 volt supply. The MK2147 is functionally equivalent and pin compatible with the established industry standard 18-pin high performance 4K x 1 static RAM.

MOSTEK's Address Activated™ circuit design technique is utilized to achieve high performance, low power, and easy user implementation. The device has a VIH = 2.0V, VIL = 0.8V, VOH = 2.4V, and VOL = 0.4V making it totally compatible with all TTL family devices. The MK2147 has a chip select power down feature which automatically reduces the power dissipation when the chip select, $\overline{CS}$, is brought inactive (high).

The MK2147 is designed for memory applications that require high bit densities, fast access, and short cycle times. The MK2147 offers the user a high density cost effective alternative to bipolar and previous generation N-MOS fast memory.

STATIC RAMS

PIN CONNECTION



PIN NAMES

A0 - A11	ADDRESS INPUTS
$\overline{CS}$	CHIP SELECT
DIN	DATA INPUT
DOUT	DATA OUTPUT
VSS	GROUND
VCC	POWER (+5V)
$\overline{WE}$	WRITE ENABLE

TRUTH TABLE

CS	WE	MODE	OUTPUT	POWER
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	D_{OUT}	Active

3.0 Z80-CPU PIN DESCRIPTION

The Z80-CPU is packaged in an industry standard 40 pin Dual In-Line Package. The I/O pins are shown in Figure 3.0-1 and the function of each is described below.

Z80 PIN CONFIGURATION

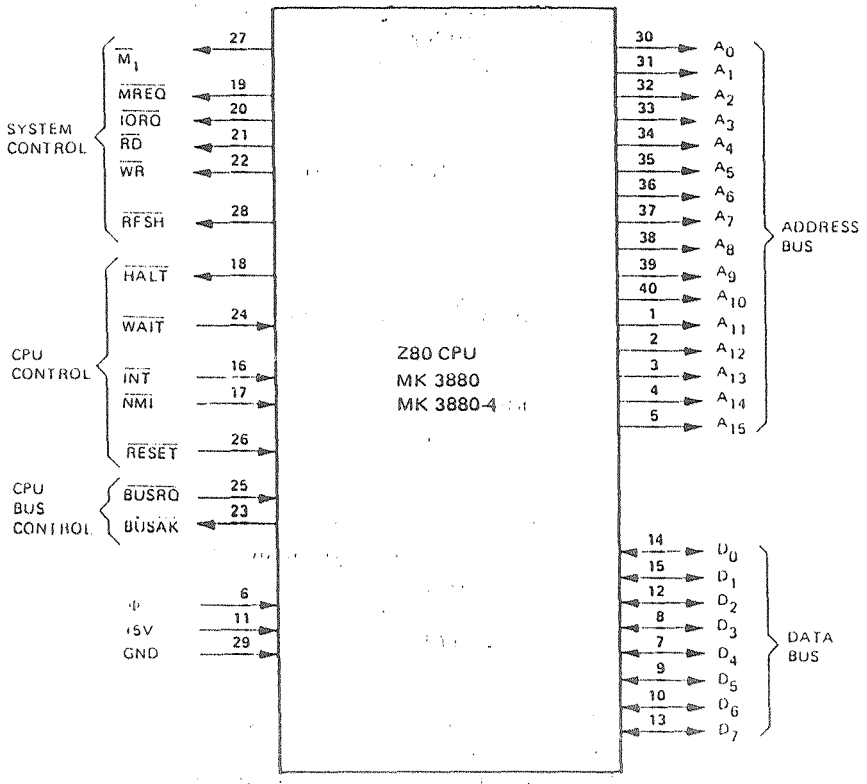


FIGURE 3.0-1

A_0-A_{15} (Address Bus)
Tri-state output, active high. A_0-A_{15} constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the 8 lower address bits to allow the user to directly select up to 256 input or 256 output ports. A_0 is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address.

D_0-D_7 (Data Bus)
Tri-state input/output, active high. D_0-D_7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.

$\overline{M_1}$ (Machine Cycle one)
Output, active low. $\overline{M_1}$ indicates that the current machine cycle is the OP code fetch cycle of an instruction execution. Note that during execution of 2-byte op-codes, $\overline{M_1}$ is generated as each op code byte is fetched. These two byte op-codes always begin with CBH, DDH, EDH, or FDH. $\overline{M_1}$ also occurs with $\overline{IORQ}$ to indicate an interrupt acknowledge cycle.

$\overline{MREQ}$ (Memory Request)
Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.

$\overline{IORQ}$
(Input/Output Request)

Tri-state output, active low. The $\overline{IORQ}$ signal indicates that the lower half of the address bus holds a valid I/O address for a I/O read or write operation. An $\overline{IORQ}$ signal is also generated with an $\overline{M_1}$ signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during M_1 time while I/O operations never occur during M_1 time.

$\overline{RD}$
(Memory Read)

Tri-state output, active low. $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

$\overline{WR}$
(Memory Write)

Tri-state output, active low. $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.

$\overline{RFSH}$
(Refresh)

Output, active low. $\overline{RFSH}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and current $\overline{MREQ}$ signal should be used to do a refresh read to all dynamic memories. A_7 is a logic zero and the upper 8 bits of the Address Bus contains the I Register.

Device Family

$\overline{HALT}$
(Halt state)

Output, active low. $\overline{HALT}$ indicates that the CPU has executed a HALT software instruction and is awaiting either a non maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.

$\overline{WAIT}$*
(Wait)

Input, active low. $\overline{WAIT}$ indicates to the Z80-CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. This signal allows memory or I/O devices of any speed to be synchronized to the CPU.

$\overline{INT}$
(Interrupt Request)

Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the $\overline{BUSRQ}$ signal is not active. When the CPU accepts the interrupt, an acknowledge signal ($\overline{IORQ}$ during M_1 time) is sent out at the beginning of the next instruction cycle. The CPU can respond to an interrupt in three different modes that are described in detail in section 8.

$\overline{NMI}$

Input, negative edge triggered. The non maskable interrupt request line has a higher priority than $\overline{INT}$ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. $\overline{NMI}$ automatically forces the Z80-CPU to restart to location 0066_H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycles can prevent the current instruction from ending, and that a $\overline{BUSRQ}$ will override a $\overline{NMI}$.

$\overline{\text{RESET}}$	Input, active low. $\overline{\text{RESET}}$ forces the program counter to zero and initializes the CPU. The CPU initialization includes: 1) Disable the interrupt enable flip-flop 2) Set Register I = 00_H 3) Set Register R = 00_H 4) Set Interrupt Mode 0 During reset time, the address bus and data bus go to a high impedance state and all control output signals go to the inactive state. No refresh occurs.
$\overline{\text{BUSRQ}}$ (Bus Request)	Input, active low. The bus request signal is used to request the CPU address bus, data bus and tri-state output control sighals to go to a high impedance state so that other devices can control these buses. When $\overline{\text{BUSRQ}}$ is activated, the CPU will set these buses to a high impedance state as soon as the current CPU machine cycle is terminated.
$\overline{\text{BUSAK}}$* (Bus Acknowledge)	Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.
Φ	Single phase system clock.

*While the Z80-CPU is in either a $\overline{\text{WAIT}}$ state or a Bus Acknowledge condition, Dynamic Memory Refresh will not occur.

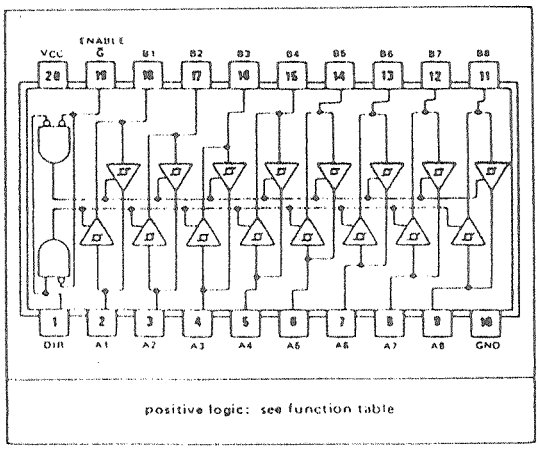
TYPES SN54LS245, SN74LS245
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7612471, OCTOBER 1976

- Bi-directional Bus Transceiver in a High-Density 20-Pin Package
- 3-State Outputs Drive Bus Lines Directly
- P-N-P Inputs Reduce D-C Loading on Bus Lines
- Hysteresis at Bus Inputs Improve Noise Margins
- Typical Propagation Delay Times, Port-to-Port . . . 8 ns
- Typical Enable/Disable Times . . . 17 ns

TYPE	I_{OL} (SINK CURRENT)	I_{OH} (SOURCE CURRENT)
SN54LS245	12 mA	−12 mA
SN74LS245	24 mA	−15 mA

SN54LS245 . . . J PACKAGE
SN74LS245 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

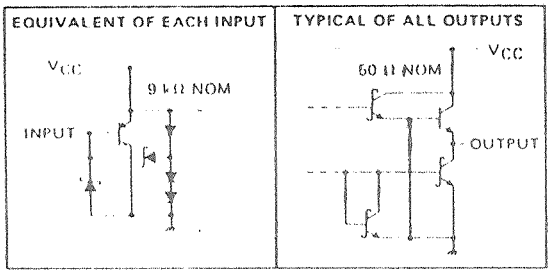
description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

The SN54LS245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS245 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

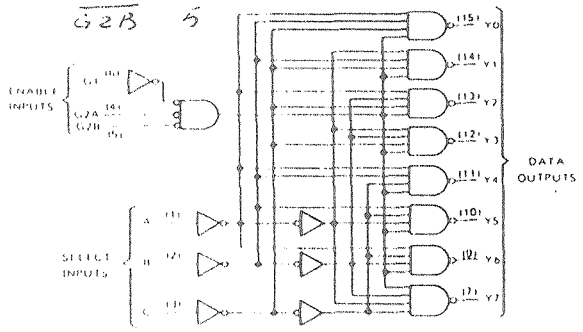
Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS245 . . . . . −55°C to 125°C
SN74LS245 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

DESIGN GOAL
This page provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

functional block diagrams and logic

'LS138, 'S138



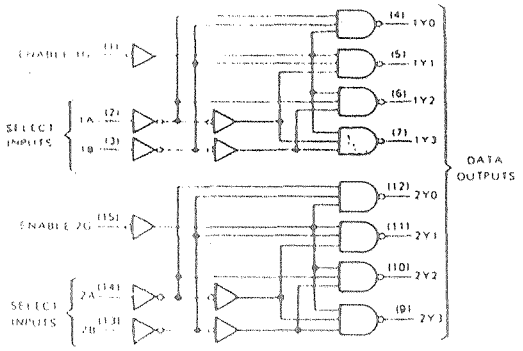
'LS138, 'S138
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

H = high level, L = low level, X = irrelevant

'LS139, 'S139



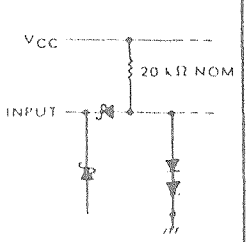
'LS139, 'S139
(EACH DECODER/DEMULTIPLEXER)
FUNCTION TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

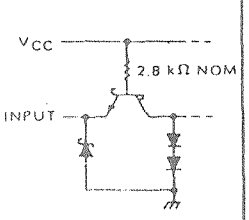
H = high level, L = low level, X = irrelevant

schematics of inputs and outputs

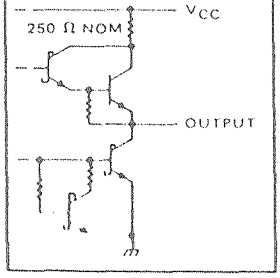
EQUIVALENT OF EACH INPUT OF 'LS138, 'LS139



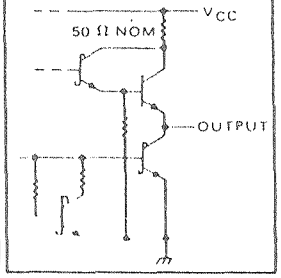
EQUIVALENT OF EACH INPUT OF 'S138, 'S139



TYPICAL OF OUTPUTS OF 'LS138, 'LS139



TYPICAL OF OUTPUTS OF 'S138, 'S139



TYPES SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

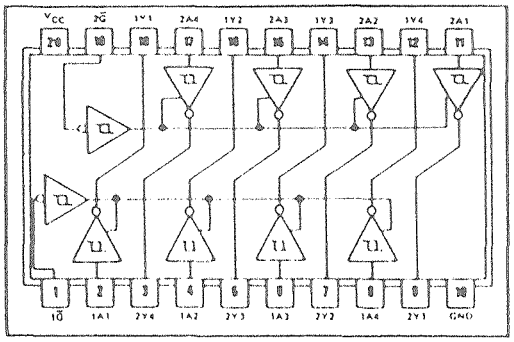
	Typical I_{OL} (Sink Current)	Typical I_{OH} (Source Current)	Typical Propagation Delay Times		Typical Enable/ Disable Times	Typical Power Dissipation (Enabled)	
			Inverting	Noninverting		Inverting	Noninverting
SN54LS'	12 mA	−12 mA	10.5 ns	12 ns	18 ns	130 mW	135 mW
SN74LS'	24 mA	−15 mA	10.5 ns	12 ns	18 ns	130 mW	135 mW
SN54S'	48 mA	−12 mA	4.5 ns	6 ns	9 ns	450 mW	538 mW
SN74S'	64 mA	−15 mA	4.5 ns	6 ns	9 ns	450 mW	538 mW

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins

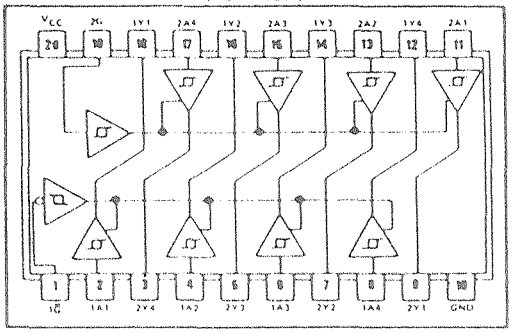
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out, improved fan-in, and 400 mV noise margin. The SN74LS' and SN74S' can be used to drive terminated lines down to 133 ohms.

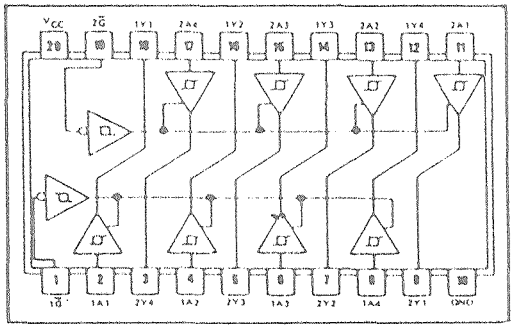
SN54LS240, SN54S240 . . . J
SN74LS240, SN74S240 . . . J OR N
(TOP VIEW)



SN54LS241, SN54S241 . . . J
SN74LS241, SN74S241 . . . J OR N
(TOP VIEW)

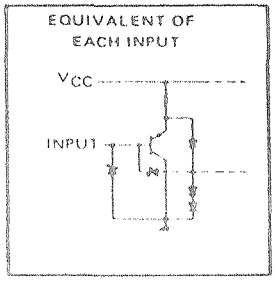


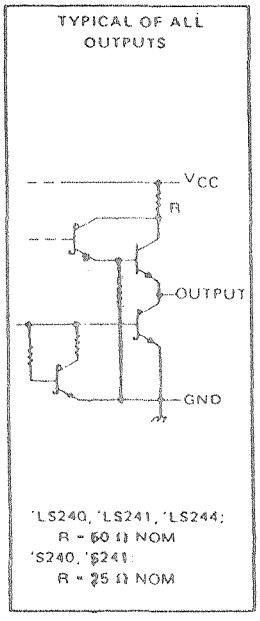
SN54LS244 . . . J
SN74LS244 . . . J OR N
(TOP VIEW)



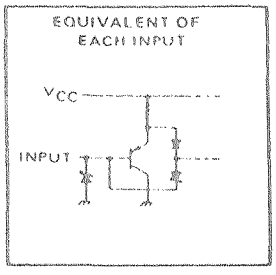
schematics of inputs and outputs

'LS240, 'LS241, 'LS244





'S240 'S241



National Semiconductor

ADC0816, ADC0817 8-Bit μP Compatible A/D Converters with 16-Channel Multiplexer

General Description

The ADC0816, ADC0817 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 16 channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 16-channel multiplexer can directly access any one of 16-single-ended analog signals, and provides the logic for additional channel expansion. Signal conditioning of any analog input signal is eased by direct access to the multiplexer output, and to the input of the 8-bit A/D converter.

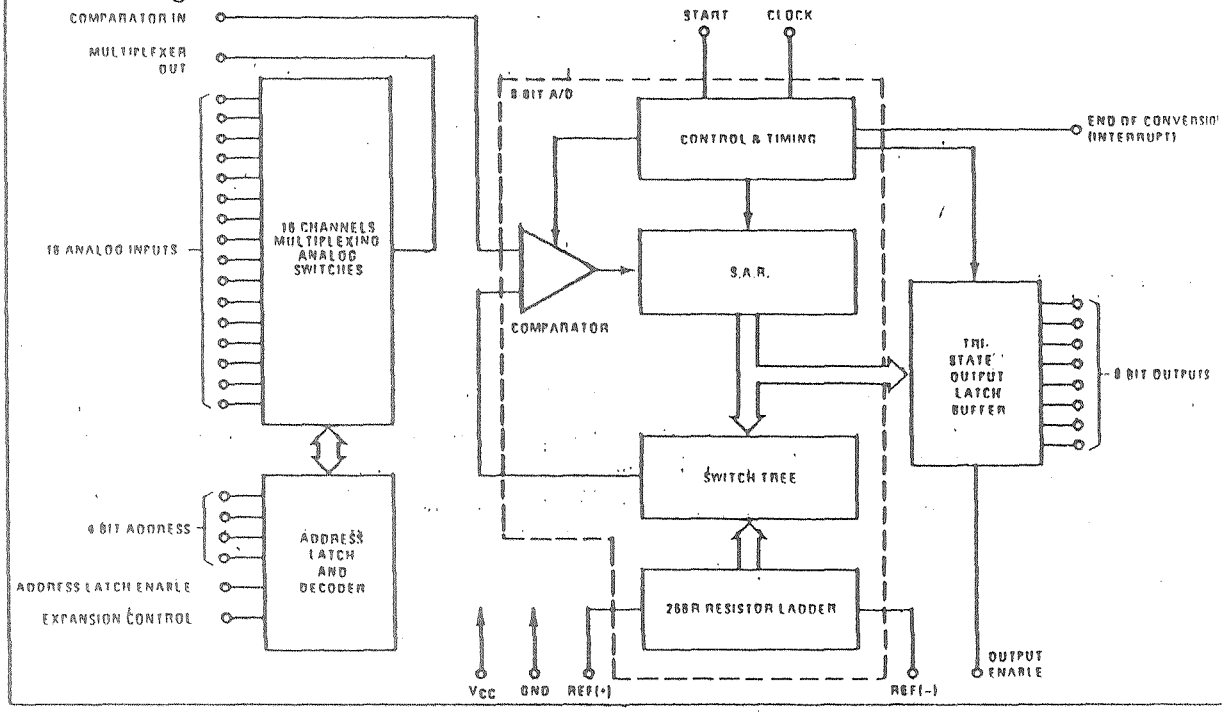
The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0816, ADC0817 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0816, ADC0817 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For similar performance in an 8-channel, 28-pin, 8-bit A/D converter, see the ADC0808, ADC0809 data sheet.

Features

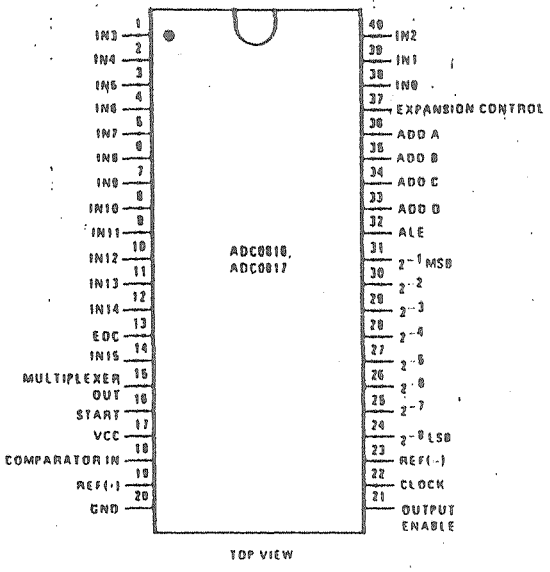
- Resolution — 8-bits
- Total unadjusted error — ± 1/2 LSB and ± 1 LSB
- No missing codes
- Conversion time — 100 μs
- Single supply — 5 V_{DC}
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- 16-channel multiplexer with latched control logic
- Easy interface to all microprocessors, or operates "stand alone"
- Outputs meet T^2L voltage level specifications
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Standard hermetic or molded 40-pin DIP package
- Temperature range −40°C to +85°C or −55°C to +125°C
- Low power consumption — 15 mW
- Latched TRI-STATE® output
- Direct access to "comparator in" and "multiplexer out" for signal conditioning

Block Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

Timing Diagram

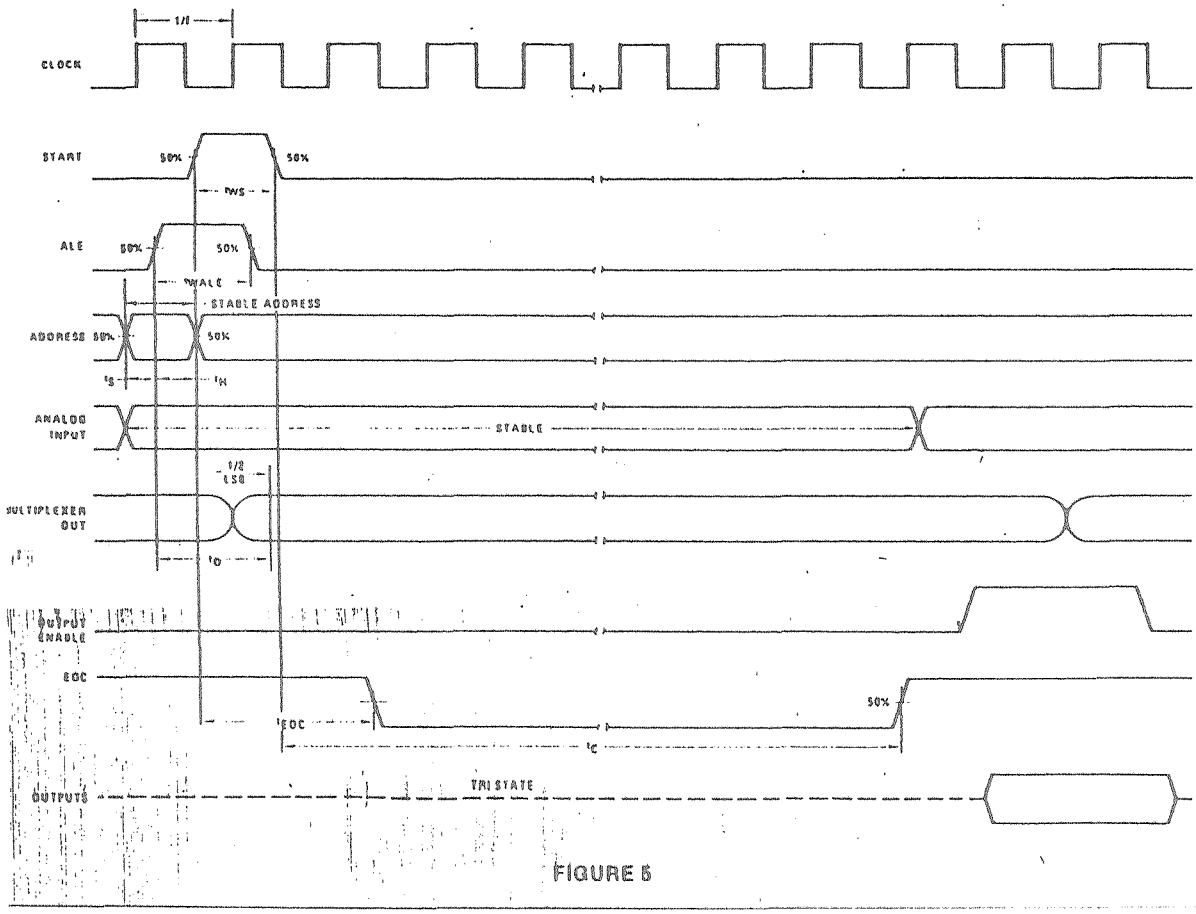
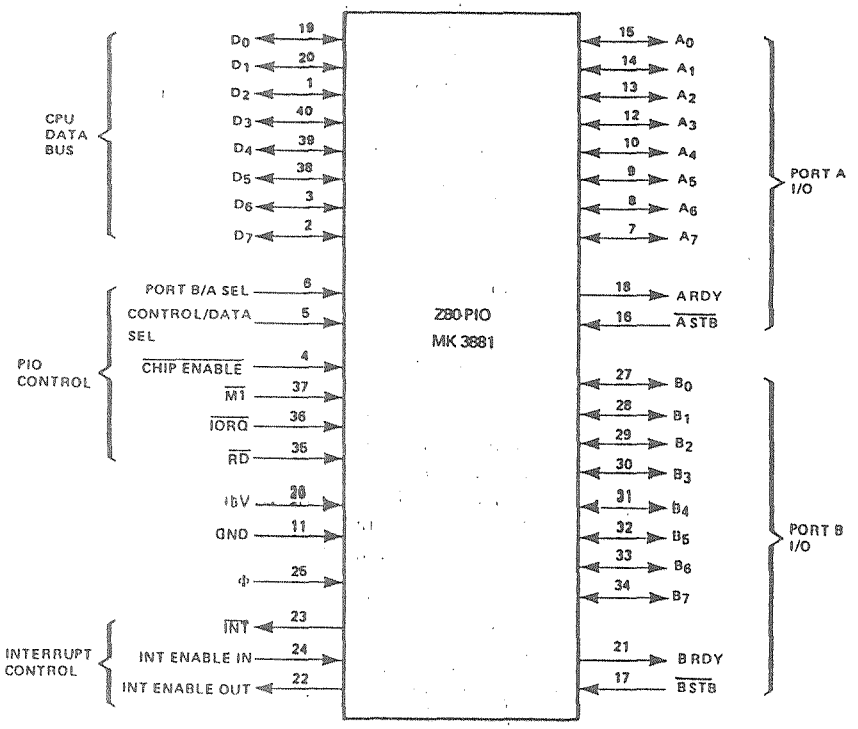


FIGURE 5

PIO PIN CONFIGURATION
Figure 3.0-1



3.0 PIN DESCRIPTION

A diagram of the Z80-PIO pin configuration is shown in figure 3.0-1. This section describes the function of each pin.

D_7-D_0 — Z80-CPU Data Bus (bidirectional, tristate)
This bus is used to transfer all data and commands between the Z80-CPU and the Z80-PIO. D_0 is the least significant bit of the bus.

B/A Sel — Port B or A Select (input, active high)
This pin defines which port will be accessed during a data transfer between the Z80-CPU and the Z80-PIO. A low level on this pin selects Port A while a high level selects Port B. Often Address bit A_0 from the CPU will be used for this selection function.

C/D Sel — Control or Data Select (input, active high)
This pin defines the type of data transfer to be performed bwtween the CPU and the PIO. A high level on this pin during a CPU write to the PIO causes the Z80 data bus to be interpreted as a command for the port selected by the B/A Select line. A low level on this pin means that the Z80 data bus is being used to transfer data between the CPU and the PIO. Often Address bit A_1 from the CPU will be used for this function.

$\overline{CE}$ — Chip Enable (input, active low)
A low level on this pin enables the PIO to accept command or data inputs from the CPU during a write cycle or to transmit data to the CPU during a read cycle. This signal is generally a decode of four I/O port numbers that encompass port A and B, data and control.

Φ — System Clock(input)
The Z80-PIO uses the standard Z80 system clock to synchronize certain signals internally. This is a single phase clock.

$\overline{M1}$ — Machine Cycle One Signal from CPU (input, active low)
This signal from the CPU is used as a sync pulse to control several internal PIO operations. When M1 is active and the RD signal is active, the Z80-CPU is fetching an instruction from memory. Conversely, when M1 is active and IORQ is active, the CPU is acknowledging an interrupt. In addition, the M1 signal has two other functions within the Z80-PIO.

1. M1 synchronizes the PIO interrupt logic.

2. When M1 occurs without an active RD or IORQ signal the PIO logic enters a reset state.

$\overline{IORQ}$ — Input/Output Request from Z80-CPU (input, active low)
The $\overline{IORQ}$ signal is used in conjunction with the B/A Select, C/D Select, $\overline{CE}$, and $\overline{RD}$ signals to transfer commands and data between the Z80-CPU and the Z80-PIO. When $\overline{CE}$, $\overline{RD}$ and $\overline{IORQ}$ are active, the port addressed by B/A will transfer data to the CPU (a read operation). Conversely, when $\overline{CE}$ and $\overline{IORQ}$ are active but $\overline{RD}$ is not active, then the port addressed by B/A will be written into from the CPU with either data or control information as specified by the C/D Select signal. Also, if $\overline{IORQ}$ and $\overline{M1}$ are active simultaneously, the CPU is acknowledging an interrupt and the interrupting port will automatically place its interrupt vector on the CPU data bus if it is the highest device requesting an interrupt.

B_0-B_7 — Port B Bus (bidirectional, tristate)
This 8 bit bus is used to transfer data and/or status or control information between Port B of the PIO and a peripheral device. The Port B data bus is capable of supplying 1.5ma@ 1.5V to drive Darlington transistors. B_0 is the least significant bit of the bus.

$\overline{B\ STB}$ — Port B Strobe Pulse from Peripheral Device (input, active low)
The meaning of this signal is similar to that of $\overline{A\ STB}$ with the following exception:
In the Port A bidirectional mode this signal strobes data from the peripheral device into the Port A input register.

B RDY — Register B Ready (output, active high)
The meaning of this signal is similar to that of A Ready with the following exception:
In the Port A bidirectional mode this signal is high when the Port A input register is empty and ready to accept data from the peripheral device.

$\overline{RD}$ — Read Cycle Status from the Z80-CPU (input, active low)
If $\overline{RD}$ is active a MEMORY READ or I/O READ operation is in progress. The $\overline{RD}$ signal is used with B/A Select, C/D Select, $\overline{CE}$ and $\overline{IORQ}$ signals to transfer data from the Z80-PIO to the Z80-CPU.

IEI — Interrupt Enable In (input, active high)
This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.

IEO — Interrupt Enable Out (output, active high)
The IEO signal is the other signal required to form a daisy chain priority scheme. It is high only if IEI is high and the CPU is not servicing an interrupt from this PIO. Thus this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its CPU interrupt service routine.

$\overline{INT}$ — Interrupt Request (output, open drain, active low)
When $\overline{INT}$ is active the Z80-PIO is requesting an interrupt from the Z80-CPU.

A_0-A_7 — Port A Bus (bidirectional, tri-state)
This 8 bit bus is used to transfer data and/or status or control information between Port A of the Z80-PIO and a peripheral device. A_0 is the least significant bit of the Port A data bus.

$\overline{A\ STB}$ — Port A Strobe Pulse from Peripheral Device (input, active low)
The meaning of this signal depends on the mode of operation selected for Port A as follows:

1) Output mode: The positive edge of this strobe is issued by the peripheral to acknowledge the receipt of data made available by the PIO.

2) Input mode: The strobe is issued by the peripheral to load data from the peripheral into the Port A input register. Data is loaded into the PIO when this signal is active.

3) Bidirectional mode: When this signal is active, data from the Port A output register is gated onto Port A bidirectional data bus. The positive edge of the strobe acknowledges the receipt of the data.

4) Control mode: The strobe is inhibited internally.

A RDY — Register A Ready (output, active high)
The meaning of this signal depends on the mode of operation selected for Port A as follows:

1) Output mode: This signal goes active to indicate that the Port A output register has been loaded and the peripheral data bus is stable and ready for transfer to the peripheral device.

2) Input mode: This signal is active when the Port A input register is empty and is ready to accept data from the peripheral device.

3) Bidirectional mode: This signal is active when data is available in Port A output register for transfer to the peripheral device. In this mode data is not placed on the Port A data bus unless $\overline{A\ STB}$ is active.

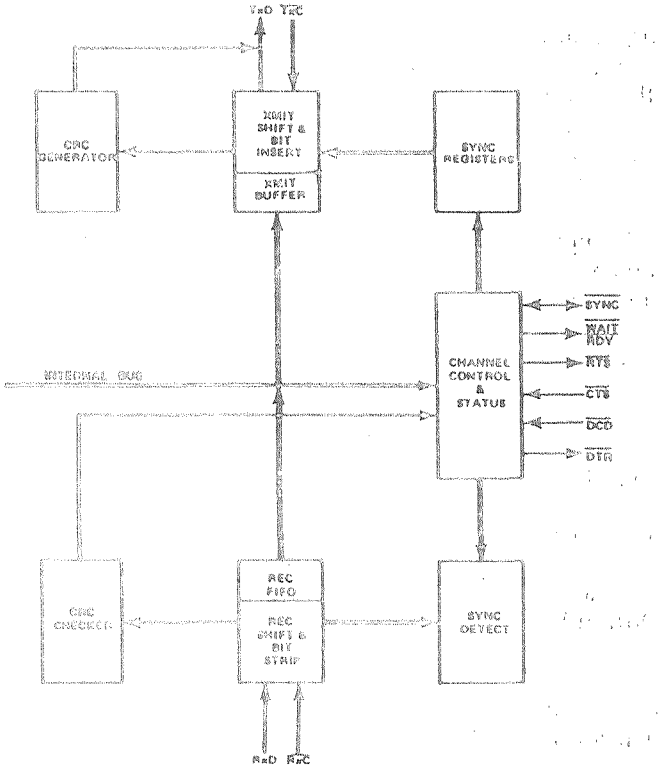
4) Control mode: This signal is disabled and forced to a low state.

2.0 SIO ARCHITECTURE

A block diagram of the SIO is shown in Figure 1. The internal structure includes a Z80-CPU bus interface, internal control and interrupt logic and two full duplex channels. The interrupt control logic determines which channel and which device within the channel is the highest priority for purposes of the automatic interrupt vectoring. Priority is fixed with Channel A assigned higher priority than Channel B and the Receiver, Transmitter and External/Status assigned priority in that order within each channel.

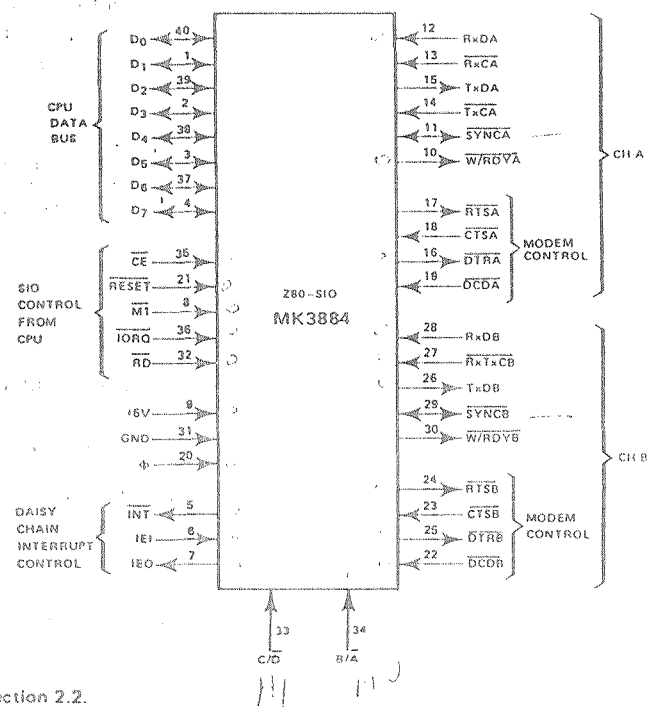
The channel logic is shown in block form in Figure 2. Each channel has five 8-bit control registers and three 8-bit status registers. The interrupt vector is written into an 8-bit register in Channel B and may also be read from that channel. The receiver has three 8-bit buffer registers in FIFO arrangement in addition to the 8-bit input shift register. The transmitter has one 8-bit buffer register in addition to the 8-bit output shift register. The CRC generator/checkers are 16-bit shift registers with appropriate internal feedback (programmable) for two different CRC codes.

CHANNEL BLOCK DIAGRAM *
Figure 2.0



*Configuration of Channel B will vary according to bonding option. See Section 2.2.

SIO PIN OUT
Figure 2.1



D_0-D_7	System Data Bus (bidirectional, tri-state)
B/$\overline{A}$	Channel B or A select (input high is Channel B)
C/$\overline{D}$	Control or Data select (input high is control)
$\overline{CE}$	Chip Enable (input, active low)
$\overline{M1}$	Machine Cycle One Signal from Z80-CPU (input, active low)
$\overline{IORQ}$	Input/Output request from Z80-CPU (input, active low)

$\overline{RD}$	Read Cycle Status from the Z80-CPU (input, active low)
Φ	System Clock (input)
$\overline{RESET}$	Reset (input, active low) disables both receivers and transmitters. T x DA and T X DB are forced marking. Modem controls are forced high. Control registers must be rewritten after SIO is reset and before any data is transmitted or received. All interrupts are disabled.
IEI	Interrupt Enable In (input, active high)
IEO	Interrupt Enable Out (output, active high) IEI and IEO form a daisy-chain connection for priority interrupt control.
$\overline{INT}$	Interrupt Request (output, open drain, active low).
$\overline{WAIT/READY\ A}$ $\overline{WAIT/READY\ B}$	Two pins, one for each channel. They may be programmed to serve as ready lines for use with a DMA Controller or they may serve as wait lines to synchronize the Z80-CPU to the SIO data rate.
$\overline{CTSA}$, $\overline{CTSB}$	Clear to Send (2 pins, inputs, active low). When programmed as AUTO ENABLES, these inputs enable the transmitters of their respective channels. If these pins are not programmed as transmitter enables, they may be programmed as general-purpose input pins. These inputs are Schmitt-trigger buffered to allow slow-rise time inputs.
$\overline{DCDA}$, $\overline{DCDB}$	Data Carrier Detect (2 pins, inputs, active low.) These pins are similar to the $\overline{CTS}$ inputs, except that they are usable as receiver enables rather than transmitter enables.
RxDA, RxDB	Receive Data, (2 pins, inputs, active high.)
TxDA, TxDB	Transmit Data. (2 pins, outputs, active high.)
$\overline{RxCA}$, $\overline{RxCB}$	Receiver clocks (inputs, active low.) (Two pads, one per channel. See note on Bonding Option.) Schmitt-trigger buffered.
$\overline{TxCA}$, $\overline{TxCB}$	Transmitter Clocks (inputs, active low.) (Two pads, one per channel. See note on Bonding Option.) Schmitt-trigger buffered.
$\overline{RTSA}$, $\overline{RTSB}$	Request to Send (2 pins, outputs, active low.) When the RTS bit is set, the $\overline{RTS}$ pin goes low. When the bit is reset in asynchronous mode, the pin goes high, but only after the transmitter is empty. In synchronous modes, $\overline{RTS}$ is a simple output which strictly follows the state of the $\overline{RTS}$ bit.
$\overline{DTRA}$, $\overline{DTRB}$	Data Terminal Ready (2 pins, output, active low.) Pin follows state programmed with DTR bit. (Two pads, one per channel. See note on Bonding Option.)

$\overline{SYNCA}$, $\overline{SYNCB}$ — External Character Synchronization (2 pins, input/output, active low.) If the External Synchronization mode is selected, assembly of characters will begin on the next rising edge of $\overline{R \times C}$. If internal character sync modes are selected, the pins are outputs that are active during part of the clock cycles that a sync character is recognized. The sync condition is not latched, so this pin will be active every time a sync pattern is recognized, regardless of character boundaries. In asynchronous modes, these pins are simple inputs to the HUNT/SYNC bits in Status Register 0 and may be used for any input function desired. However, if EXTERNAL/STATUS interrupts are enabled in the asynchronus mode, then SYNC should not be left floating as this could cause spurious interrupts to occur.

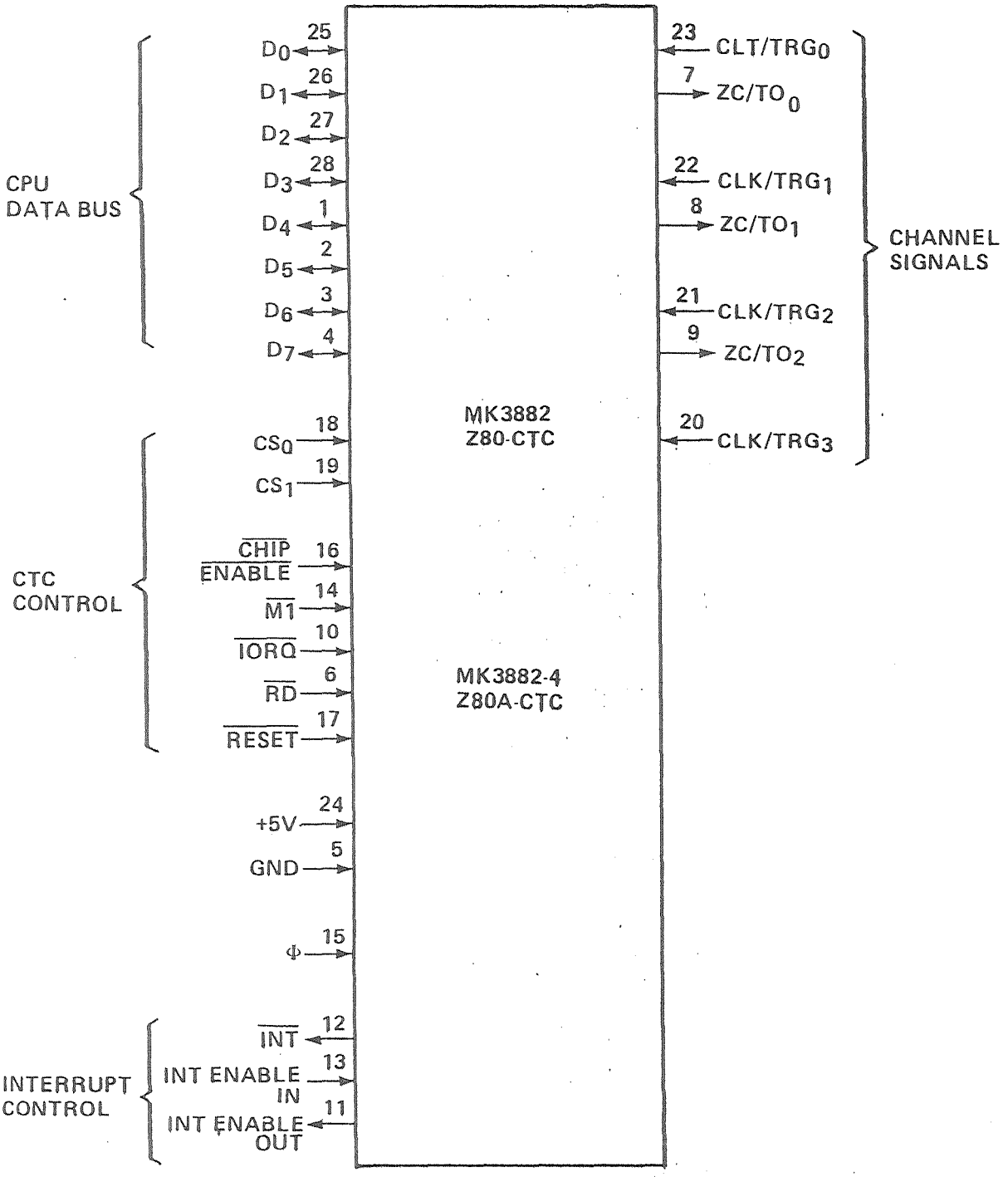
NOTE: When used as an external synchronization pin, it must not become active for three system clock cycles after the previous rising edge of $\overline{R \times C}$. This requirement normally can be met by allowing $\overline{SYNC}$ to change only on the falling edge of $\overline{R \times C}$.

2.2 NOTE ON BONDING OPTION:

Due to package constraints, there are only five pins available for seven signals: $\overline{DTRB}$, $T \times DB$, $\overline{R \times T \times CB}$, $R \times DB$, $\overline{SYNCB}$, $\overline{T \times CB}$ and $\overline{R \times CB}$. Figure 2.2 outlines the pin out of all three SIO options. These options are designated by three different part numbers, the MK3884, MK3885 and MK3887. Since the parts differ by only the bonding option, all three parts are offered in the same packaging, frequency and temperature ranges.

SIO PIN	MK3884	MK3885	MK3887
25	$\overline{DTRB}$	$T \times DB$	$\overline{DTRB}$
26	$T \times DB$	$\overline{T \times CB}$	$T \times DB$
27	$\overline{R \times T \times CB}$	$\overline{R \times CB}$	$\overline{T \times CB}$
28	$R \times DB$	$R \times DB$	$\overline{R \times CB}$
29	$\overline{SYNCB}$	$\overline{SYNCB}$	$R \times DB$

Z80-CTC PIN CONFIGURATION
Figure 3.0-1



3.0 CTC PIN DESCRIPTION

A diagram of the Z80-CTC pin configuration is shown in Figure 3.0-1. This section describes the function of each pin.

D7 - D0
Z80-CPU Data Bus (bi-directional, tri-state)

This bus is used to transfer all data and command words between the Z80-CPU and the Z80-CTC. There are 8 bits on this bus, of which D0 is the least significant.

CS1 - CS0
Channel Select (input, active high)

These pins form a 2-bit binary address code for selecting one of the four independent CTC channels for an I/O Write or Read (See truth table below.)

	CS1	CS0
Ch0	0	0
Ch1	0	1
Ch2	1	0
Ch3	1	1

$\overline{CE}$
Chip Enable (input, active low)

A low level on this pin enables the CTC to accept control words, Interrupt Vectors, or time constant data words from the Z80 Data Bus during an I/O Write cycle, or to transmit the contents of the Down Counter to the CPU during an I/O Read cycle. In most applications this signal is decoded from the 8 least significant bits of the address bus for any of the four I/O port addresses that are mapped to the four Counter/Timer Channels.

Clock (Φ)
System Clock (input)

This single-phase clock is used by the CTC to synchronize certain signals internally.

$\overline{M1}$
Machine Cycle One Signal from CPU (input, active low)

When $\overline{M1}$ is active and the $\overline{RD}$ signal is active, the CPU is fetching an instruction from memory. When $\overline{M1}$ is active and the $\overline{IORQ}$ signal is active, the CPU is acknowledging an interrupt, alerting the CTC to place an Interrupt Vector on the Z80 Data Bus if it has daisy chain priority and one of its channels has requested an interrupt.

$\overline{IORQ}$
Input/Output Request from CPU (input, active low)

The $\overline{IORQ}$ signal is used in conjunction with the $\overline{CE}$ and $\overline{RD}$ signals to transfer data and Channel Control Words between the Z80-CPU and the CTC. During a CTC Write Cycle, $\overline{IORQ}$ and $\overline{CE}$ must be true and $\overline{RD}$ false. The CTC does not receive a specific write signal, instead generating its own internally from the inverse of a valid $\overline{RD}$ signal. In a CTC Read Cycle, $\overline{IORQ}$, $\overline{CE}$ and $\overline{RD}$ must be active to place the contents of the Down Counter on the Z80 Data Bus. If $\overline{IORQ}$ and $\overline{M1}$ are both true, the CPU is acknowledging an interrupt request, and the highest-priority interrupting channel will place its Interrupt Vector on the Z80 Data Bus.

3.0 CTC PIN DESCRIPTION (CONT'D)

$\overline{RD}$

Read Cycle Status from the CPU (input, active low)

The $\overline{RD}$ signal is used in conjunction with the $\overline{IORQ}$ and $\overline{CE}$ signals to transfer data and Channel Contr Words between the Z80-CPU and the CTC. During a CTC Write Cycle, $\overline{IORQ}$ and $\overline{CE}$ must be true a $\overline{RD}$ false. The CTC does not receive a specific write signal, instead generating its own internally from t inverse of a valid $\overline{RD}$ signal. In a CTC Read Cycle, $\overline{IORQ}$, $\overline{CE}$ and $\overline{RD}$ must be active to place the conter of the Down Counter on the Z80 Data Bus.

IEI

Interrupt Enable In (input, active high)

This signal is used to help form a system-wide interrupt daisy chain which establishes priorities when mo than one peripheral device in the system has interrupting capability. A high level on this pin indicates th no other interrupting devices of higher priority in the daisy chain are being serviced by the Z80-CPU.

IEO

Interrupt Enable Out (output, active high)

The IEO signal, in conjunction with IEI, is used to form a system-wide interrupt priority daisy chain. IE(is high only if IEI is high and the CPU is not servicing an interrupt from any CTC channel. Thus this sig nal blocks lower priority devices from interrupting while a higher priority interrupting device is beir serviced by the CPU.

$\overline{INT}$

Interrupt Request (output, open drain, active low)

This signal goes true when any CTC channel which has been programmed to enable interrupts has a zer count condition in its Down Counter.

$\overline{RESET}$

Reset (input, active low)

This signal stops all channels from counting and resets channel interrupt enable bits in all control register thereby disabling CTC-generated interrupts. The ZC/TO and $\overline{INT}$ outputs go to their inactive states, IE(reflects IEI, and the CTC's data bus output drivers go to the high impedance state.

CLK/TRG3–CLK/TRG0

External Clock/Timer Trigger (input, user-selectable active high or low)

There are four CLK/TRG pins, corresponding to the four independent CTC channels. In the Counte Mode, every active edge on this pin decrements the Down Counter. In the Timer Mode, an active edge o this pin initiates the timing function. The user may select the active edge to be either rising or falling.

ZC/TO2–ZC/TO0

Zero Count/Timeout (output, active high)

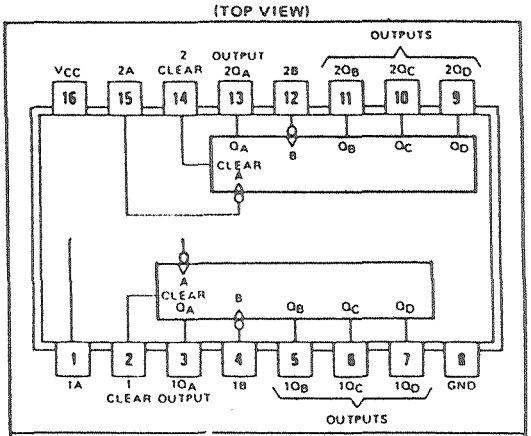
There are three ZC/TO pins, corresponding to CTC channels 2 through 0. (Due to package pin limita tions channel 3 has no ZC/TO pin.) In either Counter Mode or Timer Mode, when the Down Counte decrements to zero an active high going pulse appears at this pin.

TYPES SN54390, SN54LS390, SN54393, SN54LS393, SN74390, SN74LS390, SN74393, SN74LS393
DUAL 4-BIT DECADE AND BINARY COUNTERS

BULLETIN NO. DL-S 7612099, OCTOBER 1976

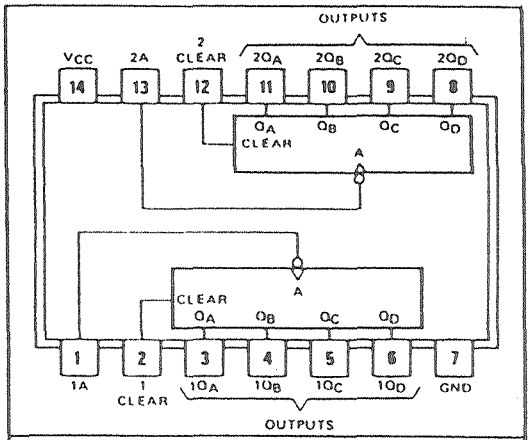
- Dual Versions of the Popular '90A, 'LS90 and '93A, 'LS93
- '390, 'LS390. . .Individual Clocks for A and B Flip-Flops Provide Dual ÷2 and ÷5 Counters
- '393, 'LS393. . .Dual 4-Bit Binary Counter with Individual Clocks
- All Have Direct Clear for Each 4-Bit Counter
- Dual 4-Bit Versions Can Significantly Improve System Densities by Reducing Counter Package Count by 50%
- Typical Maximum Count Frequency . . . 35 MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

SN54390, SN54LS390 . . . J OR W PACKAGE
SN74390, SN74LS390 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: ...gh input to clear resets all four outputs low

SN54393, SN54LS393 . . . J OR W PACKAGE
SN74393, SN54LS393 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: High input to clear resets all four outputs low

description

Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The '390 and 'LS390 incorporate dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The '393 and 'LS393 each comprise two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The '390, 'LS390, '393, and 'LS393 have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

Series 54 and Series 54LS circuits are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 and Series 74LS circuits are characterized for operation from 0°C to 70°C.

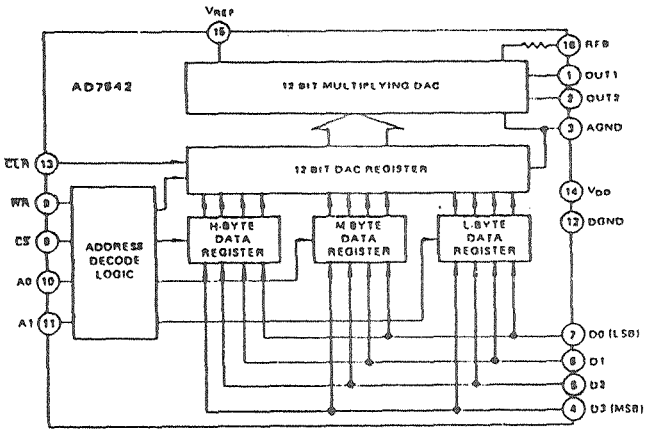
CMOS µP-Compatible 12-Bit DAC

AD7542

FEATURES

Resolution: 12 Bits
Nonlinearity: ±1/2LSB T_{min} to T_{max}
Low Gain Drift: 2ppm/°C typ, 5ppm/°C max
Microprocessor Compatible
Full 4-Quadrant Multiplication
Low Multiplying Feedthrough
Low Power Dissipation: 40mW max
Low Cost
Small Size: 16-Pin DIP
Latch Free (Protection Schottky Not Required)

AD7542 FUNCTIONAL BLOCK DIAGRAM



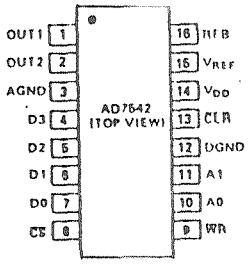
GENERAL DESCRIPTION

The AD7542 is a precision 12-bit CMOS multiplying DAC designed for direct interface to 4- or 8-bit microprocessors.

The functional diagram shows the AD7542 to consist of three 4-bit data registers, a 12-bit DAC register, address decoding logic and a 12-bit CMOS multiplying DAC. Data is loaded into the data registers in three 4-bit bytes, and subsequently transferred to the 12-bit DAC register. All data loading or data transfer operations are identical to the WRITE cycle of a static RAM. A clear input allows the DAC register to be easily reset to all zeros when powering up the device.

The AD7542 is manufactured using an advanced thin film on monolithic CMOS fabrication process. Multiplying capability, low power dissipation, +5V operation, small size (16-pin DIP) and easy µP interface make the AD7542 ideal for many instrumentation, industrial control and avionics applications.

PIN CONFIGURATION (NOT TO SCALE)



ORDERING INFORMATION

Relative Accuracy (T_{min} to T_{max})	Gain Error +25°C	Temperature Range and Package[1] Commercial (Plastic) 0 to +70°C	Industrial (Ceramic) -25°C to +85°C	Extended (Ceramic) -55°C to +125°C
±1LSB	±2 3LSB	AD7542JN	AD7542AD	AD7542SD
±1/2LSB	±2 3LSB	AD7542KN	AD7542BD	AD7542TD
±1/2LSB	±1LSB	AD7542GKN	AD7542GBD	AD7542GTD

[1] Analog Devices is offering the AD7542 in chip carriers. For information contact the factory.

PACKAGE IDENTIFICATION[1]

Suffix "N" = Plastic DIP (N16B)
Suffix "D" = Ceramic DIP (D16B)

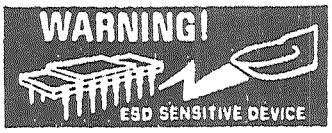
[1] See Section 19 for package outline information.

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

V_{DD} to AGND . . . . . 0V, +7V
V_{DD} to DGND . . . . . 0V, +7V
AGND to DGND . . . . . V_{DD}
DGND to AGND . . . . . V_{DD}
Digital Input Voltage to DGND
(pins 4–11, 13) . . . . . –0.3V, +15.3V
V_{PIN1}, V_{PIN2} to AGND . . . . . –0.3V, +15V
V_{REF} to AGND . . . . . ±25V
V_{RFB} to AGND . . . . . ±25V
Power Dissipation (Package)
Plastic (Suffix N)
To +70°C 670mW
Derates above +70°C by . . . . . 8.3mW/°C
Ceramic (Suffix D)
To +75°C 450mW
Derates above +75°C by . . . . . 6mW/°C
Operating Temperature Range
Commercial Plastic (JN, KN, GKN versions) . . . 0 to +70°C
Industrial Ceramic (AD, BD, GBD versions)
. . . . . –25°C to +85°C
Extended Ceramic (SD, TD, GTD versions) . –55°C to +125°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



9

TERMINOLOGY

RELATIVE ACCURACY
Relative accuracy on endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in % or ppm of full scale range or (sub) multiples of 1LSB.

DIFFERENTIAL NONLINEARITY
Differential nonlinearity is the difference between the *measured* change and the *ideal* 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range insures monotonicity.

GAIN ERROR
Gain is defined as the ratio of the DAC's Full Scale output to its reference input voltage. An *ideal* AD7542 would exhibit a gain of –4095/4096. Gain error is adjustable using external trims as shown in Figures 5 and 6.

OUTPUT LEAKAGE CURRENT
Current which appears at OUT1 with the DAC register loaded to all 0s or at OUT2 with the DAC register loaded to all 1s.

MULTIPLYING FEEDTHROUGH ERROR
AC error due to capacitive feedthrough from V_{REF} terminal to OUT1 with DAC register loaded to all 0s.

PIN	MNEMONIC	FUNCTION	PIN	MNEMONIC	FUNCTION
1	OUT1	DAC current output bus. Normally terminated at op amp virtual ground	7	D0	Data Input (LSB)
			8	$\overline{CS}$	Chip Select Input
			9	$\overline{WR}$	WRITE Input
2	OUT2	DAC current output bus. Normally terminated at ground	10	A0	Address Bus Input
			11	A1	Address Bus Input
3	AGND	Analog Ground	12	DGND	Digital Ground
4	D3	Data Input (MSB)	13	$\overline{CLR}$	Clear Input
5	D2	Data Input	14	V_{DD}	+5V Supply Input
6	D1	Data Input	15	V_{REF}	Reference Input
			16	R_{FB}	DAC Feedback Resistor

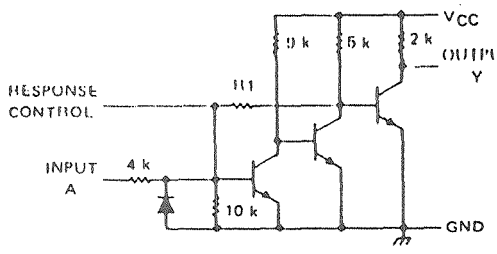
Table I. Pin Function Description

TYPES SN75189, SN75189A QUADRUPLE LINE RECEIVERS

BULLETIN NO. DL S 7312035, SEPTEMBER 1973

- Input Resistance . . . 3 kΩ to 7 kΩ
- Input Signal Range . . . ±30 V
- Fully Interchangeable with Mototola MC1489, MC1489A
- Operates From Single 5-V Supply
- Built-in Input Hysteresis (Double Thresholds)
- Response Control Provides:
  Input Threshold Shifting
  Input Noise Filtering
- Satisfies Requirements of EIA RS-232-C

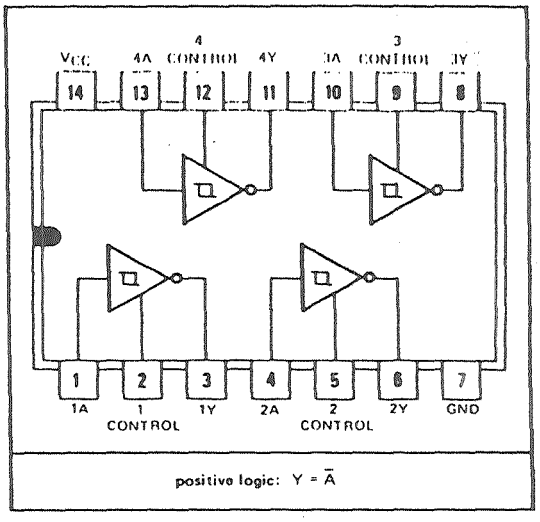
schematic (each receiver)



	SN75189	SN75189A
R1	10 k	2 k

Resistor values shown are nominal and in ohms.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



5

description

The SN75189 and SN75189A are monolithic quadruple line receivers designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. A separate response control terminal is provided for each receiver. A resistor or a resistor and bias voltage can be connected between this terminal and ground to shift the input threshold voltage levels. An external capacitor can be connected from this terminal to ground to provide input noise filtering.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	10 V
Input voltage	±30 V
Output current	20 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1 W
Operating free-air temperature range	0°C to 75°C
Storage temperature range	−65°C to 175°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

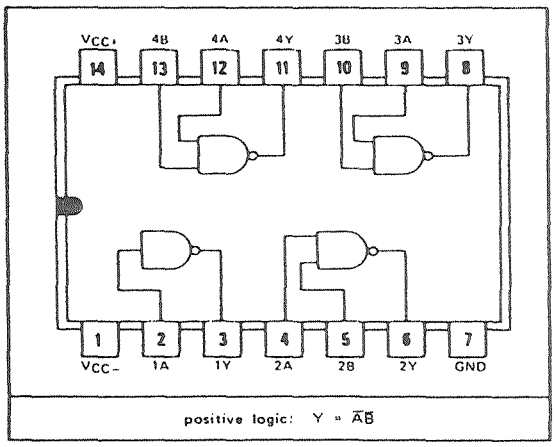
NOTES: 1. Voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the J package, SN75189 and SN75189A chips are glass-mounted.

TYPE SN75188
QUADRUPLE LINE DRIVER

BULLETIN NO. DL-S 7711874, SEPTEMBER 1973 REVISED JANUARY 1977

- Meets Specifications of EIA RS-232C
- Designed to be Interchangeable with Motorola MC1488
- Current-Limited Output . . . 10 mA Typical
- Power-Off Output Impedance . . . 300 Ω Min
- Slew Rate Control by Load Capacitor
- Flexible Supply Voltage Range
- Input Compatible with Most TTL and DTL Circuits

J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{AB}$

description

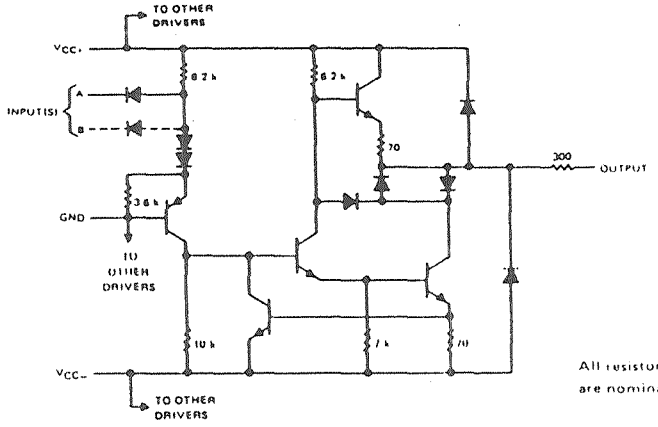
The SN75188 is a monolithic quadruple line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard RS-232C with a diode in series with each supply-voltage terminal as shown under typical applications. The device is characterized for operation from 0°C to 75°C.

FUNCTION TABLE

A	B	Y
H	H	L
L	X	H
X	L	H

H = high level, L = low level,
X = irrelevant

schematic (each driver)



All resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} at (or below) 25°C free-air temperature (see Notes 1 and 2)	15 V
Supply voltage V_{CC-} at (or below) 25°C free-air temperature (see Notes 1 and 2)	−15 V
Input voltage range	−15 V to 7 V
Output voltage range	−15 V to 15 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1 W
Operating free-air temperature range	0°C to 75°C
Storage temperature range	65°C to 175°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, refer to the Maximum Supply Voltage Curve, Figure 6, and the Dissipation Derating Curves in the Thermal Information Section, which begins on page 21. In the J package, SN75188 chips are glass-mounted.

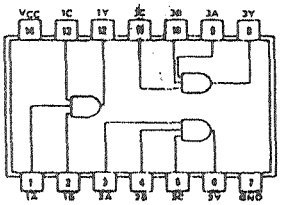
PIN ASSIGNMENTS (TOP VIEWS)

TRIPLE 3-INPUT
POSITIVE-AND GATES

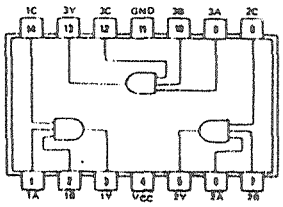
11

positive logic:
$Y = ABC$

See page 6-10



SN54H11 (J) SN74H11 (J, N)
SN54LS11 (J, W) SN74LS11 (J, N)
SN54S11 (J, W) SN74S11 (J, N)



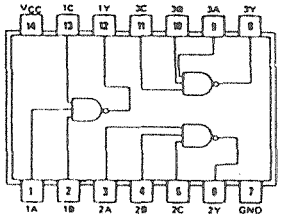
SN54H11 (W)

TRIPLE 3-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

12

positive logic:
$Y = \overline{ABC}$

See page 6-4



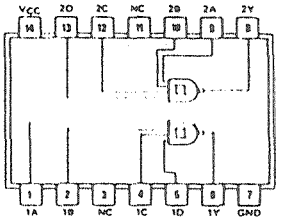
SN5412 (J, W) SN7412 (J, N)
SN54LS12 (J, W) SN74LS12 (J, N)

DUAL 4-INPUT
POSITIVE-NAND
SCHMITT TRIGGERS

13

positive logic:
$Y = \overline{ABCD}$

See page 6-14



SN5413 (J, W) SN7413 (J, N)
SN54LS13 (J, W) SN74LS13 (J, N)

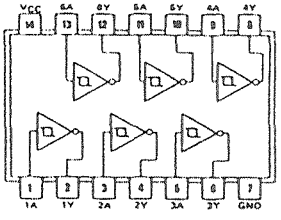
NC—No internal connection

HEX SCHMITT-TRIGGER
INVERTERS

14

positive logic:
$Y = \overline{A}$

See page 6-14

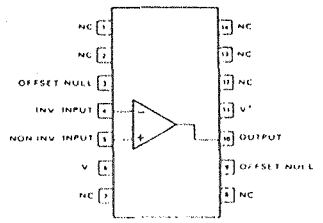


SN5414 (J, W) SN7414 (J, N)
SN54LS14 (J, W) SN74LS14 (J, N)

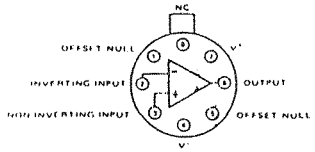
μA741-T • μA741C-A,T,V

PIN CONFIGURATION

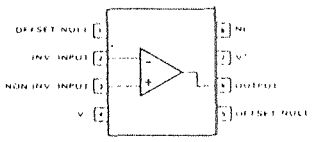
A PACKAGE



T PACKAGE



V PACKAGE



FEATURES

- INTERNAL FREQUENCY COMPENSATION
- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- EXCELLENT TEMPERATURE STABILITY
- HIGH INPUT VOLTAGE RANGE
- NO LATCH-UP

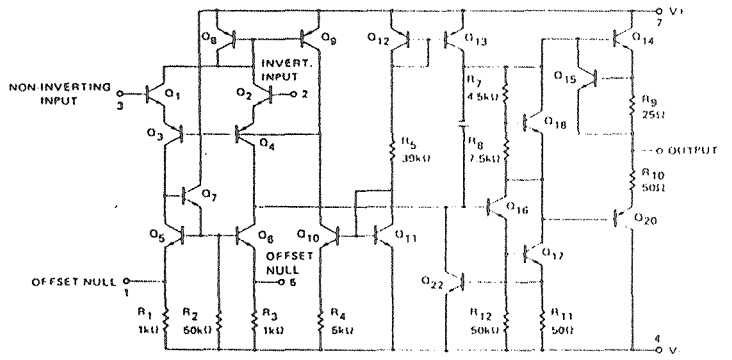
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	μA741C	±18V
	μA741	±22V
Internal Power Dissipation (Note 1)		500mW
Differential Input Voltage		±30V
Input Voltage (Note 2)		±15V
Voltage between Offset Null and V—		±0.5V
Operating Temperature Range		
	μA741C	0°C to +70°C
	μA741	−55°C to +125°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Solder, 60 sec.)		300°C
Output Short Circuit Duration (Note 3)		Indefinite

NOTES:

1. Rating applies for case temperatures to 125°C; derate linearly at 6.5mW/°C for ambient temperatures above 175°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions	LIMITS Typ	Units
Input Capacitance		1.4	pF
Offset Voltage Adjustment Range		±15	mV
Output Resistance		75	
Transient Response	V_{IN} = 20mV, R_L = 2KΩ, $C_L \leq 100pF$		
Rise Time		0.3	μs
Overshoot		5.0	%
Slew Rate	$R_L \geq 2K\Omega$	0.5	V/μs