Structural and Functional Characterizations of Al^+ Implanted 4H-SiC Layers and Al^+ Implanted 4H-SiC *p-n* Junctions after 1950°C Post Implantation Annealing

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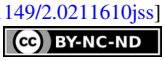
In the case of Al^+ implanted 4H-SiC, a post implantation annealing temperature of 1950°C has the beneficial effect of maximizing both the electrical activation of implanted Al and the reordering of the lattice damaged by the Al ions. However, the formation of extended defects in the implanted layers and that of carbon vacancies in the n-type epi-layers below the implanted layers may be hardly avoided. This study contains the results of structural and electrical investigation showing that: *(i)* on increasing the implanted Al concentration different type of extended defects form and grow; *(ii)* a strong anisotropic hole transport occurs when the Al implanted surface layer is confined by and contains stacking faults. This study also reports experimental and simulated values of the area and the perimeter components of the current density of Al^+ implanted 4H-SiC p-i-n diodes. The simulations show that these components may be, at least qualitatively, accounted for by the sole hypothesis of carrier lifetime dominated by carbon-vacancy related traps and by the presence of a negative fixed charge at the sample surface.



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The selected area doping by ion implantation is a largely used technology for the fabrication of SiC electronic devices. Such technology requires a mandatory post implantation annealing for the electrical activation of the implanted dopants and the reordering of the SiC crystalline lattice damaged by the ion bombardment. The higher the temperature of this annealing the more effective are both these phenomena.[1–4] While the industry has the understandable need to limit the thermal budget for device fabrication, the academy is exploring extremely high annealing temperatures because this is needed to understand all the phenomena related to the heating of both implanted and unimplanted regions of a SiC crystal.[5–7]

4H-SiC is the SiC poly-type more used for power electronic devices. Aluminum (Al) is the preferred acceptor dopant of 4H-SiC when very high acceptor concentrations are needed. The fact that the 4H-SiC epi-wafers are mostly of n-type conductivity, imposes the use of p-type emitters to obtain p-i-n vertical power diodes. Such emitters are generally homo-epitaxial Al doped materials, mesa etched, with junction terminations obtained by Al ion implantation.

Among all the implanted dopants in 4H-SiC, Al is the one for which the increase of the post implantation temperature up to 2000°C has given the most beneficial effects for what concerns the p-type conductivity values. After these annealing treatments, hole mobility values in Al implanted layers are very similar to those found in Al doped epitaxial materials in spite of the fact that the implanted materials have a higher density of structural defects. In fact, it is known that during annealing extended defects form and grow in the implanted regions. How these defects may affect the carrier transport is still an open issue. In this study, the presence of different defect structures for implanted Al concentration below and far above the Al solid solubility in 4H-SiC at 1950°C is reported. Moreover, a peculiar anisotropic carrier transport in the heaviest doped sample has been found.

The saturation density of carbon-vacancy V_C in unimplanted n-type 4H-SiC epi-materials has been seen to increase of orders of magnitudes after thermal treatments performed at temperature going from 1500°C to 1950°C.[8] In 4H-SiC substrates below an implanted layer, a competitive mechanism between V_C formation and V_C annihilation has been observed.[9] The former mechanism being driven by the very high post implantation annealing temperature, while the latter by a C interstitial injection from the implanted regions. These results and the knowledge that the V_C related traps are carrier lifetime killer defects, have led us to study how the sole hypothesis of a carrier lifetime dominated by V_C related traps may account for the simulation of the current-voltage curves of Al implanted bipolar 4H-SiC diodes.

Experimental

Semi-Insulating High Purity (HPSI) 4H-SiC 8°-off axis ⟨0001⟩ has been implanted at 400°C with Al^+ ions of various energy and doses so to obtain almost box shaped depth profiles with heights in the range 1×10^{19}–5×10^{20} cm^{-3} and thickness of about 400 nm. The as implanted samples were diced in 5×5 mm^2 pieces. The implanted surface of each piece was protected by a pyrolyzed resist film (C-cap) before to perform a 1950°/5min thermal treatment in high purity Ar ambient. After that, C-cap was removed by a 850°C/15min dry oxidation. Triangular Ti/Al ohmic contacts were fabricated on the corners of the square samples to obtain a van der Pauw (vdP) device geometry for electrical characterization. The temperature dependence of the sheet resistance was measured in the range 20–680 K. Keithely current source and voltage source meters have been used for electrical measurements. Samples have been cooled below room temperature (RT) in a closed-cycle He-cooled cryostat, and heated above RT by a MMR heated sample holder. The lattice structure of the implanted and annealed layers has been investigated by Transmission Electron Microscopy (TEM) using a FEI Tecnai F20 ST transmission electron microscope operating at 200 kV. The samples for TEM were cross-sections cut parallel to the plane (10–10).

A piece of a n-type epitaxial 4H-SiC ⟨0001⟩ 8° off-axis wafer has been used to fabricate vertical p-i-n diodes with 2×10^{20} cm^{-3} Al^+ implanted emitters and different diameters in the range 150 – 1000 μm by selected area ion implantation. The n^- epi-layer was 25 μm thick with 3×10^{15} cm^{-3} net donor density. These diodes received the same post implantation annealing with C-cap than the above HPSI samples. After annealing, 1000°C/2min alloyed Ti/Al and Ni ohmic contacts have been fabricated on anode and cathode, respectively. The surface

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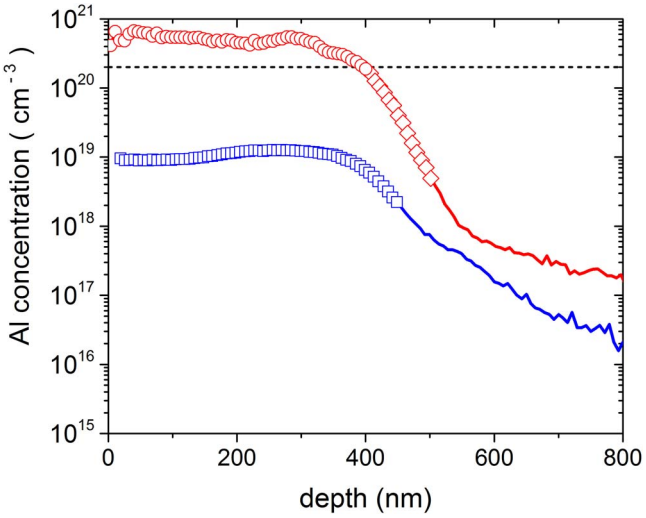

Figure 1. SIMS Al depth profiles of the samples with plateau Al concentration values of: (□, –) 1×10^{19} cm^{-3} and (○,◇,–) 5×10^{20} cm^{-3}. Symbols indicate the regions where extended defects are observed in the WB-TEM micrographs reported in Figs. 2a and 2b obtained on the same specimens. Open squares and diamond (□,◇) indicate the presence of *D* defects whereas open circles (○) that of basal plane stacking faults (see text). The horizontal dashed line is the solubility of Al in 4H-SiC at 1950°C, i. e. 2×10^{20} cm^{-3}.[17]

of these diodes is not passivated, thus only native oxide is present at the diode periphery. Static forward current-voltage characteristics at room temperature have been measured by an instrumental setup with a 1×10^{-14} A current floor, 30 meV step voltage and 4 s delay time after polarization and before current reading were used. By the procedure described in Ref. 10 the curves of the area and perimeter current densities versus voltage have been obtained. It is worthwhile to underline the fact that these curves are specific of the diode family and depend only on the processing history of the devices as shown in previous studies.[11–13]

The simulations of the curves of forward area and perimeter current densities versus voltage have been performed in the Synopsys-Sentaurus TCAD suite. These simulations are based on the solution of the stationary drift-diffusion equations. Specific models for SiC take into account the incomplete ionization of dopants and the band-gap narrowing versus carrier density.[14] General models for Auger[15] and Shockley-Read-Hall recombination are also taken into account. The carrier mobility in SiC is modelled by using the empirical relation of Caughey-Thomas with the fitting parameters of SiC taken from Ref. 16. The carrier lifetime is assumed to be controlled only by traps related to the carbon vacancies in 4H-SiC. The role of the surface is assumed controlled by a fixed charge trapped in the native oxide.

The Al depth profiles of all the samples used in this study have been measured by Secondary Ion Mass Spectrometry (SIMS) performed in a Cameca IMS-4f spectrometer with an 8 keV O_2^+ primary ion beam.

Results and Discussion

Structural characterizations.—Figure 1 shows the Al depth profiles for the samples with the lowest and highest plateau of implanted Al concentration as measured by SIMS. In Figs. 2a and 2b corresponding cross-sectional [10–10] weak beam (WB) micrographs of the same samples are reported, respectively.

In Fig. 1, symbols indicate in both the SIMS profiles, the regions where extended defects are observed in the corresponding WB-TEM micrographs reported in Figs. 2a and 2b. In Fig. 1 the value 2×10^{20} cm^{-3} of the Al solid solubility in 4H-SiC at 1950°C[17] is also shown for comparison purpose.

In Fig. 2a, small loops are uniquely visible. These loops form a network of almost orthogonal traces that in the [10–10] projection correspond to the {−12-13} and/or {−24-23} planes. In Fig. 2b several types of defects are visible. These defects have been labeled with letters from *A* to *D*. *A* and *B* defects are polygonal loops differing in size, *A* defects being the smallest. In the case of *B* defects, it has been possible to demonstrate that they have a complex structure related to Al precipitates and vacancy agglomerates.[18] *C* defects are stacking faults lying on the (0001) basal plane of the 4H-SiC lattice. The distribution of these defects is not uniform and appears to peak in a buried region close to the end of the Al implanted plateau. A last type of defect has been labelled *D*; *D* defects are confined into a layer between the implanted Al plateau and the unimplanted substrate. The WB images of the *D* defects in Fig. 2b and of those in Fig. 2a show, in both the cases, that these defects share the same habit planes. For this reason from hereafter the term "*D* defects" will be used also for the defects of Fig. 2a.

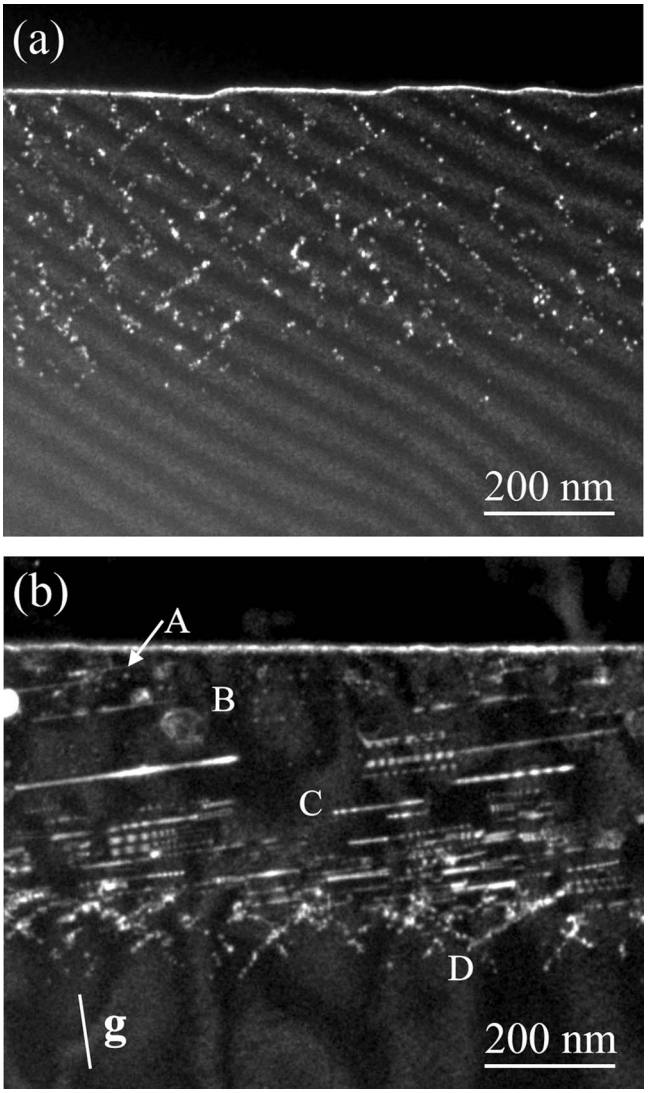

Figure 2. (a,b). [10–10] cross-sectional WB (-g,4g) g = [0004] micrograph of the near surface regions of: (a) 1×10^{19} cm^{-3} and (b) 5×10^{20} cm^{-3} Al implanted HPSI 4H-SiC specimens, after 1950°C/5min annealing. In (b) *A*, *B*, *C* and *D* mark different defect structures (see the text). Defects of type *C* lay on the (0001) basal plane at 8.1° from the wafer surface.

The comparison of the defect type and defect depth distribution in Figs. 2a and 2b with the SIMS Al depth profiles in Fig. 1 shows that: *(i)* no extended defects are observed for implanted Al concentration below 2×10^{18} cm^{-3} (see profiles portions marked with continuous lines in Fig. 1); *(ii)* *D* defects are observed in both the SIMS profiles reported in Fig. 1, starting from similar values of the implanted Al

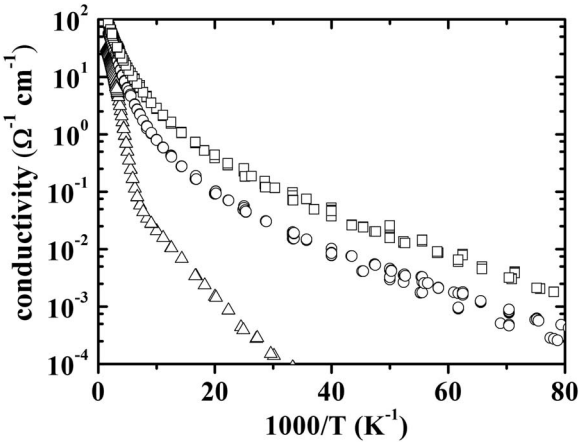

Figure 3. Temperature dependence of the conductivity of the HPSI 4H-SiC implanted with (△) 1×10^{20} cm^{-3}, (○) 3×10^{20} cm^{-3}, and (□) 5×10^{20} cm^{-3} Al concentrations after 1950°C/5min annealing.

concentrations e.g. around 2–3 $\times$ 10^{18} cm^{-3}; *(iii)* Al precipitates are observed in the surface implanted layer with Al density above the Al solubility limit of 2 $\times$ 10^{20} cm^{-3} in 4H-SiC at 1950°C; *(iv) C* defects are also found for implanted Al concentrations above a value close to the Al solubility limit. However, concerning the last point, it has been demonstrated by Energy Dispersive X-ray Spectroscopy (EDS) characterizations that *C* defects are not directly related to Al segregation or precipitation phenomena.[18,19] The observation that *C* defects are not Al-rich defects and, as above described, that their density peaks in an interface region between the Al rich plateau and the unimplanted substrate suggests that their presence may contribute to release the lattice strain present in the 4H-SiC doped surface layer. Other authors have shown that extra planes formed after the implantation and annealing process may be responsible for a c-lattice expansion observed in doped 4H-SiC epi-layers irrespective of the implanted ion species.[20] Finally, a comparison of Figs. 2a and 2b shows that: *(v) D* defects are no more observed where *C* defects are present suggesting that the *C* defects formation is also somewhat related to their coalescence. Further work is needed to clarify origin and role of the SFs presence.

Electrical characterization.—Figure 3 shows, in a *Log-linear* plot, the temperature dependence of the conductivity of the 1 $\times$ 10^{20} – 3 $\times$ 10^{20} – 5 $\times$ 10^{20} cm^{-3} Al implanted HPSI 4H-SiC specimens after 1950°C/5min annealing. Conductivity has been obtained as the reciprocal of the product between the measured sheet resistance and the FWHM thickness of the implanted layer measured by SIMS. The curve of the 1 $\times$ 10^{20} cm^{-3} sample may be described as formed by two linear traits with different thermal activation energies, about 20 meV and 100 meV at low and high temperatures, respectively. The study of these regions in the frame of the Miller and Abrahams model[21] has allowed us to ascribe the 20 meV energy to a hole transport into an impurity band by hopping between nearest neighbors (NNH), while the 100 meV to a hole transport in the valence band extended states with carrier freeze-out into the Al acceptors.[22] In Fig. 3, the curves of the 3 $\times$ 10^{20} cm^{-3} and 5 $\times$ 10^{20} cm^{-3} samples deviate from the this simple behavior. These curves show higher conductivity values than the curve of the 1 $\times$ 10^{20} cm^{-3} sample, suggesting correspondingly higher acceptor densities. As with the increase of the acceptor density the mechanism of transport in the impurity band may evolve from NNH to variable range hopping (VRH), this latter modeled by Mott,[23] the conductivity curves of Fig. 3 have been studied in the light of the following conductivity temperature dependence:

$$\sigma(T) \propto exp[-(T_0/T)^{1/n}] \quad [1]$$

where T_0 is a reference temperature. Eq. 1 coincides with the Mott law for 3D non-interacting carriers if $n = 4$. Alternatively, when hops of non-interacting carriers are permitted only into a plane (2D), as for a strongly anisotropic carrier transport, n takes the value of 3.[24] Notice that Eq. 1 reduces to the NNH conductivity if $n = 1$.

As shown in Ref. 24, 25 the temperature dependence of Eq. 1 is such that the derivative d $ln(\sigma)$/d $ln(T)$ is a straight line of slope $p = -1/n$ when plotted by using *Log-Log* scales. As an example, an ideal conductivity curve formed of two traits with $n = 1$ and different thermal activation energies of 20 meV (low temperature) and 100 meV (high temperature) has been used to plot the *Log*[d $ln(\sigma)$/d $ln(T)$] curve of Fig. 4a. This curve is formed of two connected straight lines, each one of slope $p = -1$, one shifted with respect to the other. When the same data analysis is applied to the conductivity curves of the samples of Fig. 3, the curves of Figs. 4b, 4c, and 4d are obtained. In these figures, a continuous straight line of slope $p = -1$ is shown for comparison purpose, while dashed straight lines of slopes −1, −1/4, and −1/3 have been plotted on the low temperature data of Figs. 4b, 4c, and 4d, respectively. The good agreement between these lines and the trend of the experimental data indicate that the electrical activation of the implanted Al has been so efficient that an impurity band has been formed in all the specimens. It indicates also that the carrier transport mechanism in this band corresponds to NNH in the 1 $\times$ 10^{20} cm^{-3} specimen, to a 3D-VRH in the 3 $\times$ 10^{20} cm^{-3} sample, and to a strongly anisotropic almost 2D-VRH in the 5 $\times$ 10^{20} cm^{-3} specimen. This latter is the sample where the impurity band transport is visible also around room temperature, as evident from the data analysis of Fig. 4d.

It is worthwhile to remember that during the electrical measurements used to obtain the data plotted in Fig. 3 and studied in Fig. 4, the current was flowing in the direction parallel to the sample surface. The strong carrier transport anisotropy shown by the sample of Fig. 4d is consistent with the presence of an obstacle to the current flux in the direction orthogonal to the wafer surface. This may be a negative drawback for the application of so high Al implanted concentration in the fabrication of SiC electronic devices.

Taking into account the fact that the 4H-SiC lattice structure of the implanted layer of the sample of Fig. 4d is that shown in the TEM image of Fig. 2b, we can see that the strong anisotropic hole transport takes place in a surface layer confined by and containing stacking faults. These defects are probably at the origin of the strong anisotropy of the conductivity[19] that should be avoided when using the ion implantation technology for electronic device fabrication.

p-i-n diodes analysis.—The emitters of the 4H-SiC p-i-n diodes of this study are 2 $\times$ 10^{20} cm^{-3} Al^{+} implanted and the post implantation annealing treatment is 1950°C/5min. On the base of the structural and electrical characterizations presented above, mostly *D* defects are expected. These defects do not obstacle the flux of the current in the direction perpendicular to the junction interface. But, they might be the cause of shunt or tunneling currents across the junction. The static forward current-voltage characteristics of the most of the diodes of this study have shunt currents as low as the instrumental current floor, i.e. 1 $\times$ 10^{-14} A. While, only 15% of the fabricated diodes show the absence of a forward tunneling current. For that, we might infer that *D* defects may form a preferential path for tunneling currents. The estimated diode built-in potential is about 1.6 eV. This value agrees with the expected Al electrical activation and compensation in the implanted layer on the base of previous studies[26] and the nominal net donor density of the epi-layer. Among the diodes without tunneling and shunt currents there were a sufficient number of diodes with different perimeter to area ratio, between 10% and 15% of the total per each ratio value, to apply the procedure described in Ref. 10 and to obtain the area and the perimeter forward current density curves for this family of diodes. These curves, that are shown as symbols in Figs. 5 and 6, will be used to test possible scenarios for the simulation of the forward current-voltage characteristics of the diodes under test.

The simulation of the forward area current density has been performed by the sole hypothesis of a carrier lifetime dominated by carbon-vacancy related traps and an ideal diode structure, i.e. like a semi-infinite p-n interface. Table I resumes the traps related to V_C, their charge state and their position in the 4H-SiC bandgap, taken from Ref. 27. These traps have been distributed homogeneously in the diode

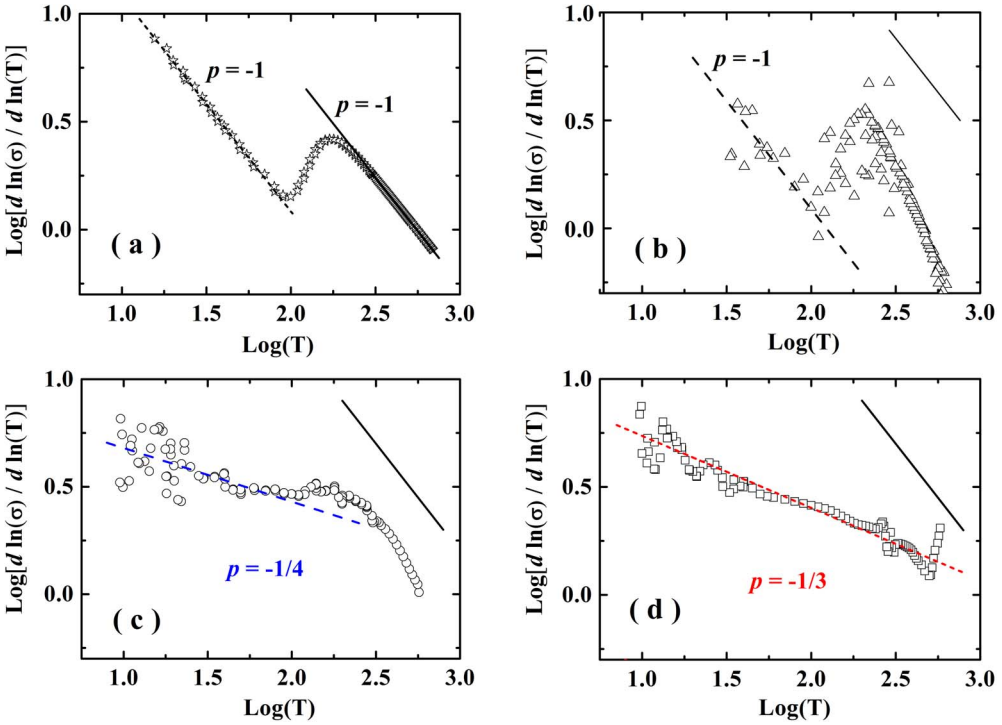

Figure 4. (a-d). *Log-Log* plot of the derivative of the ratio between the natural logarithms of the conductivity *ln*(σ) and that of the absolute temperature *ln*(T). *(a)* case of an ideal exponential conductivity curve with two traits of $I/n = 1$ and different thermal activation energies (see the text). *(b-d)* cases of the measured conductivity for the *(b)* 1×10^{20} cm^{-3}, *(c)* 3×10^{20} cm^{-3}, and *(d)* 5×10^{20} cm^{-3} samples (conductivity data in Fig. 3).

volume while hole and electron lifetimes, τ_h and τ_e, respectively, have been varied to reproduce the experimental curve. It is worthwhile to precise that lifetime contains the product of trap cross section times the trap density. In this study we performed the approximation to keep constant the trap density in the decade 10^{15} cm^{-3} and to use the cross section as adjustable parameter. Firstly, simulations have been performed with one trap at a time and optimization was looked for a limited region of the experimental curve. More precisely, the mid-gap trap EH_7 has been used to reproduce the recombination current region, i.e. the region at low voltage, while the less deep traps Z_1/Z_2 have been used to reproduce the intermediate voltage region where diffusion current may be important. Comparison between simulation outputs and experimental curve are shown in Fig. 5. The τ_h and τ_e used to obtain the simulated curves of Fig. 5 are shown in Table I. In Fig. 5, the simulated curve with all the traps at the same time but lifetimes values got from the simulations with one trap at a time, is also shown. This latter curve has a good agreement with the experimental one.

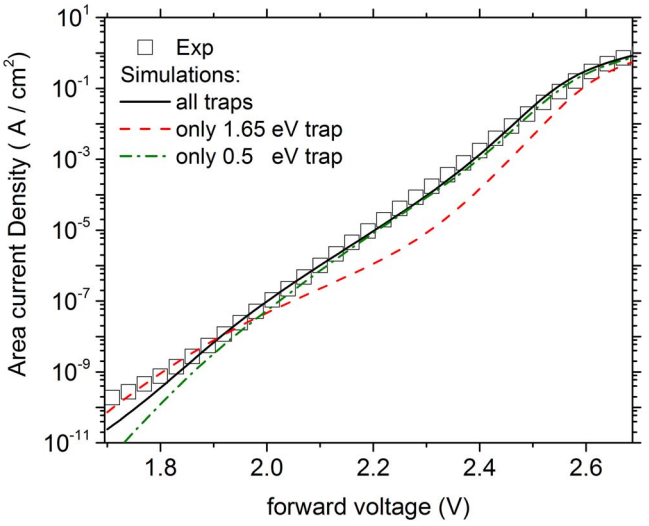

Figure 5. Comparison between experimental (symbols) and simulated (lines) area current density curves for the diodes under test in this study. Dashed and continuous lines correspond to simulations performed under the hypothesis of a single trap at a time (see legend) and all the traps at the same time, respectively.

The simulation of the perimeter current density of the 4H-SiC diodes under test has been performed taking into account the cylinder symmetry of the implanted emitters, and the presence of n-type 4H-SiC material around the emitter up to a distance of 50 μm, the same homogeneous defect distribution used for the simulation of the area current density component, i.e. defects and lifetimes of Table I, and the presence of a fixed charge at the SiC wafer surface. The latter assumption is motivated by the fact that the diodes under test have been processed leaving the SiC surface no passivated, i.e. the SiC surface remained exposed to air. It is known that a very thin silicon dioxide film growth on this surface and that such a film may contain or may trap at the oxide/semiconductor interface negative fixed charge. Simulations have been performed taking into accounts these options: *(i)* positive and negative fixed charge, *(ii)* different charge amount in the range 5×10^{12} –5×10^{14} cm^{-2}. For comparison purpose, simulations have been performed also in absence of fixed charge. The simulated perimeter current component has been obtained by subtracting the simulated area component from the results of the above simulations. Figs. 6a and 6b compare experimental and simulated curves for positive and negative fixed charge, respectively. The perimeter current curve for zero fixed charge corresponds to the current collected at the lateral side of the cylinder emitter. It can be seen that this current is too low to account for the experimental perimeter current density. Major contributions come from the hypothesis of a fixed charge at the sample surface.

Fig. 6a shows that a positive fixed charge accounts for a not negligible perimeter current contribution that saturates for charge amounts equal to or above the minimum hypothesized value of 5×10^{12} cm^{-2} without being able to equal the experimental curve. Fig. 6b shows

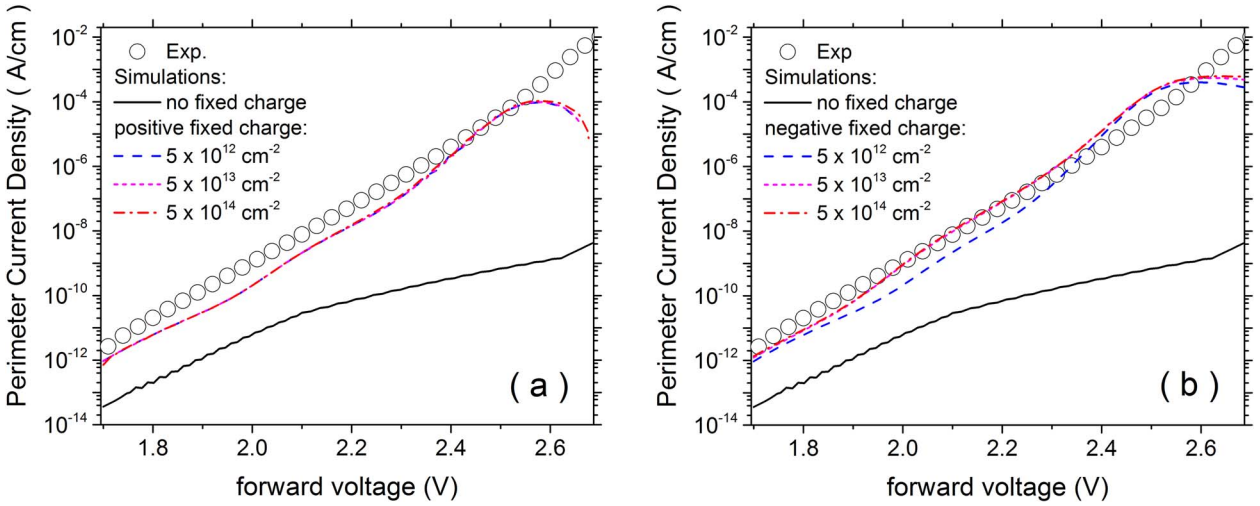

Figure 6. (a). Comparison between experimental (symbols) and simulated (lines) perimeter current density curves for the diodes under test in this study. Dashed and continuous lines are simulations outputs for the hypothesis of fixed charge of different sign, positive in *(a)* and negative in *(b)*, and various surface density values (see legend). Simulations take into account the defects of Table I and the lateral side of the implanted cylinder emitter. For comparison purpose, this latter current contribution is shown as a continuous line both in *(a)* and in *(b)*.

Table I. Traps and surface fixed charge used for the simulations of Figs. 5 and 6a, 6b.

V_C related defect	defect type	E_c - E_T (eV)	τ_e (ns)	τ_h (ns)
$EH_7(0/+)$	Donor	1.68	60	140
$Z_1(-/0)$ or $Z_2(-/0)$	Acceptor	0.5	100	5

that the hypothesis of a negative fixed charge better account for the experimental curve, in fact, for negative charge $\geq 5 \times 10^{13}$ cm^{-2} the simulated curves overlap with the experimental one. Nevertheless, it can be seen that the output plots of the simulation process do not exactly follow the shape of the experimental curve.

Taking into account the ensemble of the results of Figs. 5, 6a and 6b we can affirm that the hypothesis of forward recombination current controlled by the EH_7 traps, forward diffusion current dominated by the Z_1/Z_2 defects, negative fixed charge homogeneously distributed at the sample surface, sounds reasonable but not sufficient to describe the correct trend of both area and perimeter current density data of the diodes under test. Further study of the reverse characteristics and temperature dependence may help to clarify that point. It may be that the real system is more complex than the here proposed model.

Conclusions

The structural and electrical characterization of Al implanted HPSI 4H-SiC layers that have been annealed at 1950°C show that *(i)* on increasing the implanted Al concentration different type of extended defects form and grow; and that *(ii)* a strong anisotropic hole transport in a surface layer, confined by and containing a high density of basal plane stacking faults, can take place. Basal plane stacking faults may be detrimental for SiC electronic devices operation and they should be avoided. The results of this study suggest that a way to avoid their presence is to keep the maximum Al plateau concentration in the 4H-SiC samples below a value of about 2×10^{20} cm^{-3} that in this case also corresponds to the Al solid solubility limit at the employed annealing temperature.

Taking into account the fact that a 1950°C treatment generates an elevated density of V_C in the drift layers of ion implanted devices, this study has shown how the unique hypothesis of a carrier lifetime dominated by carbon-vacancy related traps plus fixed charge at the SiC wafer surface may account for the simulation of the forward current-voltage curves of Al implanted bipolar 4H-SiC diodes. The results of the simulations are in reasonable agreement with the experimental data.

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