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### Low-cost and green fabrication of polymer electronic devices by push-coating the polymer active layers

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3 **Low-cost and green fabrication of polymer electronic**  
4 **devices by push-coating the polymer active layers**  
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3 ABSTRACT  
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6 Due to both their easy processability and compatibility with roll-to-roll processes,  
7 polymer electronics is considered to be the most promising technology for the  
8 future generation of low-cost electronic devices such as light-emitting diodes and  
9 solar cells. However, the state-of-the-art deposition technique for polymer  
10 electronics (spin-coating) generates a high volume of chlorinated solution wastes  
11 during the active layer fabrication. Here, we demonstrate that devices with  
12 similar or higher performances can be manufactured using the push-coating  
13 technique in which a polydimethylsiloxane (PDMS) layer is simply pressed  
14 against a very small amount of solution (less than  $1\mu\text{l}/\text{covered cm}^2$ ) which is then  
15 left for drying. By tuning the PDMS thickness, both the applied pressure and the  
16 solvent diffusion rates can be optimized to generate the desired active layer  
17 thickness. Unlike spin-coating, push-coating is a slow drying process which  
18 induces a higher degree of crystallinity in the polymer thin film without the  
19 necessity for a post-annealing step. The polymer light-emitting diodes and solar  
20 cells prepared by push-coating exhibit slightly higher performances with respect  
21 to the reference spin-coated devices while at the same time reducing the amounts  
22 of active layer materials and chlorinated solvents by 50 times and over 20 times,  
23 respectively. These increased performances can be correlated to the higher  
24 polymer crystallinities obtained without applying a post-annealing treatment. As  
25 push-coating is a roll-to-roll compatible method, the results presented here open  
26 the path to low-cost and eco-friendly fabrication of a wide range of emerging  
27 devices based on conjugated polymer materials.  
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40 Keywords: polymer solar cells; polymer light-emitting devices; PDMS; organic  
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**Introduction:**

Polymer light-emitting devices (PLEDs) and solar cells (PSCs) have been developing over the past decade with a large number of publications emphasizing their potential for low-cost electronic device fabrication with efficiencies on par with their state-of-the-art inorganic counterparts.<sup>1-7</sup> PLEDs and more generally organic LEDs are successfully tackling the mobile display market thanks to their several advantages over conventional display devices, including fast response time, high brightness and contrast, low power consumption, flexibility and lightweight.<sup>8-13</sup> Similarly, PSCs now reach power conversion efficiencies (PCE) overcoming the milestone value of 10% and closing the gap with the state-of-the-art amorphous silicon solar cells.<sup>7, 14-17</sup>

While spin-coating is the most explored film deposition technique on a lab scale due to the simplicity of its use, it is possibly the least suited process to efficiently manufacture large-scale PSCs and PLEDs. To realistically reduce the production cost by using high-productivity technologies such as the roll-to-roll process, finding the adequate method (ideally performed in air and reducing the use of chlorinated solvents) is essential.<sup>18</sup> The need for scalable printing and coating techniques have recently led to explore other approaches such as contact printing,<sup>19, 20</sup> screen printing<sup>21</sup> and inkjet printing,<sup>22</sup> which have successfully been applied both in PLEDs and in PSCs. In 2012, Ikawa *et al.* developed a process referred to as push-coating in which a small amount of solution is deposited on a substrate and then covered by a multilayer elastomer resulting in the formation of homogeneous poly(3-hexylthiophene) (P3HT) layers which are consequently used as active layers for the fabrication of large-scale and low-cost organic field-effect transistors (OFETs).<sup>23</sup> This innovative active layer fabrication approach is a two-step process in which a homogeneous wet polymer layer is firstly formed by capillarity, followed by a solvent drying step (solvent diffusing through the

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3 elastomeric material). A particular attention was given to the development of the  
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5 elastomeric material (referred to as the stamp) to control the solvent diffusion kinetics.  
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7 In particular, Ikawa *et al.* emphasized that the stamp should have adequate solvent  
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9 retention properties to allow for easy removal without damaging the surface of the  
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11 active layer at the end of the deposition process. The strategy used to generate such  
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13 solvent retention properties was to develop a poly(dimethylsiloxane) (PDMS) based  
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15 trilayer stamp in which a fluorocarbon polymer with solvent diffusion barrier properties  
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17 is sandwiched between two micrometer thin PDMS layers.  
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21 Push-coating can be considered an eco-friendly process as it reduces the amount  
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23 of active layer materials and chlorinated solvents by factors of approximately 50 and 20,  
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25 respectively, compared to spin-coating. In particular, chlorinated solvents have been  
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27 proven to have short-term and long-term effects on both the environment and the human  
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29 health. Recent studies on PSCs have been focusing on reducing as much as possible  
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31 their usage during device fabrication by, for instance, using green solvent processable  
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33 active materials<sup>24</sup> or water-based microemulsions instead of chlorinated solutions.<sup>25</sup>  
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35 While push-coating considerably reduces the use of chlorinated solvents, the previously  
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37 designed trilayer stamp introduces additional preparation steps and fluorinated materials  
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39 (which may also have negative effects on the environment). Recently, a second attempt  
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41 to use push-coating for electronic device fabrication resulted in the generation of PSCs  
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43 with PCEs up to 2.65 % (as compared to 3.94% for the reference spin-coated devices).<sup>26</sup>  
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45 These promising results, obtained by using extremely thin single layer PDMS stamps,  
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47 demonstrated that push-coating can be applied not only to OFET fabrication but also to  
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49 PSCs. However, the push-coated devices displayed much lower device performances  
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51 compared to the spin-coated reference devices and the reproducibility of the  
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3 photovoltaic performances was rather low with the necessity to use weights on top of  
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5 the stamps during the process (decreased control over the process).  
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8 Here, we study the push-coating process using single layer PDMS stamps and  
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10 varying the PDMS stamp thickness to increase the control over the active layer  
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12 deposition of PLEDs and PSCs. In particular, by analyzing thickness-dependent  
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14 diffusion rates in PDMS of two typically employed solvents, we were able to optimize  
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16 the process conditions and to correlate the diffusion rates with the device performances  
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18 in standard yellow-green PLEDs based on poly(9,9-dioctylfluorene-*alt*-  
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20 benzothiadiazole) (F8BT). The solvents used for this study were chlorobenzene (CB)  
21  
22 and dichlorobenzene (DCB). We found that, in devices fabricated by push-coating using  
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24 less than 1  $\mu\text{l}$  of active layer solution/covered  $\text{cm}^2$ , external quantum efficiencies  
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26 (EQEs) and luminous efficiencies (LEs) are equivalent or higher to those obtained for  
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28 spin-coated devices. To our knowledge, this is the first time that push-coating  
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30 processing is applied to PLED fabrication. In addition, in push-coated P3HT:phenyl-  
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32 C61-butyric acid methyl ester (PCBM) PSCs, we obtained, without annealing steps,  
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34 similar or higher performances compared to annealed spin-coated active layer devices.  
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36 Unlike previous studies on push-coated PSCs, we therefore demonstrate that devices  
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38 with similar performances to spin-coated devices can be obtained by simply adjusting  
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40 the thickness of the PDMS used for this eco-friendly and roll-to-roll compatible process.  
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## 48 **Experimental Section:**

### 49 *PDMS stamp fabrication and solvent diffusion properties*

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52 PDMS elastomer (Sylgard 184) was purchased from Dow Corning. To fabricate  
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54 the stamps, the PDMS precursor was mixed with the curing agent (10:1 weight ratio)  
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56 and stirred using a glass micropipette. After degassing the mixture to remove air  
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3 bubbles formed during stirring, standard glass Petri dishes with polished surface were  
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5 used for the mixture deposition and stamp fabrication at 80°C for at least two hours.  
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7 The thickness of the PDMS stamps was controlled by the volume of mixture deposited  
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9 on the cleaned Petri dishes.  
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12 Solvent diffusion properties were characterized using two different methods and  
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14 three different solvents (water, CB and DCB) at room temperature and 50°C. The first  
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16 method consisted in immersing the PDMS stamp into the various solvents (absorption)  
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18 or letting it dry (desorption) for a given amount of time and measuring the relative  
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20 weight variation to extract absorption and diffusion rates. The second method consisted  
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22 in depositing 25 x 25 mm<sup>2</sup> PDMS stamps with various thicknesses (2, 3 and 4 mm) on 3  
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24 μL of test solvent (water, CB and DCB) for 5 min at room temperature or 50°C. The  
25  
26 weight variation of the PDMS stamps before and after the test allowed us to extrapolate  
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28 the amount of solvent retained for each PDMS stamp thickness and experimental  
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30 condition.  
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### 36 *Device preparation and characterization*

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38 Following a standard cleaning procedure, 40 nm thick poly(3,4-ethylene  
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40 dioxythiophene):poly(styrene sulfonate) (PEDOT:PSS, Clevios AI4083) layers were  
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42 spin-coated on ITO covered glass substrates and consequently annealed at 150°C for 10  
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44 min. The active layer solutions for push-coating process were prepared in either CB or  
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46 DCB at concentrations of 10 and 20 mg/ml for F8BT and P3HT:PCBM, respectively.  
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48 Note that the push-coated organic layers were prepared in air. For spin-coating, the  
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50 solution concentrations were increased to 20 and 30 mg/ml, for F8BT and P3HT:PCBM  
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52 respectively. The P3HT:PCBM ratio in both PSC active layer solution was kept at 1:0.8.  
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54 For active layers deposited on glass/ITO/PEDOT:PSS substrates (25 x 25 mm<sup>2</sup>),  
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3 volumes of 3 and 80  $\mu\text{L}$  of solution were used for push-coating and spin-coating,  
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5 respectively. Various spin-coating speeds for F8BT deposition were used to obtain a  
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7 range of active layer thicknesses while P3HT:PCBM active layers were optimized at a  
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9 thickness of 110 to 130 nm obtained at 800 rpm for 60s. The spin-coated P3HT:PCBM  
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11 active layers were annealed at 140  $^{\circ}\text{C}$  for 10 min prior to electrode deposition to  
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13 enhance their photovoltaic performances. The devices were finalized by evaporating  
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15 Ba/Al and LiF/Al electrodes, respectively for PLEDs and PSCs, prior to an  
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17 encapsulation step to prevent photo-oxidation of the devices. For PLEDs,  
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19 electroluminescence (EL) spectra were measured using CCD combined with  
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21 monochromator (Spex 270M) and applying constant bias between 3 and 12 V. The  
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23 current density-voltage-luminance (J-V-L) characteristics were recorded with a Keithley  
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25 2602 source meter. Light emitted from the devices was detected in forward direction  
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27 using a calibrated photodiode. Thicknesses of the devices were measured with a Dektak  
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29 XT (Bruker) profilometer. The encapsulated PSCs were characterized using a source  
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31 meter (Keithley 2401) and a solar simulator (AM 1.5G, 100  $\text{mW}/\text{cm}^2$ ) at room  
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33 temperature to extract their photovoltaic performances.  
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### 39 *Morphological characterizations*

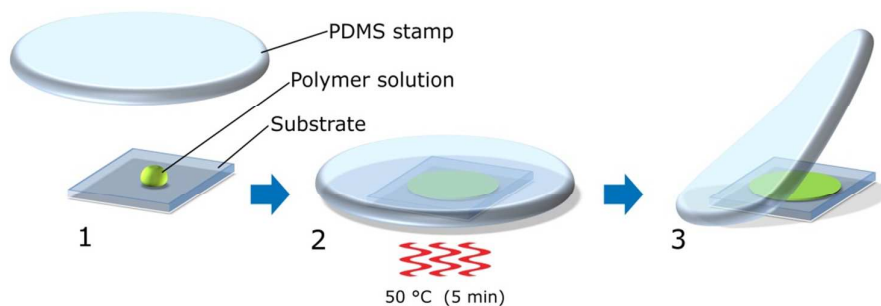
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42 AFM investigations were performed using a NT-MDT NTEGRA apparatus in  
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44 tapping mode under ambient conditions. X-ray diffraction patterns (XRD) carried out in  
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46 Bragg-Brentano geometry were obtained at 20  $^{\circ}\text{C}$  using a Siemens D-500  
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48 diffractometer equipped with a sensible detector (VORTEX), Soller slits ( $2^{\circ}$ ) and  
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50 narrow slits ( $0.3^{\circ}$ ), and a Siemens FK 60-10 2000W tube (Cu  $\text{K}_{\alpha}$  radiation,  $\lambda = 0.154$   
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52 nm). The operating voltage and current were 40 kV and 40 mA, respectively. Data were  
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54 collected from  $3^{\circ}$  to  $30^{\circ}$  ( $2\theta$ ) at  $0.05^{\circ}$  intervals (9s for each one).  
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## Results and Discussions:

### *Solvent retention in mm thick PDMS stamps*

Previous attempts for push-coating were based on the use of very thin PDMS layers either consisting of single PDMS layers or PDMS-fluoropolymer-PDMS trilayers.<sup>23, 26</sup> In the trilayers, the fluoropolymer acts as a solvent blocking layer (no solvent diffusion), allowing for the retention of the solvent in the lower part of the stamp which is in contact with the generated polymer layer. This approach induces facile removal of the stamp after the thin flat film is formed and prevents damage to the film surface while increasing the film homogeneity. In fact, the results for PSCs prepared using push-coating with 80-100 nm thick PDMS single layers exhibit a lower degree of reproducibility as the solvent quickly escapes from the top part of the PDMS leaving an entirely dry PDMS/active layer interface prior to PDMS removal which may damage the active layer surface. Additionally, due to the solvent sorption and desorption kinetics, when exposed to chlorinated solvents, nanometer thin PDMS stamps with low mechanical properties will have a tendency to buckle which further decreases the homogeneity of the generated films, in particular, for large scale device preparation (see Supporting Information, **Figure S1**). For these reasons, the study on push-coating performed until now required the application of additional weight/pressure on top of the PDMS stamps which complicates the process. Furthermore, fabrication of the trilayer stamp not only requires two mixing/curing processes but also surface functionalization to ensure that the three layers adhere to each other. On the other hand, the fabrication of 80-100 nm thin PDMS stamps requires preparing the film between two flat plates by applying a controlled pressure. Additionally, due to their low mechanical properties, their handling (e.g. deposition on the wet polymer solution) becomes much more difficult.



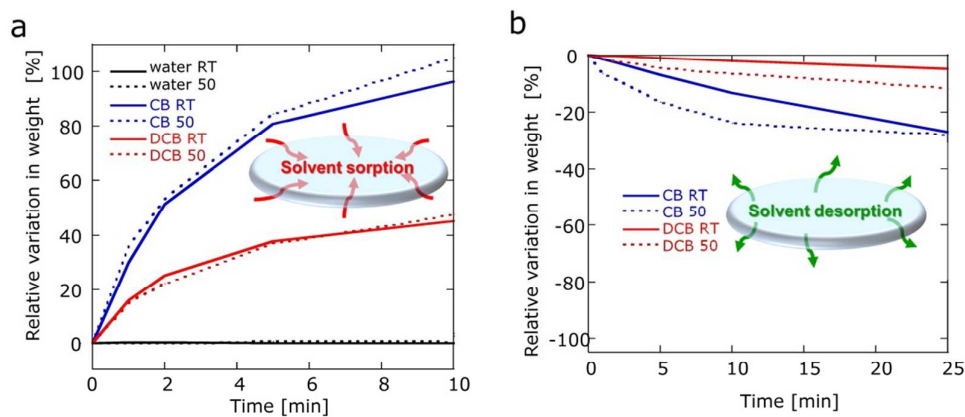
**Figure 1.** Schematic representation of the push-coating process. A droplet of the semiconducting polymer solution is placed on the substrate and the single-layer PDMS stamp is applied on top of it (step 1); the assembly is heated at 50 °C for 5 min (step 2) and then the PDMS stamp is peeled off leaving a whole thin film on the substrate (step 3).

Our approach is to fabricate thicker PDMS films (thickness on the millimeter scale) and study their sorption/desorption kinetics with the solvents commonly used for organic electronic device preparation. In thicker PDMS stamps, the solvent diffuses over larger distances from the bottom surface (in contact with the wet polymer layer) to the top surface (in contact with air) resulting in a larger quantity of solvent remaining trapped inside the stamp for relatively short push-coating times. As the single layer PDMS is produced in a single mixing/curing process and as thicker stamps can be prepared without the application of pressure by simply controlling the thickness with the volume inserted in the Petri dishes, the fabrication process of our stamps is much simpler than the ones presented in the previous studies. Last but not least, the thickness of the PDMS not only controls the solvent diffusion kinetics but also provides some weight and enhanced mechanical properties to the stamp, which makes the overall process much simpler and roll-to-roll compatible.

As depicted in **Figure 1**, in our simplified push-coating approach to fabricate polymer electronic devices, the active layer deposition consists in applying a 2-4 mm

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3 thick PDMS monolayer stamp on a 3  $\mu$ L droplet of polymer solution pre-deposited on  
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5 the glass/ITO/PEDOT:PSS substrate (step 1), followed by heating of this assembly at  
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7 moderate temperature (step 2) and finally peeling off the PDMS stamp (step 3).  
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10 To verify whether our approach using thicker PDMS stamps can be applied to push-  
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12 coating, we first studied the solvent retention abilities of 3 mm thick PDMS films. By  
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14 soaking the PDMS stamps into CB, DCB and water for up to 10 min and drying them in  
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16 air for up to 25 min (**Figure 2**), we observed that both sorption and desorption of CB  
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18 into/from PDMS occur at a much faster rate compared to DCB. However, after 10 min  
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20 of soaking, both solvents seem to be approaching a saturation level suggesting that less  
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22 DCB can be absorbed by PDMS as compared to CB. Furthermore, although no major  
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24 changes can be observed for sorption at room temperature and 50  $^{\circ}$ C for either CB or  
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26 DCB, the desorption kinetics seem to be highly dependent on the drying temperature for  
27  
28 both chlorinated solvents. Note that water does not diffuse inside the PDMS stamps  
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30 even when the stamp is soaked in water at 50 $^{\circ}$ C for 10 min.  
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**Figure 2.** Solvent sorption (a) and desorption in air (b) measured on 3 mm thick PDMS stamps at room temperature and at 50  $^{\circ}$ C.

53 This suggests that push-coating is limited to solvents displaying the adequate  
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55 PDMS surface wetting properties. However, unlike chlorinated solvents (toxic to both  
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environment and humans), water and other common polar solvents (such as alcohols) are considered eco-friendly and therefore, reducing their usage is not as essential as reducing chlorinated solvent usage. These results also suggest that the ideal conditions for push-coating (solvent remaining in the PDMS stamp to avoid surface damage and ease the stamp removal process) should be more likely obtained with DCB at 50 °C and CB at room temperature as the PDMS stamp is neither saturated with solvent nor dry. In fact, during the actual push-coating process, the amount of solvents used is rather low and therefore, to maintain high levels of solvent inside the PDMS stamps, a slow desorption rate (e.g. DCB at 50 °C) may be ideal. However, if the desorption rate is too slow (e.g. DCB at room temperature), the wet PDMS surface in contact with the dried active layer film may damage its surface (partial transfer of the active layer on the PDMS stamp upon removal).

To verify how much solvent remains inside the PDMS layer at the end of the process and assess the effect of the stamp thickness, we measured the weights of solvent included in PDMS stamps with thickness of 2, 3 and 4 mm deposited on 3  $\mu$ l of solvent. The PDMS stamps were left on the solvent droplet for 5 min at either room temperature or 50 °C. We selected a time of 5 min to ensure that no solvent remains between the substrate and the PDMS stamp. The results are summarized in **Table 1**.

**Table 1.** Solvent remaining (%) in PDMS stamps with increasing thickness.

	<b>2 mm</b>	<b>3 mm</b>	<b>4 mm</b>
CB (RT)	78	93	97
CB (50 °C)	39	75	87
DCB (RT)	85	97	98
DCB (50 °C)	54	79	87

From these experiments, we can clearly observe that DCB is retained within the PDMS stamp much more easily compared to CB. Results at 50 °C provide a wider

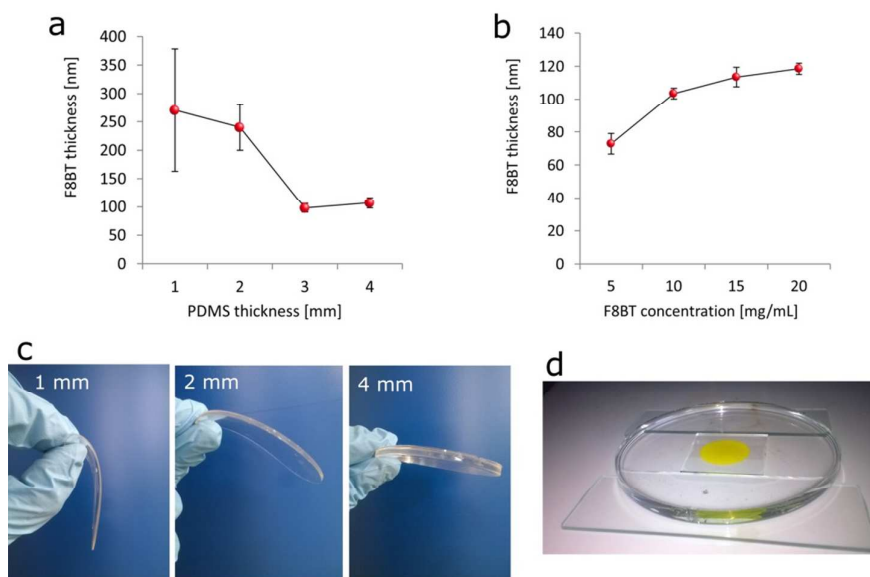
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3 range of solvent retention capacity, therefore representing the ideal system to study the  
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5 effect of solvent retention on the quality of the produced films. The differences  
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7 observed for the 2 mm thick PDMS for CB and DCB at 50 °C (39 and 54 % of solvent  
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9 remaining in the PDMS stamp for CB and DCB, respectively) suggest that, in the case  
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11 of CB, the solvent quickly moves away from the surface in contact with the substrate.  
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13 Therefore, we expect to have a higher degree of control for films prepared from DCB as  
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15 compared to those prepared with CB, in particular when using 2 mm thick PDMS  
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17 stamps.  
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### 20 21 *Increased performances in push-coated PLEDs*

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23 To assess the applicability of push-coating to solution processed PLEDs, we  
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25 chose the widely used F8BT as semiconducting light-emitting material for the active  
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27 layer. The process was performed following the conditions schematized in **Figure 1**,  
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29 including the 5 min heating at 50 °C as this step provides the best conditions and  
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31 highest film quality for push-coating. Because DCB solutions produced quite uniform  
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33 F8BT films while those push-coated from CB sometimes showed some inhomogeneity  
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35 (see Supporting Information, **Figure S2**), we employed DCB for processing F8BT  
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37 PLEDs. Furthermore, the higher degree of homogeneity obtained with DCB confirms  
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39 that the push-coating process is generally better controlled when DCB is used, as  
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41 suggested by the solvent retention tests performed on pure solvents (**Figure 2** and **Table**  
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49 To fabricate a fully functional PLED, it is important to control the active layer  
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51 thickness. In fact, for an efficient light emission from the device, the optimum thickness  
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53 of the semiconducting polymer layer is essential, since it can affect both electrical and  
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55 optical device characteristics, such as the charge carrier transport and, consequently, the  
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3 efficiency and color.<sup>27</sup> In our push-coating approach, the thickness of the PDMS stamp  
4 has a direct influence on the thickness of the F8BT film. This is not only related to the  
5 different pressure that stamps having different weights naturally apply on the polymer  
6 solution but also to the different drying kinetics when using PDMS with various  
7 thicknesses. In fact, a slower drying process and higher applied pressure (thicker  
8 PDMS) will induce the spreading of the solution over a larger area as compared to push-  
9 coating performed with thinner PDMS stamps. As shown by the plot in **Figure 3a**, by  
10 push-coating a 10 mg/mL F8BT solution in DCB, the active layer thickness decreases  
11 from around 300 to around 100 nm by increasing the PDMS thickness from 1 to 4 mm.  
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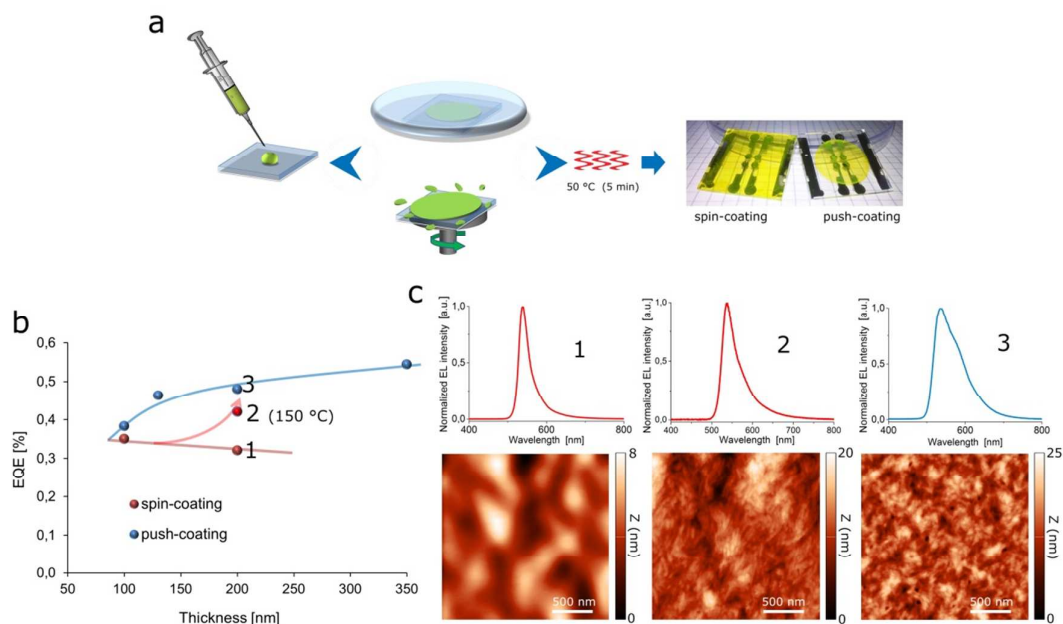


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47 **Figure 3.** a) Dependence of active layer thickness on the thickness of PDMS stamp. b)  
48 Dependence of active layer thickness on polymer concentration, using a 3 mm PDMS stamp. c)  
49 Photographs of 1, 2 and 4 mm thick PDMS stamps, showing different stiffness. d) Photograph of a push-  
50 coated F8BT film during the processing.  
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55 Another important outcome of this test is that the thickness variability is much  
56 higher in the 1 mm PDMS stamp than in the 2 mm one, while it is very small for the 3  
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3 and 4 mm stamps, which provide very similar results. This can be explained by the  
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5 synergy of two effects: the larger solvent amount retained by thicker stamps which, as  
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7 assessed before, provides an improved process control; and the change in mechanical  
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9 properties with PDMS thickness. The growing stiffness and weight observed for 1, 2  
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11 and 4 mm stamps (**Figure 3c**) correlates well with the enhancement in thickness  
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13 homogeneity/reproducibility of the F8BT film (**Figure 3a**). Additionally, thinner PDMS  
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15 stamps have a tendency to buckle during solvent diffusion which further decreases the  
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17 control over uniform film formation (**Figure S1**). Consequently, the stiffer the stamp is,  
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19 the flatter its surface will stay when put in contact with the polymer solution,  
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21 guaranteeing homogenous spreading and final film formation, as seen in the photograph  
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23 shown in **Figure 3d**.  
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28 While the stamp thickness controls film uniformity and thickness range in the  
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30 push-coating process, the semiconducting polymer concentration provides finer  
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32 thickness tunability. As an example, the plot in **Figure 3b** shows the film thickness  
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34 variation obtained by push-coating F8BT solutions in DCB at different concentrations  
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36 (5, 10, 15 and 20 mg/mL) with a 3 mm PDMS stamp; by adjusting F8BT concentration,  
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38 the active layer thickness is well tuned from 70 to 120 nm, a typical thickness range for  
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40 organic electronic devices. It is also worth noticing that, using a 2 mm stamp and  
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42 properly adjusting the polymer solution concentration, relatively homogeneous 300 nm  
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44 thick active layers can be produced by our method. These cannot be easily obtained by  
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46 spin-coating as the thickness is limited by the polymer solubility in organic solvents and  
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48 by the necessity for high rotating speeds to generate large scale homogeneous films.  
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**Figure 4.** Comparison between push-coated and spin-coated PLEDs. a) Schematic representation of device preparation. b) EQE of different spin-coated and push-coated devices as a function of F8BT thickness. c) Normalized EL spectra (top) and surface morphology (bottom) of three representative devices with 200 nm active layer thickness: (1) spin-coated, (2) spin-coated after annealing at 150 °C for 30 min, and (3) push-coated.

Once the process control and film quality of the push-coated F8BT layers was assessed, we tested them in PLEDs. To do this, we compared push-coated and spin-coated devices with the same standard architecture for yellow-green PLEDs (ITO/PEDOT:PSS/F8BT/Ba/Al) and similar active layer thickness. To facilitate a direct comparison, the spin-coated devices were manufactured in air and subjected immediately after deposition to the same mild thermal treatment optimized for the push-coating process, as schematized in **Figure 4a**. The device performances are summarized in **Table 2** and plotted in **Figure 4b** as a function of F8BT thickness (detailed characterization data are also available in the Supporting Information, **Figure S3**).



**Table 2.** Spin-coated and push-coated F8BT PLED performances.

Device type (thickness)	$V_{on}$ (V)	EQE <sup>a</sup> (%)	LE <sup>b</sup> (cd/A)	PE <sup>b</sup> (lm/W)
spin-coated (100 nm)	2.5	0.35/0.31	1.1	0.60
spin-coated (200 nm)	5.0	0.32/0.25	1.0	0.27
push-coated (100 nm)	2.5	0.39/0.37	1.3	0.65
push-coated (130 nm)	2.5	0.48/0.47	1.7	0.85
push-coated (200 nm)	3.5	0.49/0.46	1.6	0.36
push-coated (350 nm)	4.0	0.55/0.55	2.1	0.37
spin-coated (200 nm) 150°C	6.0	0.42/0.32	1.2	0.32

<sup>a</sup> Max/values for 50 mA/cm<sup>2</sup>. <sup>b</sup> Values for 50 mA/cm<sup>2</sup>.

The EQE of spin-coated PLEDs with standard (100 nm) and thicker (200 nm) active layer remained nearly constant around 0.35 %. The corresponding push-coated devices with 100 and 200 nm F8BT thickness both exceeded this efficiency value. Moreover, unlike spin-coated devices, in the push-coated PLEDs we observed a gradual efficiency increase with thickness, and the highest values were obtained for active layer thickness above 300 nm (EQE = 0.55 %, LE = 2.1 cd/A). Consequently, while the efficiency difference between the 100 nm thick devices obtained by the two different processes was narrow (0.04 %), the difference between the 200 nm spin-coated and push-coated PLEDs (0.14 %) becomes more relevant.

To shed light on the different trends observed, we investigated these devices by spectroscopical and morphological analysis. As shown in **Figure 4c**, all the devices displayed similar electroluminescence (EL) spectra, with the maximum peak located around 540 nm. However, while the device obtained by spin-coating (**1**) showed a smooth active-layer surface by AFM, with RMS roughness of 1.2 nm, the push-coated PLED (**3**) showed a more organized morphology with the polymer arranged in tightly packed fibril-like domains, resulting in a RMS roughness of 2.8 nm.

The post-deposition annealing temperature plays an essential role in determining the morphology of a spin-coated polymer film,<sup>28-30</sup> and therefore, we fabricated spin-

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3 coated devices (**2**) prepared under the same conditions as for **1** but which were annealed  
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5 at 150 °C for 30 min before evaporating the metallic electrodes. As shown by the plot in  
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7 **Figure 4b**, the annealed device **2** exhibited intermediate performances with respect to  
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9 the pristine spin-coated (**1**) and the push-coated (**3**) devices, suggesting that the  
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11 annealing process triggered the enhancement of the polymer packing/self-organization,  
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13 leading to higher PLED efficiency. This was confirmed by AFM analysis, which  
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15 evidenced that for the annealed spin-coated film **2** a fibrillar morphology resembling  
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17 that observed for the push-coated film **3** (see **Figure 4c**), with the RMS roughness  
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19 passing from 1.2 to 2.3 nm after the annealing process. In polymer semi-conducting thin  
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21 films, chain aggregation can have a major impact on the charge transport properties as  
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23 the charge transport mechanism in these materials relies on both intrachain transport  
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25 and charge hopping to neighboring chains. Therefore, a more efficient balance between  
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27 charge transport and recombination within F8BT active layer can be expected in **2** and **3**  
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29 with respect to **1**, which accounts for the different PLED performances.<sup>31</sup> In the light of  
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31 these observations, we can ascribe the slightly better performances shown by push-  
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33 coating approach with respect to spin-coating, to the slower film formation process  
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35 which produces a better polymer self-organization, possibly resulting in a moderately  
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37 higher degree of crystallinity (see Supporting Information, **Figure S4**), even without  
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39 thermal annealing. It is worth noticing that well-performing PLEDs with active layer  
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41 thickness over 300 nm cannot be easily obtained by spin-coating and their fabrication in  
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43 standard architecture has rarely been reported.<sup>32, 33</sup> Moreover, to fabricate the 200 nm  
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45 devices, 3 μL of F8BT solution at the concentration of 10 mg/mL and 80 μL of 20  
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47 mg/mL solution were used in the push-coating and spin-coating processes, respectively.  
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49 Fabricating PLEDs by push-coating therefore reduces used active layer material and  
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51 solvent amounts by factors of 50 and 20, respectively, as compared to spin-coating.  
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### *Enhanced photovoltaic effect in highly crystalline push-coated PSCs*

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6 Unlike F8BT, whose amorphous nature limits the possibility for effectively  
7 observing changes in crystallinity between push-coated and spin-coated films, much  
8 more notable changes are expected when depositing thin films based on the highly  
9 regioregular and consequently crystalline P3HT. In fact, the previous study on push-  
10 coating of P3HT films for OFET fabrication revealed that the push-coated P3HT films  
11 exhibit a higher degree of crystallinity as compared to their spin-coated equivalents.<sup>23</sup>  
12 Scientific literature clearly emphasizes that both the post-deposition annealing  
13 temperature and the boiling point of the solvent used for active layer deposition play  
14 essential roles in determining the morphology of P3HT:PCBM films.<sup>34, 35</sup> To understand  
15 the effect of the solvent (CB or DCB) over the crystallinity and device performances of  
16 push-coated P3HT:PCBM PSCs and compare them with spin-coated films, we  
17 performed the experiments with 3 mm thick PDMS stamps at 50 °C for 5 min as these  
18 process parameters resulted in the optimized active layer thickness for regular PSCs. In  
19 spin-coated films, the crystallinity of the polymer:fullerene blend depends on the  
20 evaporation rate of the solvent; a higher degree of crystallinity is obtained for slower  
21 evaporation rates. Similarly, in push-coated films, we expect to observe highly  
22 crystalline structures when using solvents with a slower diffusion rate inside the PDMS  
23 stamp. In our case, this would correspond to DCB which, coincidentally, is also the  
24 solvent with the slower evaporation rate.

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49 To determine whether our hypothesis on diffusion rate and crystallinity was  
50 valid, we first performed XRD measurements to observe the evolution of the (100)  
51 P3HT crystallinity peak in the films prepared using the two solvents by either spin-  
52 coating or push-coating (**Table 3** and **Figure S5**).

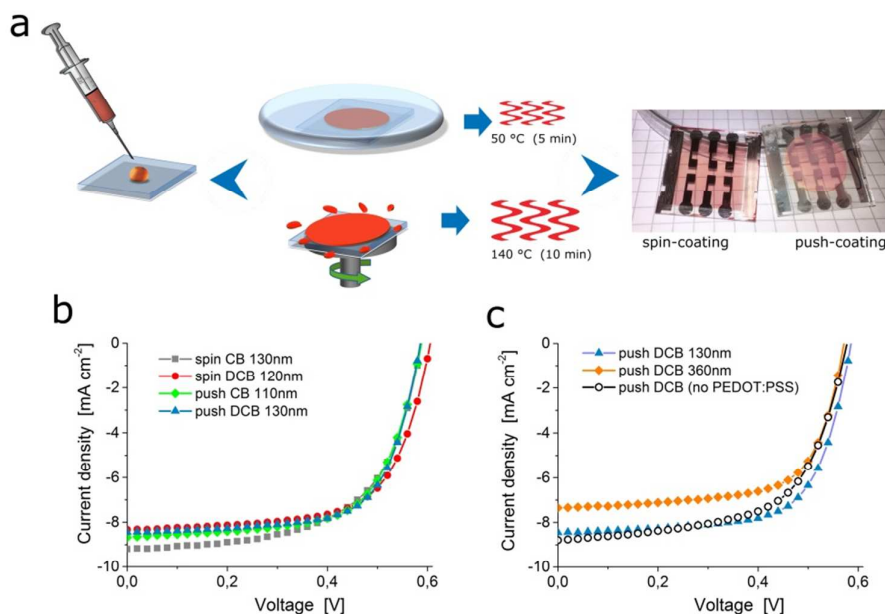
**Table 3.** P3HT crystallite characteristics in P3HT:PCBM spin-coated and push-coated films.

	$D_{(100)}^a$	$L_{(100)}^b$	$\epsilon_{rms}^c$
spin-coated (CB)	1.66	7	-
annealed at 140°C 10 min	1.63	8.5	0.04
spin-coated (DCB)	1.625	9	-
annealed at 140°C 10 min	1.60	15	0.028
push-coated (CB at 50°C 5 min)	1.59	13	0.03
push-coated (DCB at 50°C 5 min)	1.57	15	0.026

<sup>a</sup>  $D_{(100)}$  is the interplanar spacing. <sup>b</sup>  $L_{(100)}$  is the crystallite size along the (100) direction. <sup>c</sup>  $\epsilon_{rms} = (\langle \epsilon^2 \rangle)^{1/2}$  where  $\epsilon = \delta d_{(hkl)}/d_{(hkl)}$ , is the non-uniform strain, defined as root mean square of the lattice variations in the sample.<sup>35</sup>

The results on spin-coated films are well correlated with previous studies as they confirm that larger and more densely packed (shorter interplanar spacing and improved crystallite perfection, i.e. smaller  $\epsilon_{rms}$  values) P3HT crystals are obtained in thin films deposited with slower drying conditions (DCB at room temperature) as compared to CB.<sup>36, 37</sup> Note that P3HT:PCBM spin-coated films annealed at 50°C for 5 min (similarly to push-coating conditions) do not exhibit any major difference with respect to unannealed ones. However, upon annealing at 140°C, the crystalline domain size in spin-coated films increase from 7 to 8.5 nm, and from 9 to 15 nm for films deposited from CB and DCB, respectively. The push-coated films, on the other hand, readily display a high crystallinity for both CB and DCB. In fact, although push-coated films from DCB display crystallite dimensions equal to those of annealed DCB spin-coated films, the XRD measurements also reveal that they are more densely packed than the DCB spin-coated annealed films. A shorter interplanar spacing distance reflects stronger  $\pi$ - $\pi$  interactions between neighboring polymer chains and consequently, more efficient charge transport and collection (increase in FF) is expected for push-coated DCB devices compared to others. Taking into account the interplanar spacing and crystallite dimensions measured by XRD, we therefore expect to obtain increasing device FF in

the following sequence (lower to higher): spin-coated annealed CB; push-coated CB; spin-coated annealed DCB (equal or higher to push-coated CB); push-coated DCB.



**Figure 5.** Comparison between push-coated and spin-coated PSCs. a) Schematic representation of device preparation. b)  $J$ - $V$  characteristics of the spin-coated and push-coated PSCs deposited from CB and DCB. c) Comparative  $J$ - $V$  characteristics of 130 nm thick P3HT:PCBM PSCs (reference), thicker (360 nm) and simpler (no PEDOT:PSS) devices obtained by push-coating.

The device performances (**Figure 5** and **Table 4**) and, in particular, their FF, well correlate with the sequence described above. For devices with active layer thickness in the range of 110~130 nm, the average FF are 59.4, 64.6, 65.0 and 67.2 for spin-coated CB, push-coated CB, spin-coated DCB and push-coated DCB, respectively. Similarly, the PCE of the devices also follow the same trend as the crystallinity measured for the P3HT in the active layer. On the other hand, a slower drying process will not only lead to larger P3HT crystallites but also to larger donor-acceptor domains, which in turn, reduces the donor-acceptor interface area and consequently, the short-circuit current density ( $J_{sc}$ ). The open-circuit voltage ( $V_{oc}$ ) does not change

dramatically for all devices except for the spin-coated DCB devices (approximately 20 mV higher than the other devices). This may be due to a variation in vertical P3HT:PCBM concentration gradient leading to a reduction of the reverse saturation current, and consequently, an increase in Voc as observed in other similar systems.<sup>35</sup>

**Table 4.** Spin-coated and push-coated P3HT:PCBM PSC device performances.

Device type:	Jsc (mA/cm <sup>2</sup> )	Voc (mV)	FF (%)	PCE (%)
spin-coated CB (annealed, 130 nm)	9.20	590	59.4	3.23
spin-coated DCB (annealed, 110 nm)	8.34	608	65.0	3.30
push-coated CB (130 nm)	8.65	591	64.6	3.30
push-coated DCB (120 nm)	8.46	589	67.2	3.34
push-coated DCB (360 nm)	7.44	584	63.7	2.77
push-coated DCB (no PEDOT:PSS)	8.78	582	60.6	3.10

Due to this change in Voc, the increase in PCE from spin-coated to push-coated devices from DCB is of only 0.04% even though the FF increases over 2%. Furthermore, it is worth noticing that push-coated devices with thicker active layers up to 360 nm (3 times more than the commonly used active layer thicknesses in regular devices) still exhibit FF of approximately 64%, a value similar to that of annealed DCB spin-coated active layers. This suggests that non-homogeneous active layers may still display relatively high device performances which will extremely facilitate the transition from lab scale to roll-to-roll large scale device fabrication. Additionally, we have prepared push-coated DCB devices without the PEDOT:PSS hole transporting layer (which cannot be deposited using push-coating as it is deposited from water-based emulsions). These devices exhibit average PCEs of 3.1%, a value similar to that of spin-coated devices (only 5-10% lower relative PCEs). Note that removing the PEDOT:PSS layer in spin-coated devices usually results in approximately 30% reduction in PCE. Taking into account that thicker active layers and simpler device architectures can be used in push-

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3 coated devices which, furthermore, do not require any post-annealing treatment, our  
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5 devices have a great potential for the low-cost and eco-friendly fabrication of high  
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7 productivity roll-to-roll PSCs.  
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### 10 **Conclusions:**

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12 In summary, we have demonstrated that push-coating is a versatile method to  
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14 fabricate active layers for PLEDs and PSCs. In fact, unlike previous studies, our work  
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16 not only confirms that this method is applicable to many types of organic electronic  
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18 devices producing performances similar or higher than those of spin-coated devices, but  
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20 it also introduces the fact that using thicker PDMS stamps for push-coating has a variety  
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22 of advantages. The use of thicker stamps removes the necessity to engineer multilayer  
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24 stamps with nanoscale dimensions which is both complicated and time consuming. In  
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26 fact, the intrinsic mechanical and solvent diffusion properties of PDMS allow for easier  
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28 preparation and handling of the stamps which can then produce conjugated polymer-  
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30 based thin films with controllable thicknesses through push-coating. We have  
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32 demonstrated that a control over the thin film thickness can be achieved with PDMS  
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34 stamps having thicknesses of at least 3 mm. Push-coated PLEDs and PSCs were both  
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36 fabricated using volumes of solutions approximately 20 times lower compared with  
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38 common polymer layer deposition techniques (spin-coating). Considering also that  
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40 push-coating generally requires a lower polymer concentration to prepare films of  
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42 similar thickness as the spin-coated ones, the active layer material waste is remarkably  
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44 cut down and, consequently, so is the production cost. Moreover, as these layers are  
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46 usually deposited using chlorinated solvents, push-coating also considerably reduces  
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48 hazard to both environment and human health.  
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3 Our push-coated PLEDs exhibit EQEs up to 0.55% (compared to 0.35% for  
4 reference spin-coated devices) with LEs reaching values up to 2.1 cd/A (compared to  
5 1.1). Unlike spin-coated devices, the device performances of push-coated PLEDs  
6 increase with thickness which suggests that a different molecular arrangement is  
7 obtained in the thin polymer layers prepared using the two deposition techniques, as  
8 confirmed by AFM analysis.  
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17 When comparing crystallite formation and interchain interaction in  
18 P3HT:PCBM films prepared by spin-coating or push-coating, we can clearly observe  
19 that a higher degree of order is obtained for the latter. Consequently, our newly  
20 developed cost-effective and environment-friendly process allows fabricating PSCs  
21 with performances slightly exceeding those of spin-coating devices (3.30 and 3.34 % of  
22 average PCEs, respectively for spin-coating and push-coating). Although the PCEs are  
23 similar, as push-coating does not require any post-annealing process and can be used to  
24 fabricate simpler device architectures (no PEDOT:PSS) without remarkably decreasing  
25 the FF, it is an extremely promising deposition technique to produce roll-to-roll PSCs  
26 with PCEs of approximately 3% using the state-of-the-art polymer:fullerene  
27 combination materials. In conclusion, we have demonstrated that push-coating is not  
28 limited to OFETs and PSCs and, additionally, not limited to a certain number of  
29 materials but can be applied to virtually any device architecture and material provided  
30 that the solvent diffusion inside the PDMS stamp can be controlled. Therefore, our work  
31 opens the path to the fabrication of extremely low-cost electronic devices to provide  
32 displays and solar panels to everyone in both developing and developed countries  
33 around the planet.  
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