

High Temperature Etching for Threading Dislocation Investigation on GaN Epi-Layer

Ruggero Anzalone^{1,a,*}, Giuseppe Greco^{2,b}, Fabrizio Roccaforte^{2,c},
Patrick Fiorenza^{2,d}, Nicolo Piluso^{1,e} and Andrea Severino^{1,f}

¹STMICROELECTRONICS, Stradale Primosole, 50, 95121 Catania, Italy

²CNR-IMM, Strada VIII, n. 5 – Zona Industriale, 95121 Catania, Italy

^aruggero.anzalone@st.com, ^bgiuseppe.greco@imm.cnr.it, ^cfabrizio.roccaforte@imm.cnr.it,
^dpatrick.fiorenza@imm.cnr.it, ^enicolo.piluso@st.com ^fandrea.severino@st.com

Keywords: KOH etching, dislocations, high temperature, GaN

Abstract. In this work, the effect of high temperature molten KOH wet etching on GaN/AlGaN epilayer has been investigated for different family of dislocations. The high etching temperature (up to 510°C) allows a good definition of the pits, making easy the observation and the counts. Such high temperature will allow a detailed study on the statistical distribution of the dislocations on whole wafer by optical microscope for screw/mixed dislocation. A comparison on dislocation density between AlGaN/GaN structure grown on Si (111) substrate and 4H-SiC substrate has been performed.

Introduction

One of the keys for the success in the fabrication of reliable gallium nitride (GaN) -based devices depends on the ability to grow epitaxial films on substrates such as sapphire, silicon or silicon carbide, with a low density of defects [1]. In fact, the weak match in lattice parameter and thermal expansion coefficient, results in a high density (10^8 – 10^{10} cm²) of threading dislocations within the nitride film [2]. It is assumed that these defects affect the electrical performance of the devices and the optical properties of the material. For such a reason, investigating the nature of dislocations has become mandatory for GaN-based device development.

High temperature wet chemical etching is a traditionally widely used method to determine the defect density in semiconductor. For example, molten potassium hydroxide (KOH) etching, performed at temperature higher than 500°C, is a well-established method for the dislocation counting and evaluation in silicon carbide [3].

In this study, the high temperature etching effect of KOH on different GaN/AlGaN samples for threading dislocation (TD) evaluation is reported.

Experiment

In details, GaN/AlGaN layers epitaxially grown on Silicon floating zone (111)-oriented substrate and on Silicon Carbide (4H-SiC) substrate were studied. For GaN grown on Si samples, to understand the effect of the etching temperature on the dislocation, different temperatures and different etching times have been studied. The temperature was investigated from 420°C to 500°C and the times change from 30 sec to 180 sec. The short time of etching is due to the rapid etching of silicon substrate on high temperature KOH. For GaN layer grown on SiC substrate, the KOH etching was performed at 500°C for 5 minutes.

Due to the very small size of the pits, SEM or TEM and AFM analysis are the only techniques capable to observe the surface and the cross section of the samples.

Results and Discussion

In figure 1 (a and b) the SEM image of a GaN epitaxial layer grown on Silicon substrate after molten KOH etching performed for 1 minute at 420°C is reported (lower temperature investigated). To overcome the problem of very rapid etching of silicon substrate at such a high etching temperature in molten KOH, we deposited on the wafer back a Ni thin layer as sacrificial layer. With this expedient, it is possible to perform high temperature KOH etching on Si.

From literature, it was observed that, according to the Burgers vectors of TDs in a GaN epilayer, pure edge TDs are emerged into the terraces, while screw/mixed TDs are associated with the step terminations. Large etch pits exactly correspond to the step terminations, and the small etch pits always appear within the terrace [4]. Screw/mixed TDs are more readily etched and then expand into large etch pits, while edge TDs are more resistant to chemical etching. From this observation, the large etch pits originate from the screw/mixed and small ones from pure edge TDs. The origin of “very large” dislocation, which goes through the entire thickness of the GaN layer (about 2 microns), is under investigation. A plausible origin can be the deep etching of the several pits (thousand for cm²) present on the GaN surface after the epitaxial growth process and before the etching process (see figure 1c).

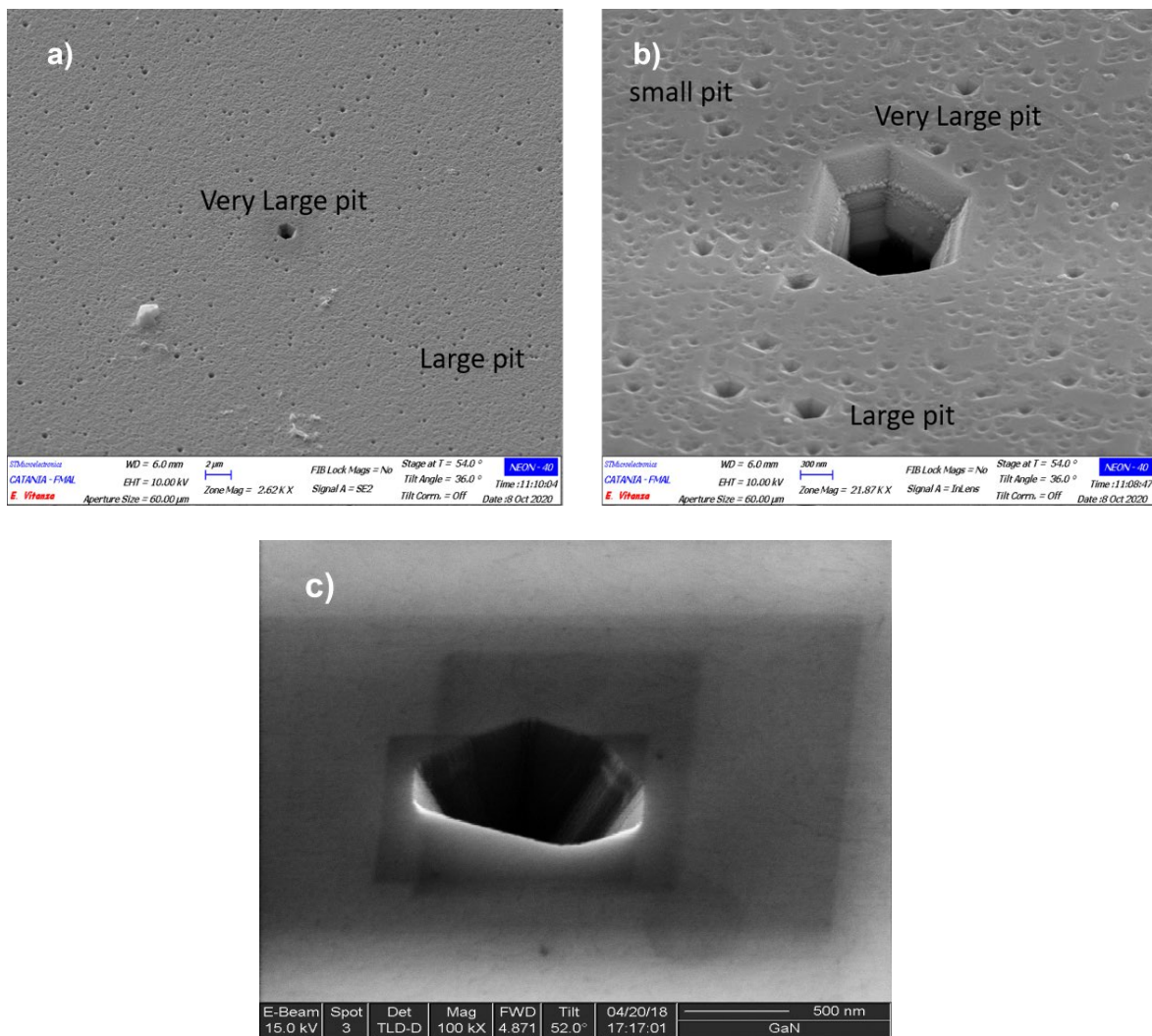


Figure 1. (a) and (b) SEM images of the GaN surface (grown on Si substrate) after molten KOH etching for 120 sec at 420°C. Three different family of pits as a function of dimension are visible. The dislocation density of the sample was evaluated about 1×10^{10} pit/cm². (c) Example of pit on GaN surface after the growth (without KOH etching).

The dislocation density of the sample reported in figure 1a was evaluated about 9.1×10^9 pit/cm², in agreement with other literature findings [5-6] using different chemistry of etching or different analysis technique.

The temperature range explored is from 420°C to 510°C and no different features were observed, except the enlargement of the “large pits” and an initial coalescence phenomenon for small pits. In this way, by increasing the time of the etching and the temperature, in the early future we will be able to have a statistical density distribution of the dislocations (at least for screw/mixed dislocation family) on whole wafer with an easy distinguishment of the large pits just by an optical microscope observation (entire 6 inch wafer will be observed). Today we are restricted only to the high-resolution techniques (SEM, TEM, AFM) that are impossible to extend to whole wafer.

The surface profile of the sample etched for 1 minute at 420°C was observed by AFM and reported in figure 2 with two different scales (5×5 micron and 20×20 micron). From the line-scan profile, the pits shown different depth and width. This is due to the different nature of dislocation as screw/mixed or pure edge TDs. The pits density evaluated from the AFM image is 8.3×10^9 pit/cm², not far from the results obtained by SEM analysis.

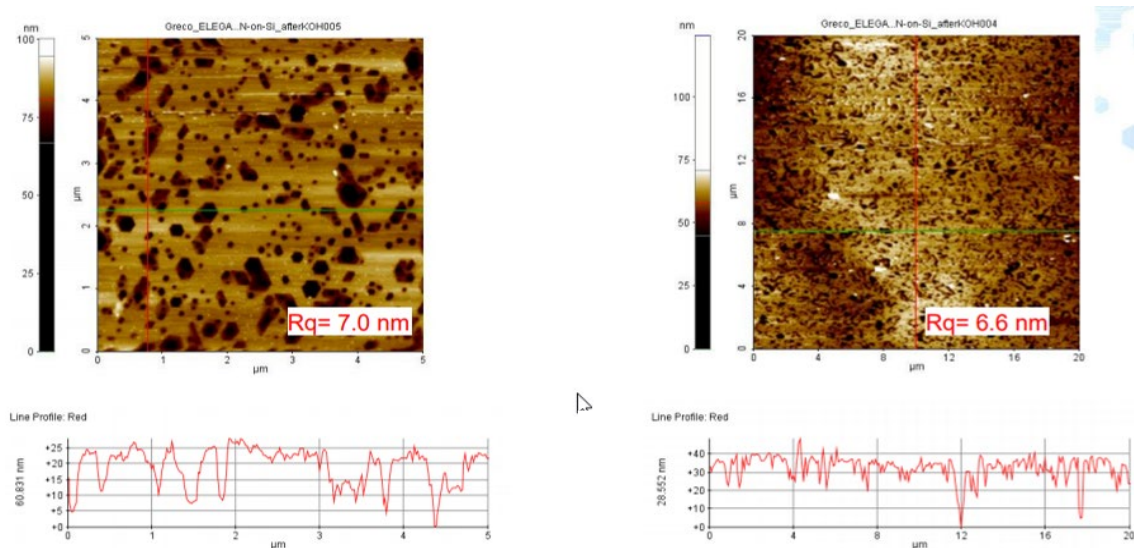


Figure 2. AFM image of the GaN surface after molten KOH etching for 120 sec at 420°C, and line scan profile of the surface (left: 5×5 μm² and right 20×20 μm²). The pits density evaluated from the AFM image is 8.3×10^9 pit/cm².

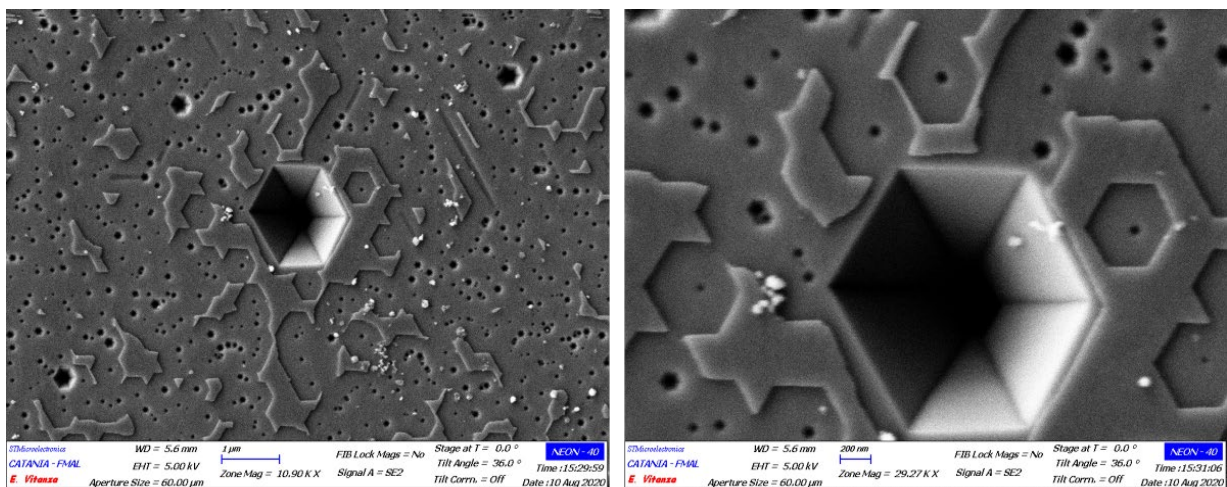


Figure 3. SEM image of the GaN surface (grown on 4H-SiC substrate) after molten KOH etching for 5 min at 500°C. Three different family of pits as a function of dimension are visible.

In figure 3, the results of KOH etching performed on GaN layers epitaxially grown on 4H-SiC are also presented. In this case, the KOH etching times was prolonged to 5 minutes and the temperature is 500°C. Also in this case, three different families of dislocations in terms of pits dimension are visible. The dislocation nature is the same of the one observed on Si substrate. The high temperature adopted makes the pits shape very well defined and easy to be counted. The dislocation density measured in GaN on SiC samples was found in the range $1-3 \times 10^9$ pit/cm², i.e. at least a factor of 3 lower than in Silicon substrate. Specifically, the AFM performed on the same GaN/SiC sample (figure 4) shows a similar profile of the one previously observed in Si, but with a lower dislocation density: around 2.2×10^9 pit/cm². The number of dislocations is quite similar to that observed with the AFM without the KOH etching of the surface (image not shown), 9.8×10^8 pit/cm².

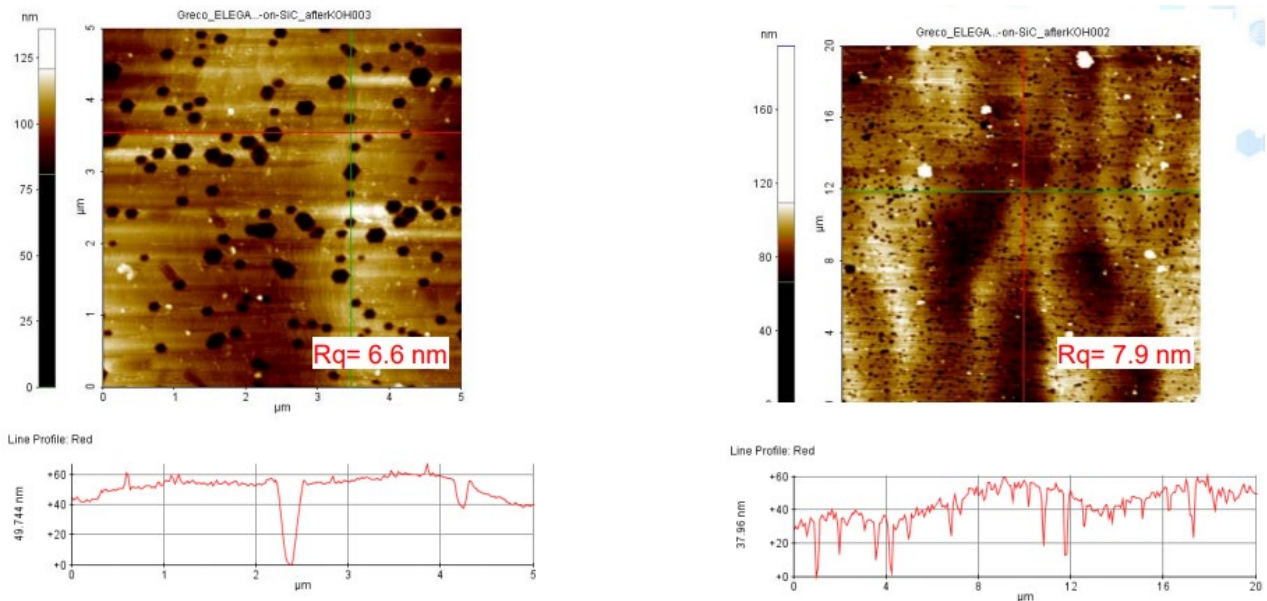


Figure 4. AFM image of the GaN surface after molten KOH etching for 5 min at 500°C and line scan profile of the surface (left: $5 \times 5 \mu\text{m}^2$ and right $20 \times 20 \mu\text{m}^2$). The pits density evaluated from the AFM image is 2.2×10^9 pit/cm².

Summary

In this work, the feasibility of high temperature molten KOH etching process on GaN sample has been shown. We compared GaN/AlGaIn layers grown on Silicon and SiC substrates, finding difference in terms of pits density. The high temperature coupled with long time etching make possible, in the early future, the implementation of optical microscope technique for whole wafer scan (6 and 8 inches) for the screw/mixed dislocation family (the large pits).

Acknowledgements

This work has been partially supported by the Italian Ministry for University and Research (MUR) in the framework of the National Project PON EleGaNTe (Electronics on GaN-based Technologies), ARS01_01007.

References

- [1] S. Nakamura, T. Mukai, and M. Senoh, *Appl. Phys. Lett.* 64, 1687 (1994).
- [2] X. H. Wu, L. M. Brown, D. Kapolnek, S. Keller, B. Keller, S. P. Den Baars, and J. S. Speck, *J. Appl. Phys.* 80, 3228 (1996).
- [3] R. Anzalone, N. Piluso, A. Severino, S. Lorenti, G. Arena and S. Coffa, *Materials Science Forum* 1662-9752, Vol. 963, pp 276-279
- [4] J Chen, J F Wang, H Wang, J J Zhu, S M Zhang, D G Zhao, D S Jiang, H Yang, U Jahn and K H Ploo. *Semicond. Sci. Technol.* 21 (2006) 1229–1235
- [5] L. Zhang, Y. Shao, Y. Wu, X. Hao, X. Chen, S. Qu, X. Xu. *Journal of Alloys and Compounds* 504 (2010) 186–191
- [6] A. Pandey, B. S. Yadav, D. V. Sridhara Rao, D. Kaur, A. K. Kapoor, *Appl. Phys. A* (2016) 122:614