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Carrot-like crystalline defects on the 4H-SiC powerMOSFET yield and reliability

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***Abstract*— The correlation between the crystalline defectiveness and the fabrication yield and reliability of 4H-SiC in vertical PowerMOSFET is mandatory in order to fine tune the life time prediction for a specific mission profile. In particular, the vertical drain leakage current at the Electrical Wafer Sorting is used usually to overlap the electrical properties and the crystalline defected. This procedure ruled out any impact of the carrot-like defects standing alone on the 4H-SiC MOSFET reliability. Carrot-like defects may play a role in the MOSFET reliability when they are combined with other crystalline or process defects.**

I. Introduction

The correlation between the crystalline defectiveness of 4H-SiC semiconductor epitaxial layers and the vertical PowerMOSFET fabricated on it is fundamental for the discrete device manufacture in terms of yield and reliability control [1,2]. The vertical drain leakage current at the Electrical Wafer Sorting (EWS) test is used to overlap the electrical properties of the device and the optically detected crystalline defected by automatic wafer inspection. This procedure allowed to correlate the electrical properties of each device containing a specific extended crystalline defect previously detected and identified by optical-based inspection techniques.

In the recent years, particular attention form the device manufactures and the scientific community has been deserved on the correlation between crystalline defects and device yield and reliability. In particular, those correlations are used to extract statistical parameters on the impact of the presence of each specific extended crystalline defect determining their so-called kill-ratio [1]. However, not exhaustive investigation are reported on the impact of the so-called Carrot-like defect.

This paper is aimed to investigate any detrimental role for the MOSFETs performances played by the carrot-like defects standing alone and which is their impact when they are combined with other crystalline defect on the device reliability in order to ensure a lifetime beyond Mission Profile Customer requirements.

II. Technology Description

In this experiment production wafers of 650 V class PowerMOSFETs devices are studied. In particular, the MOSFETs are built on 6” wafers on n-type (0001) 4H-SiC 350 µm thick substrate with a resistivity of 0.012-0.025Ω*cm. The epitaxial layer is 6 µm thick with a doping concentration of about 1×10^{16} cm^{-3}.

III. Experimental and Discussion

Optical inspections are performed using Candela 8520 by KLA-Tencor and by KLA Altair microscope during the device fabrication process steps to individuate crystalline or processing defects. The device electrical characteristics are obtained on wafers tested at Electrical Wafer Sorting (EWS) consisting in a standardized test sequence to check *the oxide integrity* (Threshold Voltage, Drain-Gate and Gate-Source Leakages); and the *vertical drain leakage currents* [Idss] at different Drain biases (50V – 320V – 520V – 650V).

Defects maps are superimposed to EWS vertical drain Leakage [idss] failure maps. In particular, it can be noticed in Fig. 1 the presence of orange labeled devices – having a Vertical Leakage current higher than 10 µA; yellow labeled devices having a EWS hard failure parameters where the gate insulator integrity is compromised. Finally, the ideal (good) devices after the EWS are also reported in Fig.1.

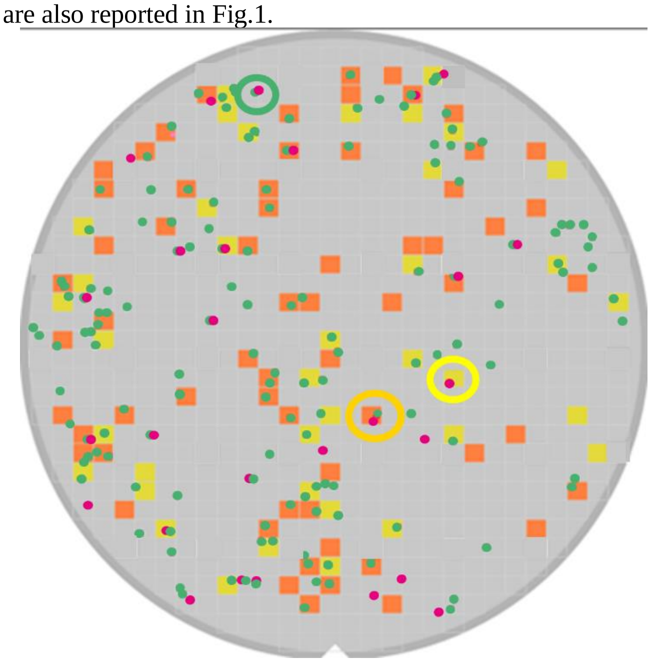
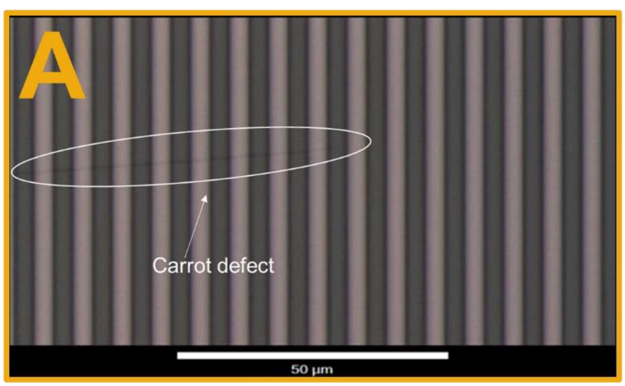


Fig.1: *Wafer level Failure Analysis (FA) map; The dots indicate optically detected defects;* ***magenta*** *indicates Carrot-Like defects;* ***green*** *indicates other epitaxial or process-related defects; Green circle – device with Carrot-like defect and EWS good; Orange circle – device with Carrot-like defect and EWS Vertical Leakage failure; Yellow circle – device with Carrot-like defect and EWS gate insulator failure.*

In the representative wafer used in this discussion, a total of 29 devices having *Carrot-Like defects* in the active area of the devices were selected. A carrot-like defect is found in 4 devices subjected to *catastrophic* failures (gate insulator integrity – yellow squares in Fig.1) and in 7 *degraded* devices suffering of high vertical drain leakage currents (orange squares in Fig.1) at EWS. Analyzing those data from a statistical point of view, a Kill-Ratio can be extrapolated. Hence, the impact of the presence of a specific extended crystalline defect linked to EWS results can estimated of ~0.4 for the Carrot-Like defect class.

The main goal of this study is to deeply investigate the type of devices named as follows: i) *Epi_Defect-EWS_Discarded* (i.e. devices with optically detected epitaxial defects discarded at EWS test having a Vertical Leakage current > 10 µA); ii) *Epi_Defect-EWS_Good*___(i.e. device with epitaxial defectiveness that successfully passed the EWS test). In particular, the focus is on those devices that passed the electrical tests (EWS good) containing the so-called *Carrot-like defect* that are definitely not affecting the device yield. Fig 2a shows a representative SEM image of an *Epi_Defect-EWS_Discarded* device having a vertical leakage current above the threshold limit (orange labeled device in Fig. 1– Vertical leakage > 10 µA). On another hand, Fig.2b shows a *Epi_Defect-EWS_Discarded* due to the insulating layer degradation (yellow devices in Fig. 1).



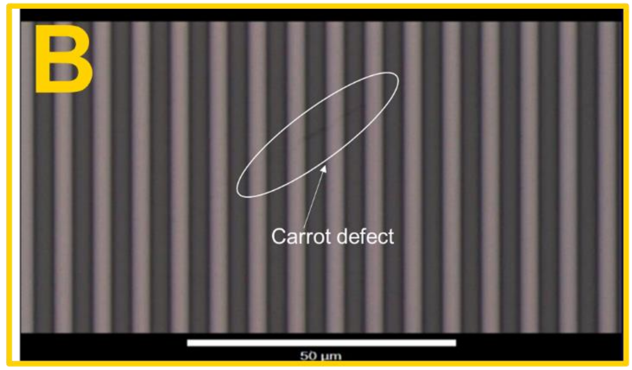


Fig.2: (a) KLA Altair image of device with Carrot-like defect and EWS Vertical Leakage fail; (b) KLA Altair image of device with Carrot-like defect and EWS oxide integrity fail.

However, the population of devices containing a carrot-like defect is not systematically discarded during the electrical tests. This demonstrates than the carrot-like crystalline defect itself cannot be responsible of the device failure. In fact, as can be seen, Fig.3 shows a typical example of an *Epi_Defect-EWS_Good* containing a carrot-like defect. Hence, it is mandatory to understand which crystalline defect or which defects combination might explain the experimental data here reported.

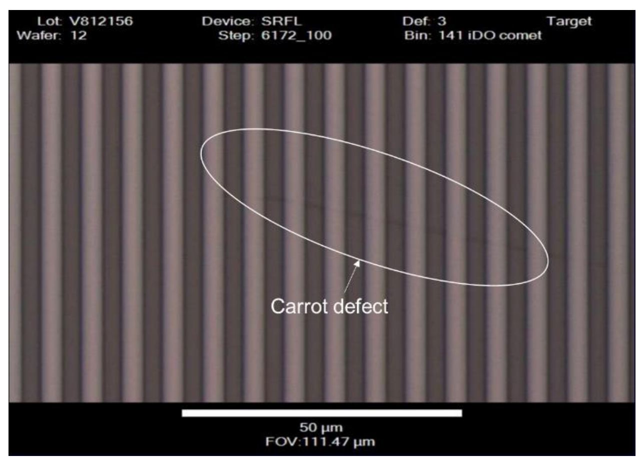


Fig3: *KLA Altair image of device with Carrot-like defect and EWS good*

The statistical information obtained overlapping the EWS data and the optically detected defects is reported in the pie distribution depicted in Fig.4.

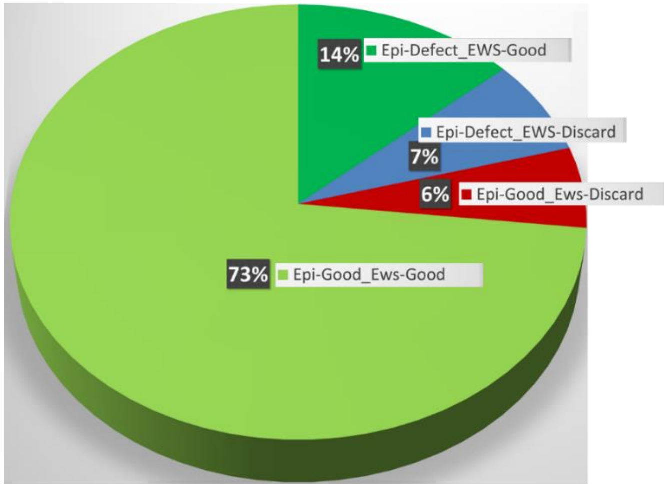


Fig.4 *Correlation between epitaxial defectiveness and EWS results: Epi_Good-EWS_Good (devices w/out epitaxial defectiveness and good at EWS test); Epi_Good-EWS_Discarded (device w/out epitaxial defectiveness and scrap at EWS test); Epi_Defect-EWS_ Discarded (device with epitaxial defectiveness and scrap devices at EWS test); Epi_Defect-EWS_ Good (device with epitaxial defectiveness and good at EWS test).*

It must be emphasized that not all the device containing an epitaxial defect are discarded. On the other hand, devices fabricated in defect-free epi-layer can be discarded at the EWS tests. Apparently, the reason behind those failure mechanisms is unclear and deserves to be fully understood. As an example, processing related defects are good candidates to explain those unexpected failures.

In Fig.5 shows the vertical drain leakages currents distributions collected at V_{DS} of 650V for the two different device families: i) without optically detected epitaxial defects (Fig. 5a); ii) devices containing a carrot-like defect (Fig. 5b). In both cases the leakage current threshold used for the EWS discard criterion is highlighted (EWS discard criterion for vertical drain current > 10 µA).

It has to be emphasized that data shown in Fig. 5a are namely related to devices without defects before any fabrication process, the leakage current may reveal if any processing related defect is created. Furthermore, Fig.5b shows a similar histogram distribution for samples containing a carrot-like defect in the device area. Hence, the carrot-like defects are not affecting the vertical leakage current distribution. In order to clarify the role of the processing related defect presence/creation and their impact on the reliability of the devices, failure analyses were performed and they will be described in the following section.

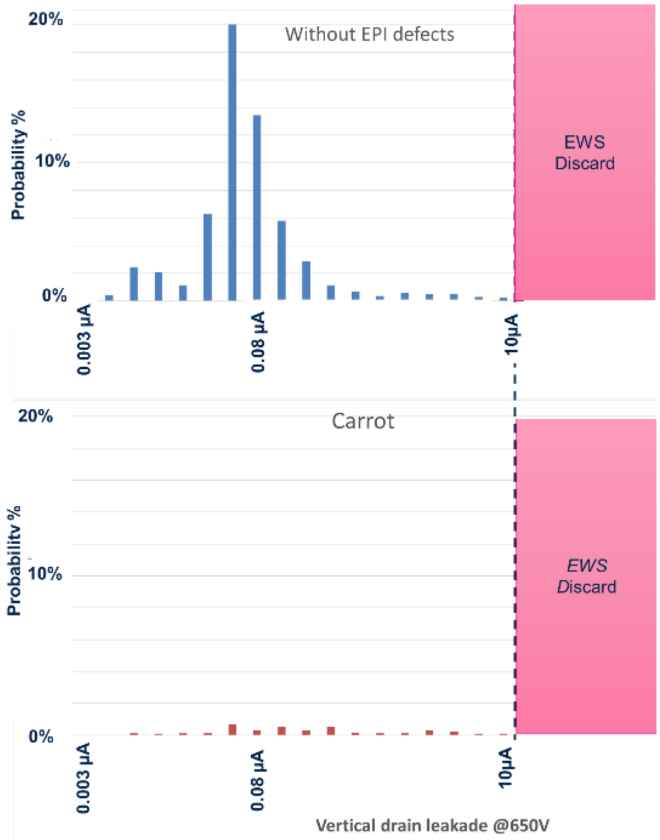


Fig.5: *Vertical Leakage distributions with (a) and w/out carrot-like defects (b).*

IV. Failure Analysis

As mentioned before, electrical test (EWS) were used to select those failed devices of interest to be investigate from a morphological point of view by means of scanning electron microscopy and focused ion beam selected are cuts (SEM and FIB) analyses. Those SEM and FIB analyses were performed in the device regions having a localized thermal emission detected by emission microscopy (Em.Mi) performed on the failed devices.

As an example, SEM and FIB failure analyses are performed on two *Epi_Defect-EWS_Discarded* as examples:

- **A:** device with Carrot-like defect and EWS Vertical Leakage failure showed in Fig.2a
- **B:** device with Carrot-like defect and EWS oxide dielectric integrity failure showed in Fig.2b

Failure Analyses on device A (Fig.6) and on device B (Fig.7) showed both a single thermal emission not coincident with the position of the Carrot-like defect.

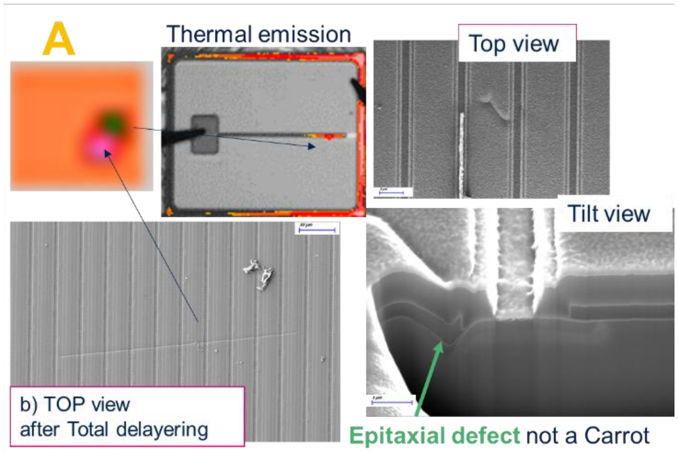


Fig.6: *An epitaxial defect (not a Carrot) has been detected. This defect is not coincident with Carrot position. A Carrot defect found in the same region detected by KLA Altair.*

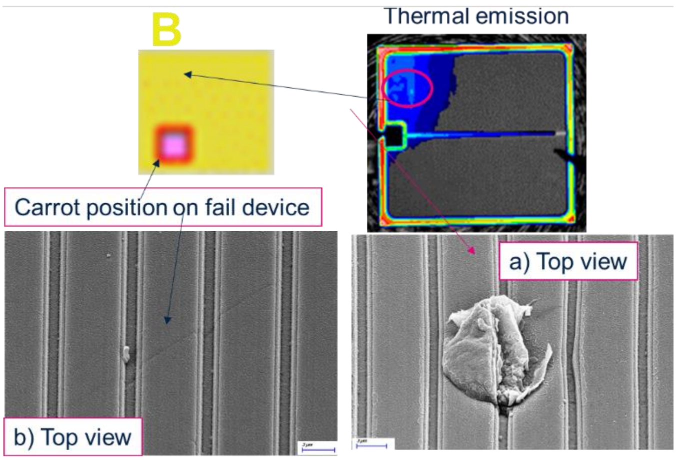


Fig.7: *A down-fall has been detected. This defect is not coincident with Carrot-like defect. (KLA Altair)*

It is important to mention that the carrot-like defect containing device usually pass the electrical test. However, those *Epi_Defect-EWS_Good* may have shown some issue at reliability tests. As an example, Fig. 8 shows the morphology of an *Epi_Defect-EWS_Good* failed during high temperature reverse bias (HTRB) accelerated stress test (V_{DS} = 600 V and T = 200°C).

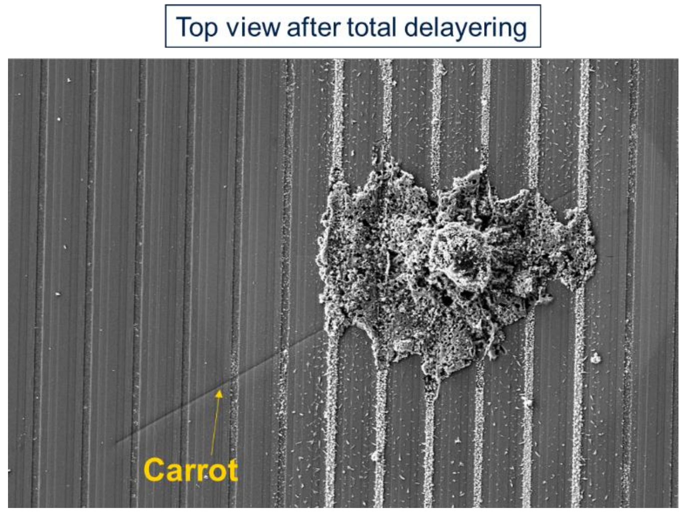


Fig.8: *An extend burn is linked to a Carrot-like defect (SEM image).*

It has to be emphasized that Carrot-like containing *Epi_Defect-EWS_Good* devices all failed beyond a typical *Mission Profile*. On the other hand, the HTRB test has been interrupted after a further half-time Mission Profile stress (50% exceeding Mission Profile stress time) because no significant variation on the failed devices were found.
In this scenario, it is mandatory to understand the physics involved in the devices failed beyond the HTRB Mission Profile test. Considering that a Carrot-like defect is contained inside all the *Epi_Defect-EWS_Good* devices under investigation, one can argue that the Carrot-like defect *per-se* is not causing the device failure under HTRB configuration. Hence, the origin of the failure mechanism of the devices containing the Carrot-like defect has to be clarified.
In order to explain which is the reason why *Epi_Defect-EWS_Good* devices passed the electrical test but suffered some reliability issue (beyond the mission profile) the following consideration can be done. A possible explanation can be given considering that carrot-like defects are often associated to other crystalline defects: i.e. threading dislocation (TD) [4]. In particular, *Hassan et al.* [4] pointed out that the carrot-like defects may have different formation mechanisms, but in all the presented models they reported the formation or the modification of a threading dislocation through the epitaxial layer that reach the semiconductor surface in the neighborhood of the carrot-like defect. In order to prove it, the device delayering is performed and the bare semiconductor surface was investigated by means of AFM.
As can be seen, AFM analyses performed on the edge of the carrot-like defect (Fig. 9) showed the presence of a peculiar triangular surface feature correlated to the presence of a TD reaching the semiconductor surface. The presence of the TDs in particular region of the elementary cell of the MOSFET were previously associated to a local shrinking of the 4H-SiC band gap inducing an enhancement of the minority carrier generation resulting in an accelerated insulating layer wear out ultimately resulting in a MOSFET reliability issue in HTRB configuration [5].

This can explain the HTRB failure statistical results. In fact, the devices having a carrot-like defect in the active area and the TD outside the device active area can survive well beyond the Mission Profile. On the other hand, when the TD associated with the carrot-like defect lays inside the active area of the device a lifetime reduction can be observed.

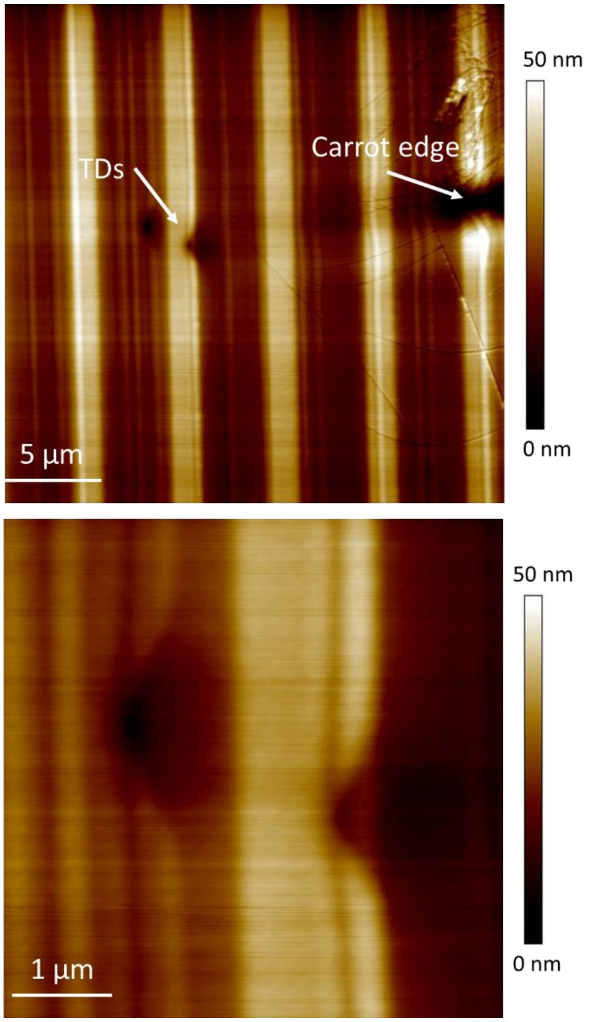


Fig.9: *AFM images collected on the edge of the carrot-like defect showed the presence of a TD*

IV. CONCLUSION

This study ruled out any detrimental role played by the Carrot-like defect standing alone in the device active area for the 650V class MOSFETs performance. Carrot-like may play a role in the MOSFET reliability when it is combined with other crystalline or process defects. As an example, when a threading dislocation associated with the carrot-like defect lays inside the active area of the device a lifetime reduction can be observed. This allowed to conclude that Carrot-like defect class shows no impact on EWS Yield Loss (~ 0%). In fact, the vertical leakage currents distribution of devices passing the EWS test and containing a carrot-like defect are perfectly superimposed with defect-free devices classified good after the EWS test.

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