Direct growth and size tuning of InAs/GaAs quantum dots on transferable silicon nanomembranes for solar cells application

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Abstract

In this paper we show for the first time the possibility to direct grow and tune the size and optical properties of high quality InAs/GaAs quantum dots on transferable crystalline silicon nanomembranes. The transferable silicon nanomembranes have been grown via in-situ H_2 prebake of porous silicon in Ultra High Vacuum Chemical Vapor Deposition UHV-CVD reactor. Flat and continuous transferable crystalline nanomembranes with thicknesses below 30 nm have been obtained. The mechanical strain in the silicon nanomembranes has been tuned via sintering temperature between 900 and 1100 °C for the direct crystalline growth of transferable InAs/GaAs (QDs)/Si foils. The size and band gap energy of these InAs/GaAs quantum dots are tuned via strain engineering in silicon nanomembranes. Several advanced techniques such as Scanning Electron Microscopy (SEM), High Resolution Transmission Electron Microscopy (HR-TEM), X-Ray Diffraction (XRD), Photoluminescence (PL) spectroscopy are used to investigate the structural and optical properties of transferable silicon

nanomembranes and the grown InAs/GaAs QDs. High quality InAs/GaAs QDs with tuned sizes grown on flat and continuous transferable crystalline nanomembranes have been obtaind. The obtained results have shown that this novel process allows the growth of well separated InAs/GaAs QDs with well defined shape, high density around $2x10^{10}/cm^2$ and a well controlled size variation as function of the substrate strain between 2 and 10 nm.

The high quality of the structural and optical properties of the InAs/GaAs QDs monolithically grown on a transferable Si nanomembranes and its compatibility with standard Si solar cells technologies offer a great opportunity for growing a cheap and high performance InAs/GaAs quantum dots/Si third generation solar cells and microelectronic devices.

Keywords

III-V-on-silicon integration; Sintered porous silicon; solar cells; ELTRAN.

Introduction

The current worldwide energy production is highly dependent on the fossil resources, such as oil, natural gas and coal. Factors, like the possible scarcity of nonrenewable resources, climatic changes, economic development and population growth are rapidly consuming natural resources, which make evident the need to develop new energy generation methods provided from renewable resources. Photovoltaic solar energy is one of the best solutions in terms of availability, profitability, non-polluting to meet future energy demand compared to classical fossil sources [1].

Photovoltaic energy technology can be classified into three generations. The first generation photovoltaic cells are characterized by solar cells based on single p-n junction of crystalline silicon wafers that are not flexible, expensive and heavy. It is also associated with a great amount of residues produced as well as by high energy consumption for its production [2]. The second generation is related to the assembly of thin films. Devices are based on films of copper, gallium diselenide (CIGS) and cadmium telluride (CdTe) indium as well as thin layers of

amorphous silicon (a-Si). Some problems related to the high toxicity of specific materials, such as cadmium, limit their use on a large scale [3-4].

Quantum dots cells make up the future 3rd generation of photovoltaic solar cells [5-7]. The insertion of quantum dots or nanoparticles, such as TiO_2-coated SiO_2 nanoparticles, CdS QDs, in 3rd generation photovoltaic (PV) cells can increase the energy conversion rate of cells by up to around 60% [8-12]. The reason is that quantum dots have completely different properties from the bulk matter, in particular higher gap energies related to the quantum confinement phenomenon and few non-radiative defects, unlike quantum wells [13-15].

Many classes of semiconductor quantum dots, including groups II-VI, III-V, IV-VI, IV, and their alloys, such as isolated quantum dots of InP, PbS, PbSe, Si, Ge, PbTe and CdTe, have been proposed for application in future generation photovoltaic cells to enhance their conversion efficiencies [15-17]. Also the growth of InAs/GaAs QDs represents a very promising way for high performance 3rd generation solar cells fabrication [18, 19]. Although the direct growth of these materials on cheap nominal silicon substrate now is possible thanks to growth process development, the production of epitaxial III-V/Si foils using a porous Si-based layer transfer process for high-efficiency solar cells has not yet been realized. Therefore, this paper fills this gap. Hence, we develop and tune the physical properties of heated porous silicon substrates, which are widely used in the fabrication of the standard silicon cells (Si p-n junction) via layer transfer process (LTP) and epitaxial layer transfer (ELTRAN) for the monolithic integration of III–V materials on the transferrable silicon nanomembranes formed at the top of heated porous silicon. We will show that the stress-induced structural defects, leading to the formation of non-radiative defects commonly observed during the direct epitaxial growth of GaAs on nominal Si (001), can be accommodated and fully inhibited by the high elasticity and flexibility of the heated porous silicon layers. [20-22] In addition to the compliant nature of the heated porous silicon substrates, the transfer of the epitaxial InAs/GaAs QDs layer

grown on heated porous silicon via LTP and ELTRAN to another low cost substrates, such glass or plastic substrates, and keep the rest of the heated porous substrate for reuse, is also possible. In this case, the double-layers porous silicon substrate, with two porous layers with different porosities, is formed on a p-type silicon substrate by electrochemical anodization and is sintered at solid state via H_2 bake at high temperature in a ultra high vacuum chemical vapor deposition (UHV-CVD) reactor. During the H_2 bake, the upper porous Si layer with low porosity transforms into a transferable Si nanomembrane via thermal surface smoothening and this formed continuous Si layer serves as seed for the epitaxial growth of active layer of solar cell. The large pores of the bottom porous Si layer transform into a brittle like-sponge silicon layer and this layer serves for the detachment of the grown layer from the original silicon substrate after the epitaxy step [23-25]. The new proposed process for the fabrication of low cost solar cells with III-V nanostructures via epitaxial layer transfer and layer transfer process is schematically presented in Figure 1.

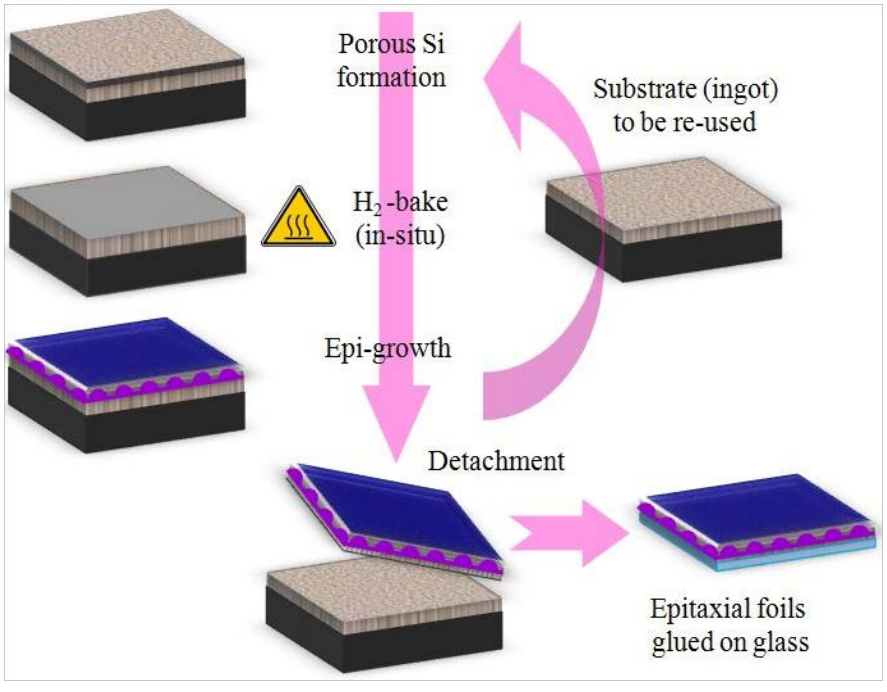


Fig. 1: Scheme of the proposed porous Si-based LTP and ELTRAN process applications for III-V Nanostructures-on-Si photovoltaic cells.

In this paper we demonstrate the possibility of replacing the growth step of Epi-silicon layer during classical LTP or ELTRAN process by the direct growth of InAs/GaAs QDs layers with tuned band gap energies for 3rd generation solar cells. This innovation is based on the exploitation of the high structural properties of the heated porous silicon for the integration of III-V nanostructures, such as InAs/GaAs QDs on Si and its compatibility with the standard silicon solar cells platform for the production of transferable foils of InAs/GaAs QDs for 3rd generation solar cells via Epitaxial Layer Transfer (ELTRAN) or layer transfer process (LTP).

Experimental details

The double-layer porous silicon substrates were fabricated by electrochemical anodization of p-type silicon substrates (100) with resistivity 10^{-2} Ω cm^{-1}. The electrochemical attack is carried out in a HF solution leading to varying porosities depending on the current density, the anodization time and the HF concentration. Two layers of different porosities were made by varying the parameters of chemical attack during etching process. The low porosity layer is formed at the top to facilitate the thermal growth of the transferable silicon nanomembrane via solid-state sintering, which serves as a seed for the epitaxial growth of photovoltaic cell, and the high porosity layer is formed at the bottom to facilitate the detachment and the transfer of the active layer during LTP. We have tested different combinations of double-layer porous Si with different porosity (ρ), thickness and different sintering degrees, in order to obtain sintered porous silicon substrates with optimal structural features adequate for successful direct growth of III-V semiconductors quantum dots on Si. To do this, we have optimized the current density, the anodization time, the HF concentration and the sintering temperature in order to control the strain and the morphology of the heated porous Si. Typical double-layer porous Si substrates characterized by a low porosity layer (20%), about 400 nm thick, at the top and a high porosity layer (35 %), about 7 µm thick, at the bottom have been fabricated according to the following steps: the first step is the formation of the low porosity layer (ρ = 20%) using an anodizing

current density of 5 mA/cm^2 and a concentration [HF] = 35% of the anodizing solution. The second step leads to the formation of the high porosity layer (ρ = 35%) using an anodizing current density of 80 mA/cm^2 and the same HF concentration of the anodizing solution. Then an ultra thin crystalline Si nanomembrane, adequate for crystalline growth, is formed at the top of the porous layer via solid-state sintering step. The sintering process is done by heating the porous silicon substrates at high temperature (in the range 900°C -1100 °C for 30 s under hydrogen gas) in an industrial ASM Ultra High Vacuum Chemical Vapor Deposition (UHV-CVD) reactor. The variation of the heating temperature is used to tune the strain in the porous layers via sintering degree in order to control the strain in GaAs buffer for InAs QDs size tuning. [25, 27]

After the high-temperature sintering step, the strain evolution in porous silicon layers versus heating temperature has been studied by X-Ray Diffraction (XRD) using Panalytical X'Pert Pro X-Ray diffractometer and the morphological properties have been studied using a Philips XL30 SFEG SEM Scanning Electron Microscope (SEM). Three sintered porous silicon substrates, with different strain values, have been selected for the growth of InAs QDs and labeled: PSi-900°C, PSi-1000°C and PSi-1100°C.

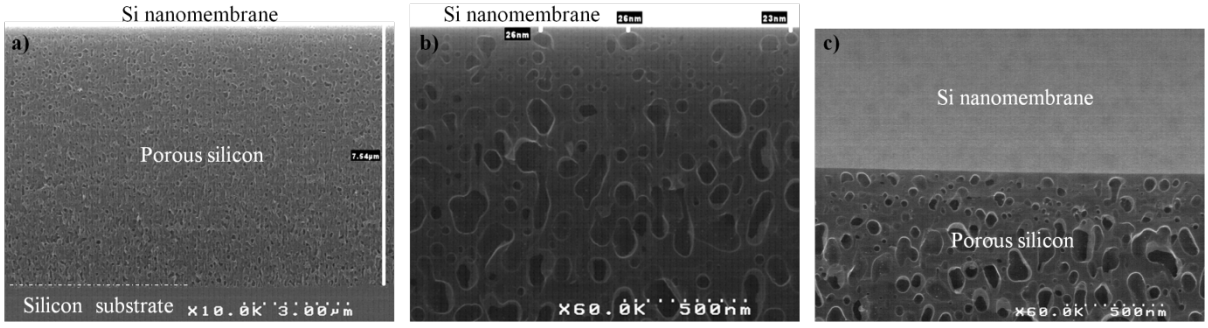
The epitaxial growth of the InAs QDs on the porous silicon substrates was carried out according to the following steps: first the heated PSi substrates undergo a Shiraki cleaning adapted to porous silicon substrates and an in-situ out gassing process at 540°C in a ultra high vacuum Molecular Beam Epitaxy reactor (Riber 32) with a background pressure of 10^{-11} Torr in order to obtain a perfect clean surface. Second, we grow a 50 nm GaAs buffer layer on the heated porous silicon substrates at 580°C using Solid Sources Molecular Beam Epitaxy SSMBE; then the InAs quantum dots are grown via Stranski-Krastanov mode by depositing three monolayers of InAs at 500 °C. The morphological changes of the surface during 2D - 3D transition, which accompanies the formation of the InAs QDs, were observed during growth step by reflection

high-energy electron diffraction (RHEED). The morphological and the structural properties of the grown InAs QDs were determined using Park XE-150 type Atomic Force Microscopy (AFM) and Jeol 2000FX type High Resolution Transmission Electron Microscopy (HRTEM) operated at 250 keV. The photoluminescence emission spectra of InAs QDs were measured by exciting with the 496,5 nm line of an Ar-ion laser. Raman spectra were obtained at room temperature (RT) via a micro-Raman system.

Results

1. Strain engineering in silicon nanomembranes for III-V-on-Silicon Integration

Figure (2-a) shows a SEM image, taken at low magnification, of the typical heated porous silicon substrate and displays the homogenous porosity and thickness of the porous layers; the thickness, measured by SEM, is around 7.54 μm. Figure (2-b) shows a high magnification SEM image taken near the surface of the porous layer of the same sample: the tiny pores of the upper low porosity layer and the flat continuous silicon nanomembrane grown at the top of porous silicon substrate during the heating step are clearly visible; the average thickness of the nanomembrane is ~ 25 nm. Figure (2-c) displays a SEM image taken at 45° tilt for the heated porous silicon top layer showing the perfect morphology and flatness of the pore-free silicon nanomembrane grown at the top of porous silicon substrate via sintering process.



Figure(2): (a) SEM image of the heated porous silicon substrate; (b) high magnification SEM taken at the top of the heated porous silicon substrate showing the sponge-like porous morphology; (c) SEM image taken at 45° tilt for top layer of heated Porous Silicon illustrating the perfect morphology of the surface.

In order to investigate the structural qualities of the formed silicon nanomembrane that will be used as a crystalline seed layer for the epitaxial growth of transferrable InAs/GaAs QDs/Si foils for photovoltaic cells and optoelectronic devices, we performed High Resolution Transmission Electron Microscopy (HRTEM) investigations on all samples. Figure (3-a) shows a low magnification TEM image of the typical heated porous silicon: both the low-porosity and high-porosity porous silicon layers are visible and we can distinguish between them by the difference in contrast. Figure (3-b) shows a high magnification TEM image near the top of the sintered porous silicon layer displaying the upper porous layer (with the formed flat silicon nanomembrane at the top) and a part of the lower high porosity layer. The shape and the size of the pores are visible. In the inset of fig. 3b it is shown the selected area electron diffraction (SAED) pattern of the heated porous silicon layers which confirms its perfect crystallinity. Figure (3-c) shows a high magnification HRTEM image, taken near the surface of the sintered porous silicon, which confirms the formation of a defects-free crystalline nanomembrane.

The high structural and morphological properties of the heated porous silicon surface, as well as its mechanical softness, make it a suitable seed for the hetero-epitaxial growth of high performance solar cells.

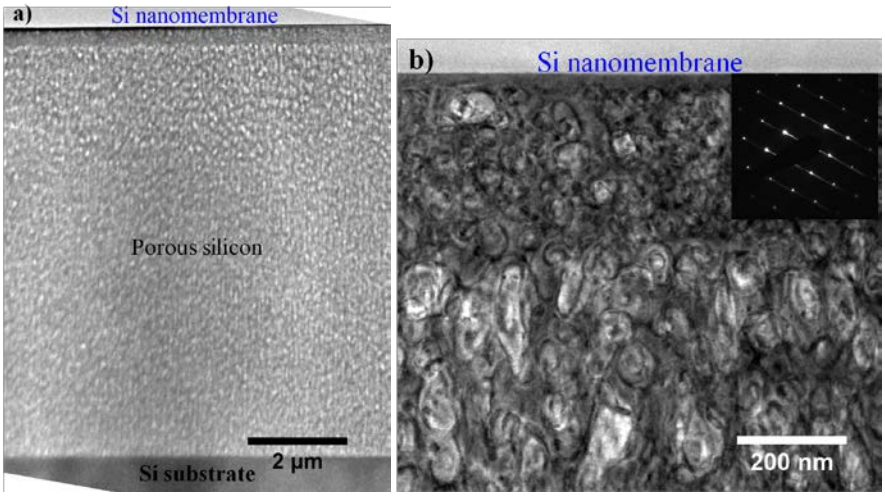


Figure (3): (a) Cross sectional TEM image of a heated porous silicon layer after H_2 prebake step ; (b) high magnification TEM image taken at the top of the heated porous silicon substrate showing the fine porous morphology inset electronic diffraction pattern illustrating the crystallinity of the heated porous silicon layer; (c) high magnification HRTEM image of the silicon nanomembrane. thermally grown at the top of the heated porous silicon layer, showing the high structural properties of the surface.

In addition to the morphological and structural changes in porous silicon layers induced by the high temperature heating during in-situ sintering process, heating porous silicon at high temperature can affect also the internal strain in the porous layers and change it from the tensile strain to compressive strain during the sintering process of the porous silicon substrates. The value of the nascent compressive strain essentially depends on the heating temperature. Several previous theoretical and experimental studies have been done on the internal strain change in sintered porous silicon during heating temperature [27]. In order to study the strain evolution (so to control it for tuning InAs QDs sizes), we performed Omega-2Theta scans around the (004) XRD on these samples using Panalytical X'Pert Pro X-Ray diffractometer with a six-axis sample stage on high resolution goniometer and absolute angular resolution equal to 0.0001 degrees. A typical XRD profile is reported in Fig. 4 and it can be fit with 2 different contributions, one corresponding to the Si substrate and the other one to the sintered porous Si layer.

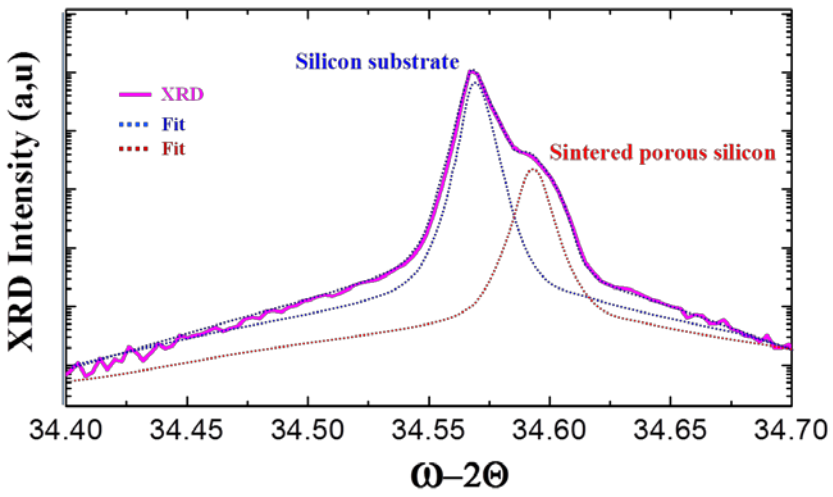


Figure (4): XRD pattern of a porous silicon substrate heated at 900°C for 30 s under H_2 ambient in UHV-CVD reactor fitted with 2 gaussian curves.

By increasing the temperature from 900 to 1100 °C during the sintering step in H_2 environment, the angle peak associated to the sintered porous layer shifts from higher angle towards the Si-peak, indicating an out-of-plane compressive strain relaxation (see Figure 5a). This relaxation is correlated to the increase of the sintering degree of porous Si. The relative contraction $\Delta a/a$ in the heated porous layer lattice with respect to the relaxed silicon substrate is proportional to the angular splitting $\Delta\theta_B$ between the two XRD spectrum peaks: $\Delta a/a = -\Delta\theta_B \cot \theta_B$, where θ_B is the Bragg's angle [27-29]. Fig 5b displays the evolution of the compressive strain occurred in porous silicon during the sintering process as a function of the heating temperature: this compressive strain is associated to the porosity decrease versus heating temperature, until the full relaxation of the heated porous layers occurs.

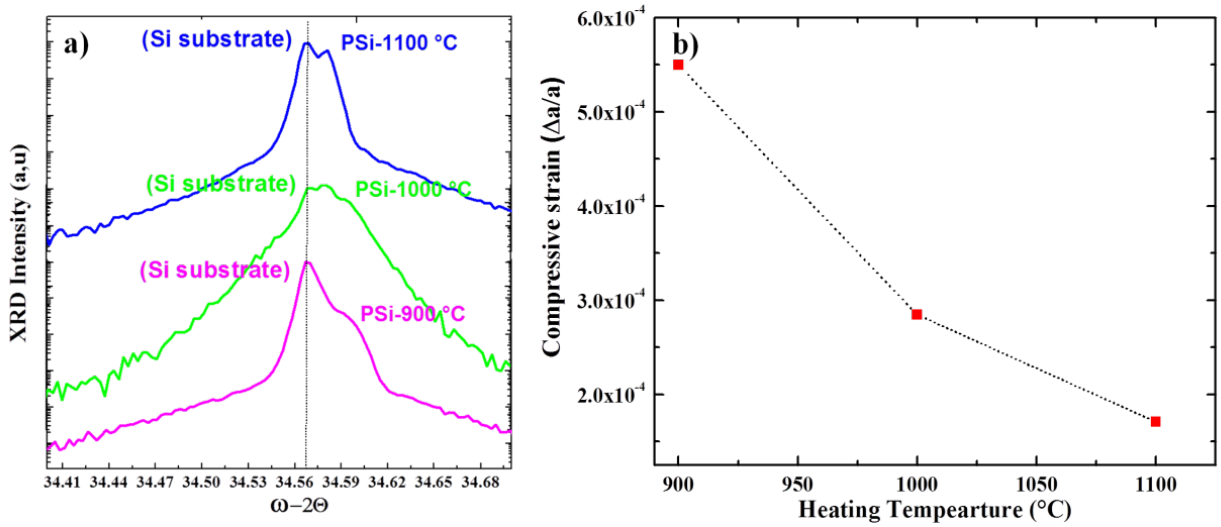


Figure (5): (a) X-Ray Diffraction profiles of in-situ sintered PSi. The shift of PSi-peak toward the Si-peak is attributed to a decrease of internal strain with heating temperature that may be correlated with the increase of the porous Si sintering.(b) Out-of-plane compressive strain evolution of the in-situ heated double layers of PSi. The strain of the heated PSi double layers relaxes at high temperature heating.

2. MBE Growth of InAs/GaAs quantum dots

After the formation of heated porous silicon substrates with high morphological qualities and controlled strain well suitable for epitaxial growth of nanostructures and LTP or ELTRAN technologies, we have exploited theirs high morphological and structural qualities for the monolithic growth of InAs/GaAs QDs to produce a cheap InAs/GaAs QDs/Si foils for high performance solar cells. Figure (6) displays the evolution of the RHEED patterns observed during the crystalline growth step confirming the transition from a two-dimensional to a three-dimensional growth after the epitaxial deposition of 3 monolayers of InAs at 500 °C and the formation of InAs QDs via Stranski-Krastanov.

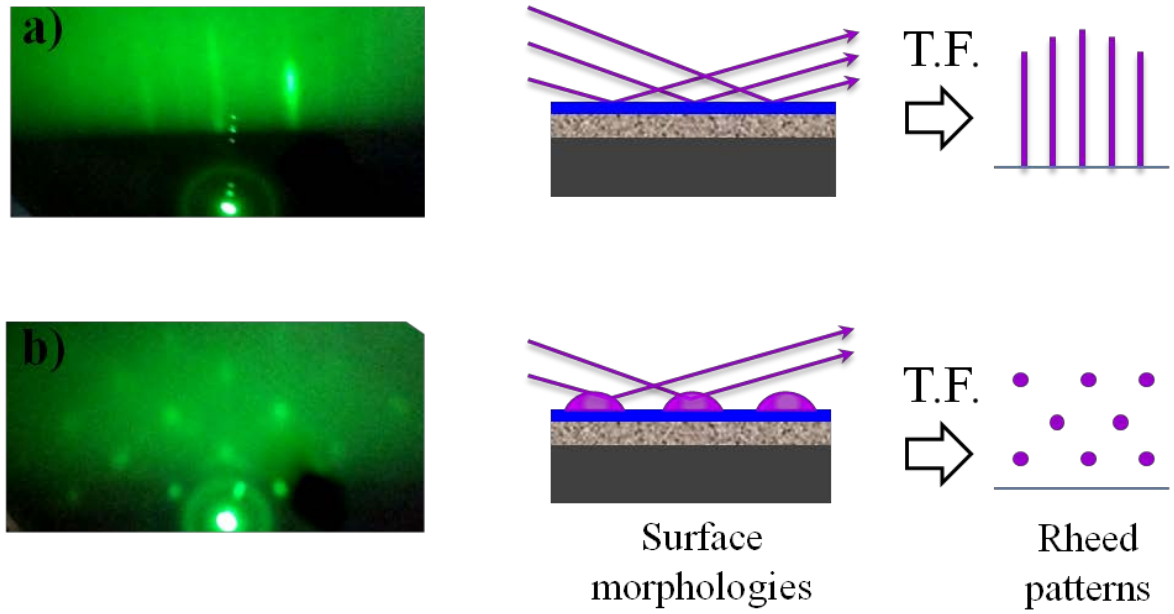


Figure (6): (a) RHEED patterns of GaAs buffer layer and (b) of the InAs QDs after the growth step with schematic explanations of the origin of their shapes.

After the growth process, we have investigated the morphological properties of the uncapped InAs QDs using Atomic Force Microscopy (AFM) in order to measure the density and size of the InAs quantum dots. Figure 7 shows AFM images of high densities InAs QDs randomly grown on different heated porous silicon templates after depositing a 40 nm GaAs buffer layer in the same growth conditions. From the analysis of the AFM images (7-a, 7-b, 7-d, 7-e, 7-g and 7-h) we have extracted the size distributions of the quantum dots for each sample and they are reported in the figures (7-c, 7-f, 7-i). The shape of the histogram curves reveals a low dispersion in the quantum dots sizes and a mean size that increases with increasing the temperature of the porous silicon annealing before the deposition.

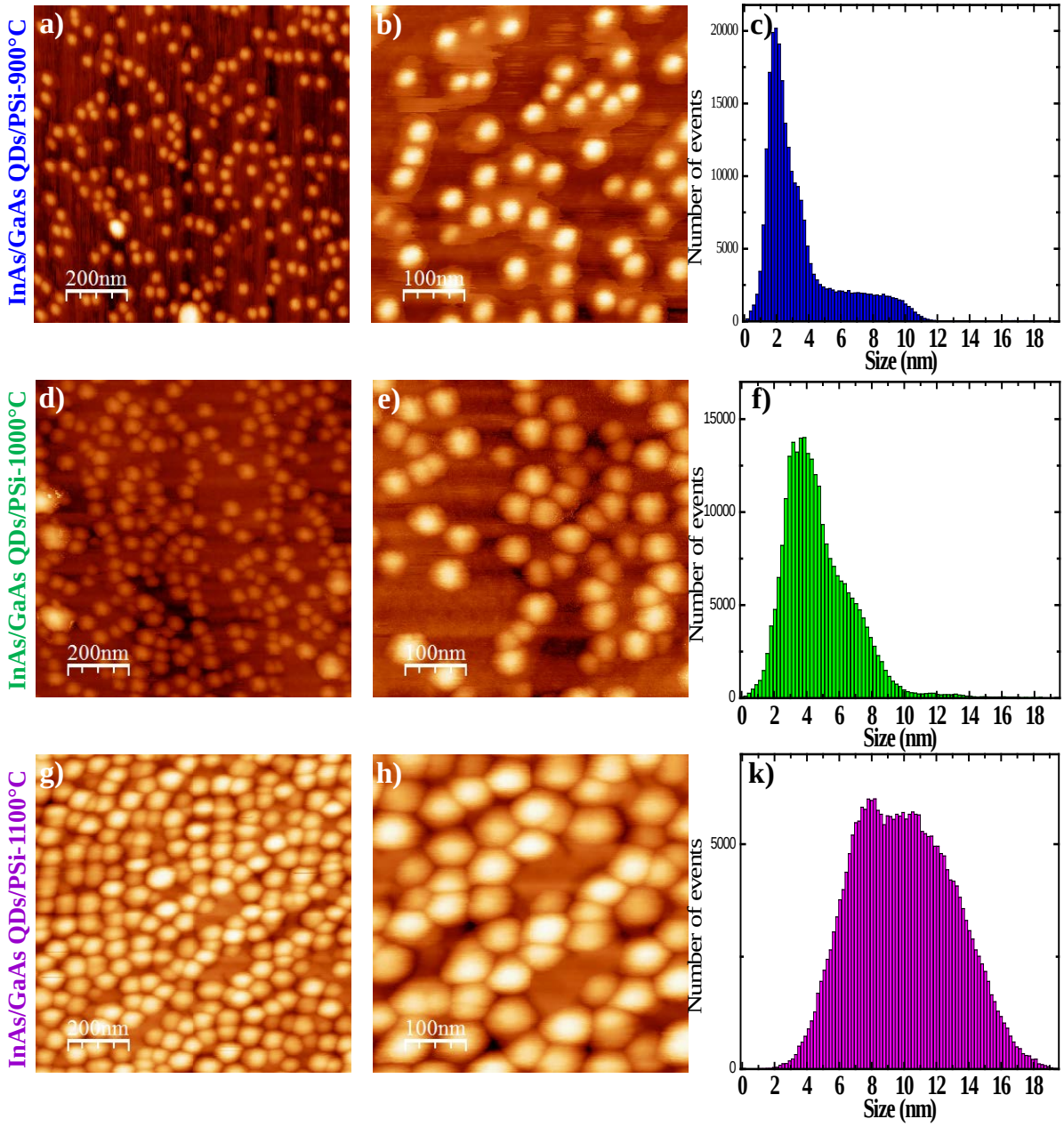


Figure (7): (a,d and g) respectively shows AFM images at low magnifications of InAs QDs grown on PSi-1100 °C, PSi-1000 °C and PSi-900 °C; (b,e and h) respectively shows AFM images at high magnifications of InAs QDs grown on PSi-1100 °C, PSi-1000 °C and PSi-900 °C and (c,f,i) respectively shows size distributions of InAs QDs /PSi-1100 °C, InAs QDs /PSi-1000°C and InAs QDs /PSi-1100 °C extracted from the AFM images.

Figure 8-a and 8-b show, respectively, the evolution of the size and of the densities of InAs QDs as a function of the sintering temperature of the porous silicon substrates. There is a clear evolution of the size and the density with the sintering temperature and therefore with the compressive strain in the porous Si layers. These results demonstrate the possibility to directly

grow InAs/GaAs QDs on heated porous silicon and control their size and densities via internal strain of the substrate.

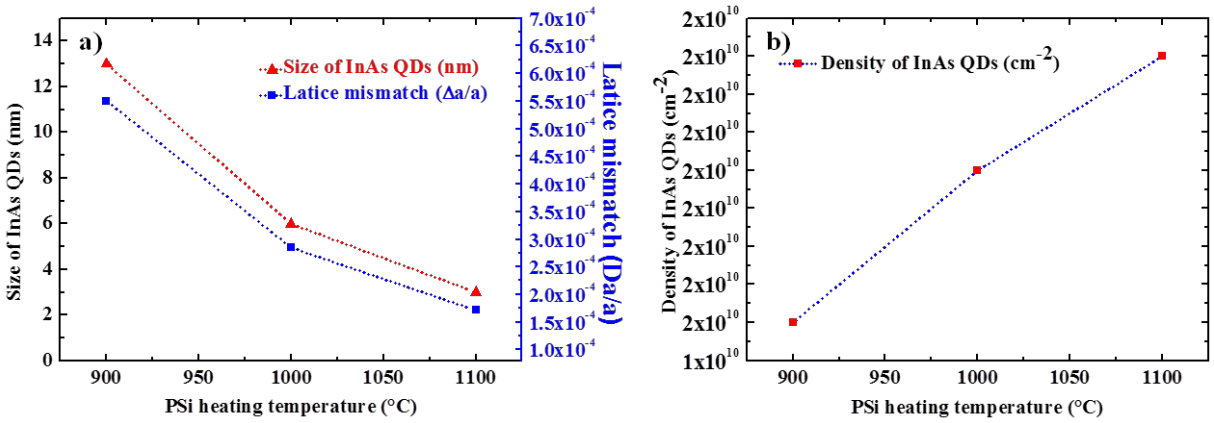


Figure (8): (a) evolution of the size and of the lattice mismatch and (b) of the density of InAs QDs as a function of the porous Si heating temperature.

The good structural and mechanical properties of the heated porous silicon substrate make it a suitable low cost compliant template for the direct growth of InAs/GaAs QDs, contrary to the other compliant substrates used in the literatures, such as patterned substrates which require the deposition of a thick buffer layer to relax the mismatch stress [29, 30]. In addition to these structural and mechanical properties of the new proposed low cost heated porous Si substrates for the III-V/Silicon integration at large-area, these substrates also allow to fabricate free-standing monocrystalline III-V/Silicon nanostructures foils for high performance photovoltaic cells, via application of the LTP or ELTRAN process on the structures.

To obtain more information about the strain engineering effects on the physical properties of the novel grown nanostructures, we have investigated the strain evolution in these samples via Raman spectroscopy operated at room temperature. Fig. (9-a) displays the Raman spectra of InAs/GaAs QDs grown on heated porous substrates with different internal strain values. The spectra are characterized by a Raman peak at 253 cm^{-1} attributed to Raman scattering of InAs QDs and 2 Raman peaks related to the GaAs buffer layer: the first one at 266 cm^{-1} is due to scattering of TO phonons and the second one at 291 cm^{-1} is attributed to the LO phonons

scattering. Fig 9-b shows the Raman spectrum of InAs/GaAs QDs with a zoom in the region from 250 to 275 cm^{-1}. The peak has been fitted with two Gaussian peaks, one centered at 266 cm^{-1} (due to GaAs buffer layer) and the second at 257 cm^{-1} (due to InAs QDs). Thanks to the compressive strain in the GaAs buffer layer caused by the residual stress in the silicon nanomembranes, the Raman peaks shift to a lower wavenumber and confirms the strain effects of the sintered porous silicon substrates on the morphological and optical properties of the InAs/GaAs QDs (see fig. 9c).

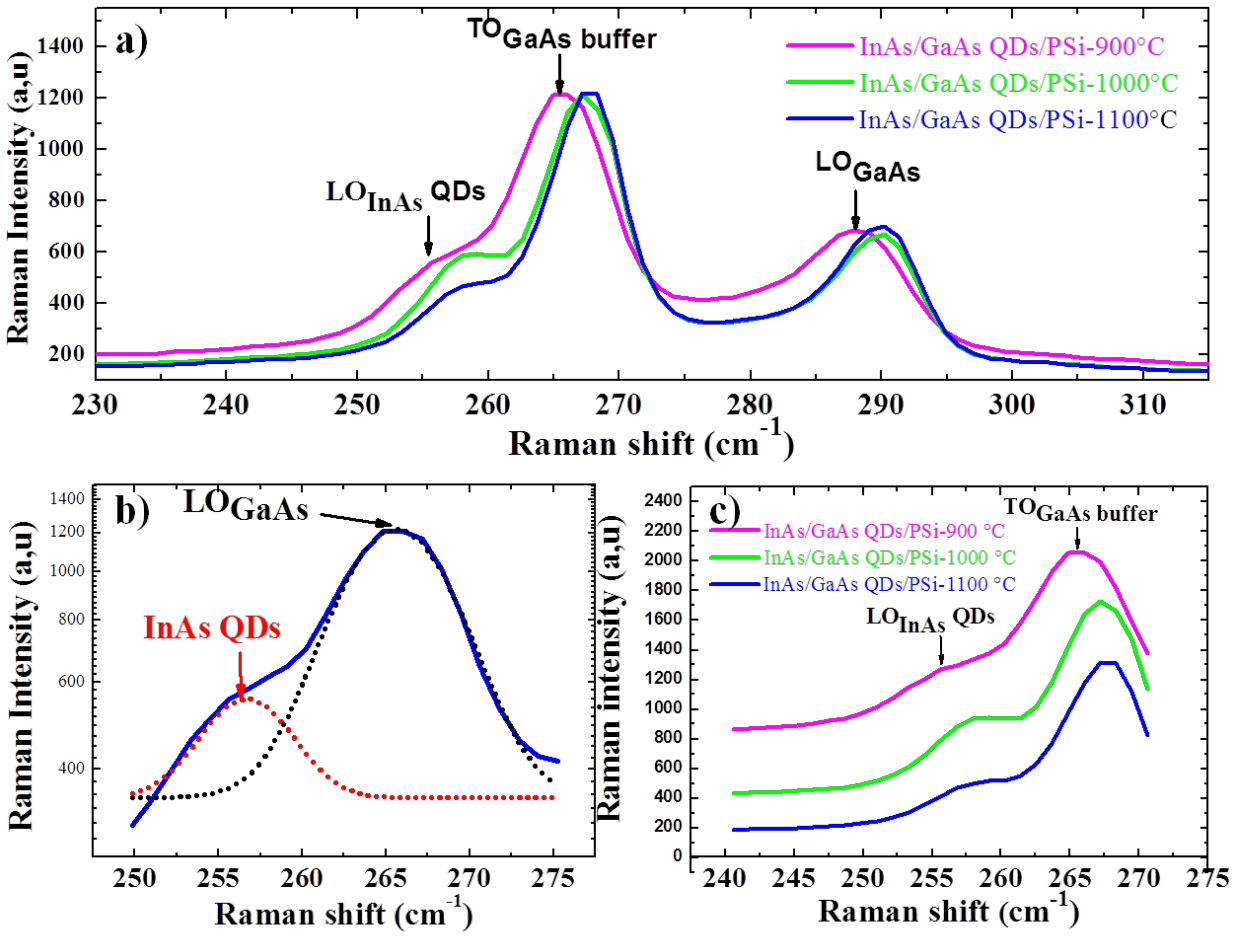


*Figure (9): (a) Raman spectra of InAs quantum dots grown by MBE on the transferable Si nanomembranes. (b) Zoom of the Raman spectrum of typical InA/GaAs QDs/PSi-*900 °C), *fitted with 2 gaussian curves. (c) Zoom of the Raman spectrum displaying the progressive Raman shift.*

Figure 10-a shows the photoluminescence (PL) spectrum of InAs QDs measured at 11 K under argon laser excitation (line: 496.5 nm). The bright emission spectrum is centered at 1.05 eV and it is the result of several different contributions. We have fitted the PL spectrum with 4 gaussian peaks, having a full width at half maximum (FWHM) of about 35 meV. The narrow width at half-height of the sample PL spectrum is due to the well self-organization of InAs QDs in the structure. The energy difference between two successive peaks is roughly the same and ranges between 30 and 70 meV. The origin of these peaks is the fluctuation of height of quantum dots by monolayers which are confirmed by structural studies.

In order to characterize the spatial location of carriers within the quantum dots, a temperature-dependent photoluminescence study is appropriate.

The evolution of PL spectra as a function of temperature is shown in Figure 10-b. We notice a low variation in the PL intensity between 11 and 300 K which proves a strong confinement effect and spatial localization of carriers within the quantum dots.

Figure 10-c shows the variation of the integrated photoluminescence intensity of InAs QDs as a function of the reciprocal temperature. We observe that the integrated PL intensity at 11 K is about 25 times higher than at 300 K. The observed decrease in photoluminescence above 80 K can be explained by the thermal activation of the carriers towards the wetting layer or towards the GaAs buffer barrier.

We can fit the curve of the integrated PL intensity as a function of the reciprocal temperature (Figure 10-c) with the following equation:

$$I_{PL}(T) = I_0 / (1 + A * \exp(-E_a / kT)) \qquad [31]$$

where E_a is the activation energy from the fundamental level of quantum dots.

From the fit we were able to extract that $E_a \approx 106$ meV. We then assume that the thermal activation of carriers outside the InAs QDs occurs through excited states towards the wetting layer or towards the GaAs barrier.

Figure 10-d shows both the PL peak position and the FWHM as a function of temperature. We observe that by increasing the temperature, the peak position slightly shifts towards the low energies, confirming the good optical quality of InAs QDs. The FWHM remains slightly constant which indicates the high uniformity of the InAs QDs. These results, which are in good agreement with data already reported in the literature, prove the optical efficiency of these InAs/GaAs QDs [32].

On other hand the strain produced by the lattice mismatch between GaAs and InAs represents the driving force for the formation of QDs via the S-K growth mode and the most important variable which affects the different features of quantum dots, such as size and density. Therefore the control of the strain in the GaAs buffer layer led to a relative control of InAs QDs size and their optical properties. Figures 10-e and 10-f show Raman shift and energy band gap evolution as a function of the internal strain in silicon nanomembranes that are used as seed layers for the growth of InAs/GaAs quantum dots. We observe that, by increasing the compressive strain, the position of the Raman peaks related to GaAs buffer layer slightly shifts towards the low wavenumbers and the energy band gap of these QDs shifts towards a lower energy. This red shift is attributed to the InAs QDs size increase.

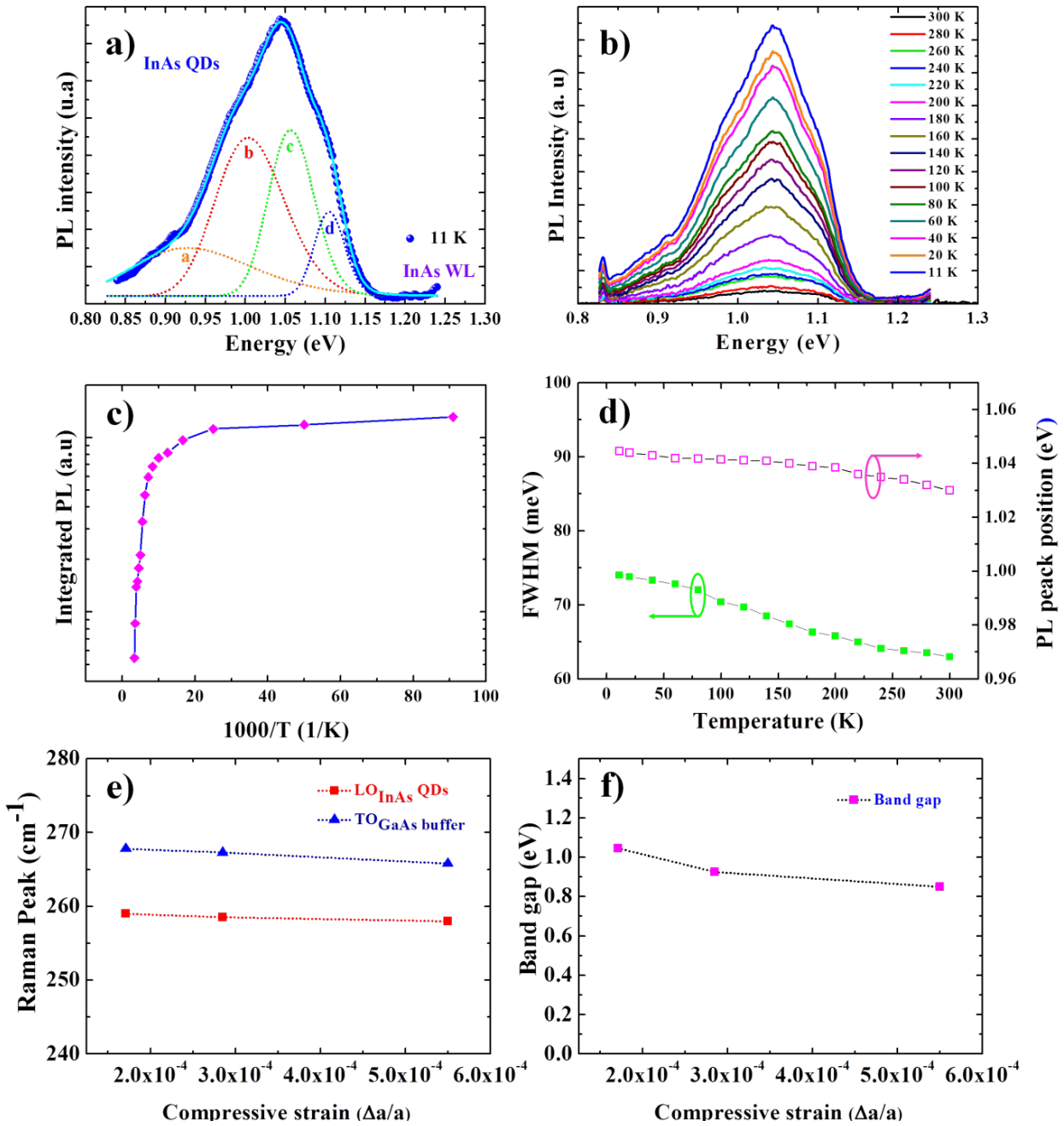


Figure (10): (a) Photoluminescence spectrum of the InAs/GaAs quantum dots grown on heated PSi substrate measured at 11 K. The PL spectrum has been fitted with four gaussian curves; (b) PL spectra measured at different temperatures between 11 and 300 K; (c) Evolution of the integrated PL intensity as a function of the inverse of the temperature; (d) temperature dependence of the PL FWHM and peak position ;(e) Raman shift as a function of the internal strain in sintered porous Si layer;(f) Energy bandgap as a function of the internal strain in sintered porous Si layer.

The good morphological, structural and optical results clearly demonstrate that the heated porous silicon can be used as a cheap compliant substrate for monolithic integration of III-V on Si, via the growth of only a few tens nanometers of GaAs buffer layer, contrary to the methods recently used for the direct growth of InAs/GaAs QDs on nominal silicon substrates, that requires the use of a thick GaAs layer to progressively plastically relax the mismatch stress. In addition to the compliant nature, the novel proposed heated PSi substrate allows also to tune the size and optical properties of QDs via internal strain in porous silicon substrates.

Conclusions

Nanoporous silicon substrates with homogenous pores and thickness haves been formed via electrochemical etching. Flat and continuous transferable crystalline nanomembranes with high structural quality and tunable strain have been thermally grown on top of a nanoporous silicon substrates via in-situ solid-state sintering process at high temperature (900°C -1100 °C) in H_2 ambient. The compliant nature and the high flatness of the crystalline nanomembranes have been exploited for direct molecular beam epitaxial growth of InAs/GaAs quantum dots on silicon. The tunable strain in nanoporous silicon has been optimized via heating temperature and exploited for tuning the sizes and band gap energies of InAs/GaAs QDs. Several advanced characterization techniques, such as AFM, TEM, Raman and PL spectroscopies have been combined to investigate the structural, morphological and optical properties of the heated porous silicon samples and of the InAs/GaAs QDs grown on the transferrable silicon nanomembranes. In addition to the well-reported structural and morphological properties of all the samples, our.

The obtained InAs/GaAs QDs samples exhibit high structural, morphological and optical properties at room temperature. These results indicate that the heated porous silicon, which is considered a cheap seed for homo-epitaxy of free-standing single crystalline foils for photovoltaic cells, can be used for the monolithic integration of III-V semiconductors on silicon

and to produce InAs/GaAs QDs on silicon foils for cheap and high performance 3rd generation solar cells and microelectronics devices.

The well morphological, structural and optical results clearly demonstrate that the heated porous silicon can be also used as a cheap compliant substrate for monolithic integration of III-V on Si, via the growth of only a few tens nanometers of GaAs buffer, contrary to the methods recently used for the direct growth of InAs/GaAs QDs on nominal silicon substrates, that requires the use of a thick GaAs layer to progressively plastically relax the mismatch stress. In addition to the compliant nature of the new proposed heated PSi substrate for the III-V/Silicon integration, it allows to fabricate large-area free-standing monocrystalline InAs/GaAs QDs foils for solar cells via application of the layer transfer process on the structure.

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