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Modeling and Experimental Validation of a Voltage-Controlled Split-Pi Converter Interfacing a High-Voltage ESS with a DC Microgrid

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Abstract: The Split-pi converter can suitably interface an energy storage system (ESS) with a DC microgrid when galvanic isolation is not needed. Usually, the ESS voltage is lower than the grid-side voltage. However, limitations in terms of the ESS current make the use of a high-voltage ESS unavoidable when high power levels are required. In such cases, the ESS voltage can be higher than the microgrid voltage, especially with low microgrid voltages such as 48 V. Despite its bidirectionality and symmetry, the Split-pi exhibits a completely different dynamic behavior if its input and output ports are exchanged. Thus, the present work aims to model the Split-pi converter operating with an ESS voltage higher than the grid-side voltage in three typical microgrid scenarios where the controlled variable is the converter's output voltage. The devised state-space model considers the parasitic elements and the correct load model for each scenario. Furthermore, it is shown that the presence of the input LC filter can make the design of the loop controllers more complicated than in the case of a lower ESS voltage than the grid-side voltage. Finally, the study is validated through simulations and experimental tests on a lab prototype, and a robustness analysis is performed.

Keywords: Split-pi; bidirectional converter; energy storage system; droop control; feed-forward control; DC microgrid

1. Introduction

The growing interest in DC electrical microgrids has triggered a renewed interest in power electronics, specifically in the devices and circuits enabling the correct interfacing of a DC bus with distributed generation units, energy storage systems (ESSs), and passive or active loads. In particular, bidirectional DC/DC converters used to interface ESSs with DC buses are considered crucial due to the manifold beneficial effects of ESSs on DC microgrids [1,2]. In fact, ESSs play a key role in providing the needed flexibility to maintain the stable operation of the microgrid. Furthermore, they improve the system's robustness and resiliency by compensating for the intermittency of renewable generation, providing ramping support to generators, and acting as backup power sources. Finally, ESSs ensure a power buffer that can be leveraged to apply suitable energy management strategies to the microgrids by defining the optimal power flows according to the chosen objectives [3–5]. For example, the minimum electricity bill, the maximum efficiency, or the minimum load demand uncertainty can be pursued. In addition, bidirectional DC/DC converters are also increasingly employed in other applications, such as uninterruptable power supplies and electric vehicles [6].

The simplest bidirectional DC/DC converters are non-isolated and are obtained by replacing the unidirectional switches of the basic DC/DC converter topologies with bidirectional switches. Additional degrees of freedom can be achieved with isolated topologies

based on high-frequency transformers (HFTs), where the turn ratio of the HFT can be used to adjust the boosting capability of the converter. In such structures, the galvanic isolation between the input and output ports of the converter provides the circuit with increased safety. The most popular isolated bidirectional DC/DC converter is the Dual Active Bridge (DAB) converter [7,8]. It is based on two full-bridge circuits, each of which is placed on one side of the HFT. This converter is particularly suited to high-power applications. Recent studies also put in evidence the good attitude of the DAB in providing an active current limitation in case of a short circuit at the output terminals. This capability is of the utmost importance in DC microgrids, where the design of an appropriate protection system remains a significant challenge so far [7,8].

Most of the current research on circuit topologies for bidirectional DC/DC converters is focused on minimizing weight, volume, losses, and cost and on enhancing power density and reliability using wide-bandgap (WBG) semiconductors. In addition, recent research has mainly focused on topologies that are inherently scalable and modular [9]. From this point of view, non-isolated bidirectional DC/DC converters are interesting since they can provide benefits in terms of efficiency, size, weight, cost, and modularity [5,7].

Reference [7] presents an exhaustive overview of DC/DC bidirectional converters. Besides reviewing both non-isolated and isolated configurations, the most relevant control schemes and switching strategies were analyzed for both converter categories. The need for designing highly efficient and reliable soft-switching strategies was highlighted. Furthermore, whenever applicable, the combination of pulse width modulation (PWM) with single-phase shift control was suggested to limit current stress, circulating currents, and conduction losses. Such a combination can also expand the range of the zero-voltage switching (ZVS) operation.

In [9], a comparative analysis was conducted to assess the suitability of several single-phase non-isolated bidirectional DC/DC converters to be used in DC microgrids with multiple ESSs. The study focused on power sharing among distributed generation units by using droop control to equalize the state of charge (SOC) of multiple ESS architectures in both charging and discharging modes. Several topologies (e.g., single-stage and cascaded buck-boost, buck-boost with tapped inductors, and SEPIC) were investigated and compared in terms of DC voltage regulation, discharge current, SOC discharge rate, and number of active/passive circuit components. In addition, extensive reviews of non-isolated bidirectional DC/DC converter structures were presented in [5,10]. The studies included converter classifications based on efficiency, simplicity, cost, and flexibility. Moreover, the half-bridge topology with coupled inductors (including the related interleaved variants) was identified as the most promising topology from the efficiency and robustness standpoints.

Among the non-isolated bidirectional DC/DC converters, the Split-pi recently emerged as a noteworthy option. This converter is based on two cascaded half-bridge converters (HBCs) with a common bulk capacitor, as shown in Figure 1. It can work in four operating modes, which depend on the relationship between the voltage at the input and output ports and the power flow direction, according to Table 1. As a matter of fact, there are not many papers on the Split-pi available in the literature [11–24]. In particular, refs. [11–18] analyzed various aspects of the Split-pi topology and its open-loop control, showing that this converter features high efficiency like the DAB but also exhibits reduced switch count, smaller reactive components, and suitability for multiphase systems.
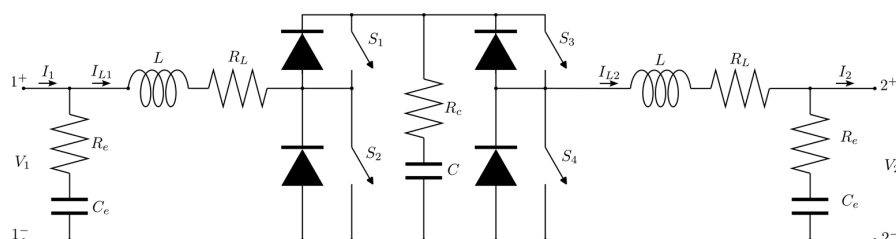

Figure 1. Schematics of the Split-pi converter.

Table 1. Operating modes of the Split-pi converter.

Mode	Voltage Relationship	Power Flow Direction
1	$V_1 \leq V_2$	port 1 $\to$ port 2
2	$V_1 \leq V_2$	port 2 $\to$ port 1
3	$V_1 > V_2$	port 1 $\to$ port 2
4	$V_1 > V_2$	port 2 $\to$ port 1

On the other hand, only six papers studied the performance of the Split-pi under a closed-loop control [19–24]. In particular, ref. [19] focused on the regulation of the internal bulk capacitor's voltage and [20,21] regulated the output voltage of the converter connected to a passive load, whereas [22] controlled the power flow in a Split-pi connected to a microgrid with stiff voltage regulation.

A more extensive study was performed in [23,24] to show how to correctly model and control the Split-pi used as an ESS converter operating in Modes 1 and 2 in all the five possible DC microgrid scenarios. Such scenarios stem from the combination of the nature of the active load of the ESS converter and the three possible control modes for the converter itself. On the one hand, the ESS converter can be controlled to behave either as a non-stiff voltage generator, a stiff voltage generator, or a current generator under the supervision of an energy management system (EMS). On the other hand, the DC microgrid can or cannot encompass droop-controlled voltage generators in addition to current generators and passive loads.

Although [23,24] considered the Split-pi operating in Modes 1 and 2, the operation in Modes 3 and 4 (i.e., with ESS voltage higher than grid-side voltage) is also possible. For example, using a high-voltage ESS (i.e., above 200 V) is unavoidable when high power levels are required because of the limitations in terms of the ESS current that arise from technical and safety considerations. In such a case, the ESS voltage can be higher than the microgrid voltage, especially with low microgrid voltages such as 48 V.

Given the bidirectional and symmetrical nature of the Split-pi, in the first place, it could seem that exchanging the relationship between the voltages of the ESS and the DC bus (i.e., considering Modes 3–4 instead of Modes 1–2) does not imply any modification with respect to the configuration studied in [23]. Instead, as will be shown in Section 2, the Split-pi converter exhibits a different dynamic behavior if its input and output ports are exchanged. This result is counter-intuitive considering the bidirectionality and symmetry of the converter, and it implies a more complicated design of the converter controllers and a more limited bandwidth. Thus, it is worth being investigated in detail.

The present work considers the same Split-pi converter as in [23,24]. However, the voltage levels of the ESS and the DC microgrid are exchanged, i.e., the Split-pi is supposed to interface a 180 V, 750 W storage system with a 48 V DC microgrid. Thus, the converter is operated in Modes 3–4. The study is performed in three of the five possible DC microgrid scenarios, i.e., those in which the controlled variable is the converter's output voltage rather than the output current. A state-space model of the converter is devised considering the parasitic elements and the correct load model for each scenario. The study is validated performing simulations and experimental tests on the same prototypal Split-pi described in [24]. The obtained experimental results are coherent with the simulations and validate the study. Finally, a robustness analysis is performed, and the limitations of the proposed converter are discussed.

The paper is structured as follows. Section 2 clearly highlights the differences between the operation in Modes 1–2 vs. Modes 3–4 and recalls the case study, the DC microgrid scenarios, and the closed-loop control scheme. Section 3 describes the state-space model of the Split-pi operating with an ESS voltage higher than the grid-side voltage and the design of the control system. The simulations and experimental tests are described and commented on in Sections 4 and 5, respectively. Section 6 presents a robustness analysis and discusses the limitations of the proposed converter. Finally, some conclusions are drawn.

2. Comparison between Operation in Modes 1–2 vs. Modes 3–4 and Overview of Previous Work

In this section, the differences between the Split-pi operation used as a storage converter with the ESS voltage lower or higher than the grid-side voltage are clearly highlighted. Then, the case study, the possible DC microgrid scenarios, and the closed-loop control scheme are briefly recalled from [23].

2.1. Comparison between Operation in Modes 1–2 vs. Modes 3–4

It is possible to refer to Figure 2 to understand the reason for the different behavior of the proposed storage converter in Modes 1–2 vs. Modes 3–4. Indeed, for power flowing from the high side to the low side (i.e., in Modes 2 and 3), the converter is characterized by the same topology: an LC filter followed by a buck converter. Such a filter is formed by the high-side inductor and the bulk capacitor. Likewise, for power flowing from the low side to the high side (i.e., in Modes 1 and 4), the Split-pi always behaves as a boost converter followed by an LC filter formed by the high-side inductor and the high-side capacitor.
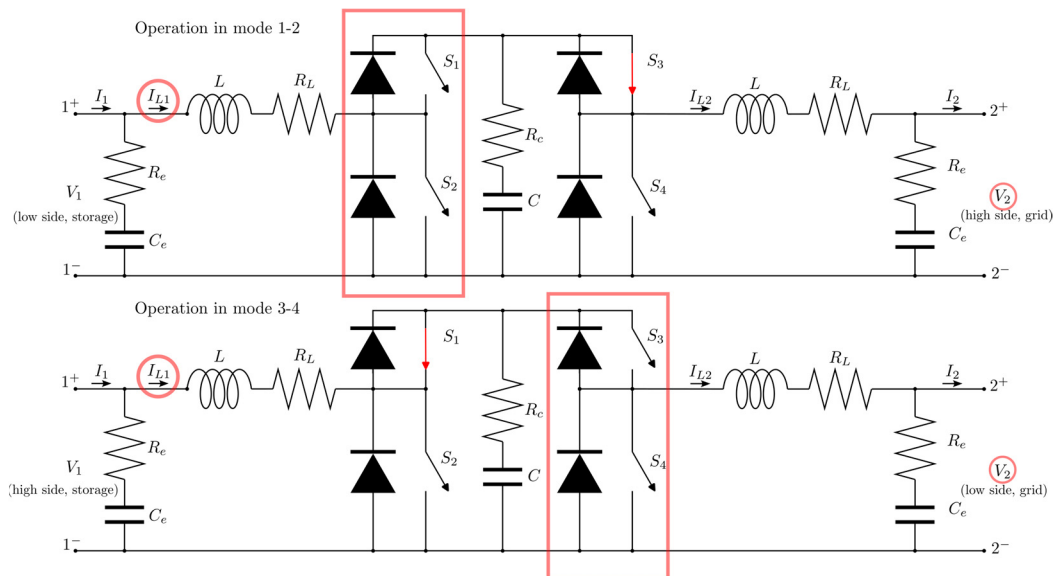

Figure 2. Comparison between operation in Modes 1–2 and 3–4 of the bidirectional Split-pi converter.

However, further reasoning highlights a substantial difference that makes the storage converter's state-space model different from the one devised in [23]. A perfect symmetry would imply also exchanging the controlled variables I_{L1} and V_2 with I_{L2} and V_1, respectively. In this condition, the state-space model would not change. However, this exchange is not possible since the goal for a storage converter is to control the output voltage (to perform grid voltage regulation) and the storage current (to keep it within the limits recommended by the manufacturer). As will be shown in Section 3, not exchanging the controlled variables results in a different state-space model of the converter.

Specifically, in Mode 1, the inner control loop regulates the boost converter's input current, whereas the input current of the LC filter (formed with the high-side capacitor) is controlled in Mode 4. Likewise, in Mode 2, the inner control loop regulates the current on the inductor of the buck's output filter (formed with the low-side capacitor). On the other hand, in Mode 3, the inner control loop regulates the current on the LC filter formed with the bulk capacitor located before the buck converter.

As will be shown in Section 3, if the resonance introduced by the latter filter is poorly damped, the design of the controllers becomes more complicated than in the case of the Split-pi operating in Modes 1–2, and a more limited bandwidth can be achieved.

2.2. Overview of the Case Study

The chosen case study is a Split-pi converter interfacing a 180 V, 750 W battery storage system with a 48 V DC microgrid encompassing passive and active loads. For example, it could represent a scaled version of the DC microgrid onboard an unmanned marine vehicle with several low-power 48 V loads whose combination exceeds the maximum operational current of a single 48 V battery. In such a case, it is worth connecting the required number of batteries in series to reduce the storage current and, thus, the cables' volume and weight.

The switching frequency value was chosen as a compromise between the dynamic performance and losses. Then, the reactive components of the Split-pi were sized by limiting the maximum ripple on the inductor current ($r_{i\%} = \pm 6.0\%$), the external capacitors' voltage ($r_{ve\%} = \pm 0.2\%$), and the bulk capacitor ($r_{v\%} = \pm 0.2\%$). Most of the rated parameters of the Split-pi chosen as a case study are the same as those reported in Table 3 of [23]. Nevertheless, some parameters were changed to allow the operation in Modes 3 and 4. In particular, the input and output currents/voltages are exchanged; the maximum ESS charge/discharge current is now 5 A; and the nominal duty cycle and load resistance are $\bar{d} = 0.277$ and $R_n = 3.333 \, \Omega$, respectively. Table 2 summarizes the main parameters of the Split-pi converter considered in the present study. Furthermore, it is worth highlighting that the duty cycles of the four switches in Modes 3 and 4 are {HBC1_top, HBC1_bottom, HBC2_top, HBC2_bottom} = {1, 0, d, 1 − d}.

Table 2. Main parameters of the Split-pi converter.

Parameter	Symbol	Value
Switching frequency	F_{sw}	20 kHz
Nominal input voltage	V_{1n}	180 V
Nominal output voltage	V_{2n}	50 V
Nominal power	P_n	750 W
Nominal load resistance	R_n	3.333 Ω
Nominal input current	I_{1n}	4.167 A
Max. charge/discharge current	I_{cx}, I_{dx}	5 A
Nominal output current	I_{2n}	15 A
Nominal duty-cycle	$\bar{d}$	0.277
Inductance value of L	L	1000 μH
Parasitic resistance of L	R_L	65 mΩ
Capacitance value of C_e	C_e	200 μF
Parasitic resistance of C_e	R_e	260 mΩ
Capacitance value of C	C	540 μF
Parasitic resistance of C	R_c	125 mΩ

As for the droop characteristics of the storage converter and the voltage generator of the microgrid, they were designed as follows. The droop parameters chosen for the ESS converter in Scenarios #2 and #3 were $E_{ds} = 50$ V and $R_{ds} = 0.2 \, \Omega$. They were chosen to impose a 6% voltage reduction at the nominal current. On the other hand, the droop parameters of the microgrid's voltage generator in Scenario #3 were $E_d = 55$ V and $R_d = 0.666 \, \Omega$. With such values, the ESS was supposed to be inactive for 50% of the microgrid's rated load power and charged below (or discharged above) such a threshold.

2.3. DC Microgrid Scenarios

Following the approach of [23], it is possible to consider five DC microgrid scenarios. They stem from the valid combinations of the three control modes that can be used for the power converters of the microgrid devices: non-stiff droop control, stiff droop control, and current control. Such scenarios are summarized in Table 3, which is a more compact version of the table reported in [23]. For improved clarity, each scenario is also referred to using an abbreviation like Sx–Gy, where x and y denote the control mode for the storage (S) and grid-side (G) converters. For example, D = non-stiff droop control; S = stiff droop control; C = current control; and N = no grid-side generator is present or operated in droop

mode. In the present work, only the first three scenarios are analyzed, i.e., those in which the controlled variable is the Split-pi's output voltage.

Table 3. Possible DC microgrid scenarios.

Microgrid Scenario	Storage Converter	Other Microgrid Generators
#1 (SS-GN)	Droop mode with droop resistance $R_d = 0$ (stiff)	No other generator present (passive load) or all current-controlled by the EMS
#2 (SD-GN)	Droop mode with droop resistance $R_d \neq 0$	No other generator present (passive load) or all current-controlled by the EMS
#3 (SD-GD)	Droop mode with droop resistance $R_d \neq 0$	At least one is droop-controlled, and none has $R_d = 0$
#4 (SC-GD)	Current mode	At least one is droop-controlled, and none has $R_d = 0$
#5 (SC-GS)	Current mode	One is droop-controlled and has $R_d = 0$ (stiff); the others, if present, are current-controlled by the EMS

In general, the load of the ESS converter is the combination of the voltage/current microgrid generators and passive loads. If droop-controlled voltage generators are present, they can be aggregated into a single equivalent generator with no-load voltage E_d and droop resistance R_d. Current generators can be aggregated into a single generator I. Ultimately, in the first three scenarios, the converter's load can be easily reduced to an equivalent load resistor R parallel connected to a current generator I_{eq}, as shown in [23].

2.4. Closed-Loop Control Scheme

The closed-loop control scheme for the ESS converter encompasses a current loop for I_{L1} and a voltage loop for V_2 to control the storage-side current and the output voltage, respectively. The voltage loop is complemented by a feed-forward (FF) action to reduce the voltage overshoot. In Modes 3 and 4, the FF term is the nominal duty cycle $\bar{d}$, whereas it is $(1 - \bar{d})^{-1}$ in Modes 1 and 2. Furthermore, in Scenarios #2 and #3, a third loop is required to implement the storage converter's droop characteristic. In order to prove the merit of the FF action, it is worth considering also a baseline scenario derived from Scenario #1 by deactivating the FF action.

The complete closed-loop control scheme is shown in Figure 3. In such a scheme, $G_{p1}(s)$ is the transfer function that expresses the relationship between d and I_{L1}; $G_{p2}(s)$ describes the dependence of the output current I_2 on I_{L1}; and $G_{p2}(s) \cdot R$ expresses the relationship between I_{L1} and V_2. The transfer functions of the current and voltage controllers are denoted by $G_{ci1}(s)$ and $G_{cv2}(s)$. The external current generator I_{eq} behaves as a disturbance that is suitably compensated for by the control system, regardless of its transfer function.
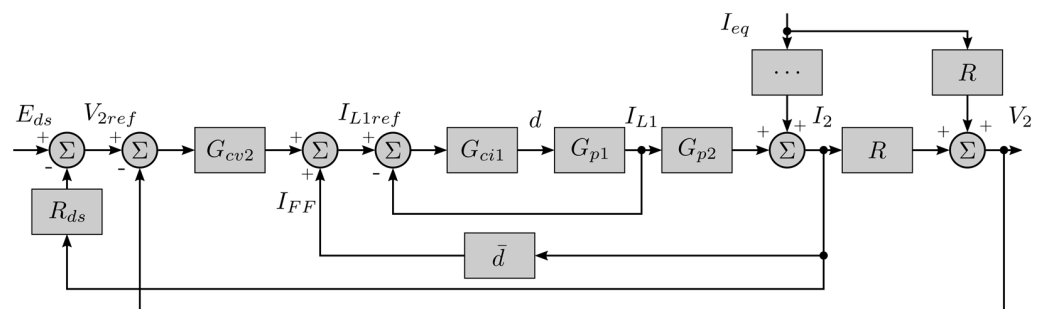

Figure 3. Control scheme used for voltage control of the Split-pi converter in Modes 3–4.

As in the usual practice, the duty cycle was limited between 0 and 0.95 to avoid prolonged transients with a unity duty cycle, which corresponds to a short circuit for the source of the HBC that works as a boost converter. This limitation did not affect the control

performance since the duty cycle had an average value $\overline{d} = 0.277$ and never reached 0.95, not even during transients, as will be shown in Sections 4 and 5. Furthermore, the reference for the inductor current I_{L1} was saturated to comply with the maximum charging/discharging current of the ESS and the allowed SOC limits. This limitation slightly reduced the dynamic performance of the system but was required to guarantee a safe operation of the ESS.

3. State-Space Model and Control System Design

In this section, the state-space model of the Split-pi converter operating in Modes 3–4 in Scenarios #1–#3 is given. Furthermore, based on such a model, the control system design procedure is described, and the parameters of the designed controllers are given for each scenario.

3.1. State-Space Model

The state-space model of the voltage-controlled Split-pi operating with an ESS voltage higher than the grid-side voltage was determined according to [25], considering the parasitic elements. It can be expressed in matrix form as follows:

$$\begin{cases} \dot{x} = Ax + Bu \\ y = Cx + Du \end{cases} \text{ with } \begin{cases} A = dA_{on} + (1-d)A_{off} \\ B = dB_{on} + (1-d)B_{off} \\ C = dA_{on} + (1-d)C_{off} \\ D = dD_{on} + (1-d)D_{off} \end{cases} \tag{1}$$

by considering $R_p = R//R_e$, $R_{sum} = R + R_e$, $R_{tot} = R_p + R_L + R_c$, and:

$$x = \begin{bmatrix} I_{L1}, & I_{L2}, & V_c, & V_e \end{bmatrix}' \tag{2}$$

$$u = \begin{bmatrix} V_1, I_{eq} \end{bmatrix}' \quad y = \begin{bmatrix} I_{L1}, V_2, I_2 \end{bmatrix}' \tag{3}$$

$$A_{on} = \begin{bmatrix} -\frac{R_L+R_c}{L} & \frac{R_c}{L} & -\frac{1}{L} & 0 \\ \frac{R_c}{L} & -\frac{R_{tot}}{L} & \frac{1}{L} & -\frac{R}{LR_{sum}} \\ \frac{1}{C} & -\frac{1}{C} & 0 & 0 \\ 0 & \frac{R}{R_{sum}C_e} & 0 & -\frac{1}{R_{sum}C_e} \end{bmatrix} \tag{4}$$

$$A_{off} = \begin{bmatrix} -\frac{R_L+R_c}{L} & 0 & -\frac{1}{L} & 0 \\ 0 & -\frac{R_p+R_L}{L} & 0 & -\frac{R}{LR_{sum}} \\ \frac{1}{C} & 0 & 0 & 0 \\ 0 & \frac{R}{R_{sum}C_e} & 0 & -\frac{1}{R_{sum}C_e} \end{bmatrix} \tag{5}$$

$$B_{on} = B_{off} = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{R_p}{L} \\ 0 & 0 \\ 0 & \frac{R}{R_{sum}C_e} \end{bmatrix} \tag{6}$$

$$C_{on} = C_{off} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & R_p & 0 & \frac{R}{R_{sum}} \\ 0 & \frac{R_e}{R_{sum}} & 0 & \frac{1}{R_{sum}} \end{bmatrix} \tag{7}$$

$$D_{on} = D_{off} = \begin{bmatrix} 0 & 0 \\ 0 & R_p \\ 0 & -\frac{R}{R_{sum}} \end{bmatrix} \tag{8}$$

It can be noticed that the matrices A_{on} and A_{off} of the model are different from those devised in [23] for a Split-pi operating in Modes 1–2. This results in different system dynamics.

3.2. Control System Design

By leveraging the devised model, it is possible to design a suitable control system for the Split-pi converter. In this work, classic PI or PID controllers were considered according to the approach shown in [26]. Thus, the general transfer function expressed by (9) was considered.

$$G_{PID}(s) = \left(K_p + \frac{K_i}{s} + sK_d \right) \frac{1}{1 + s\frac{K_d}{NK_p}} \tag{9}$$

where *N* is typically chosen greater than 10.

In order to design the PID controller, the state-space model was linearized around the rated operating point corresponding to $\bar{d}$ and $\bar{x} = [I_{L10}, I_{L20}, V_{c0}, V_{e0}]' = [4.167, 15, 180, 50]'$, thus obtaining the small-signal transfer functions $G_{p1}(s)$ and $G_{p2}(s)$. Then, the controllers $G_{ci1}(s)$ and $G_{cv2}(s)$ were designed based on the Bode diagrams of the two open-loop subsystems. More precisely, the controllers $G_{ci1}(s)$ and $G_{cv2}(s)$ were designed to impose suitable values of the crossover frequency ω_c and phase margin m_φ and to ensure a suitable gain margin m_g [23,27]. Such specifications (ω_c, m_φ, and m_g) were evaluated considering the open-loop function $G_{Fi}(s) = G_{ci1}(s)G_{p1}(s)$ for the inner loop and the function $G_{Fv}(s) = G_{cv2}(s)\frac{G_{ci1}(s)G_{p1}(s)}{1+G_{ci1}(s)G_{p1}(s)}$ for the outer loop. To impose suitable values of the crossover frequency ω_c and phase margin m_φ, the controller parameters K_p, K_i, and K_d of the PID were chosen such that the following equations were satisfied:

$$|G_c(j\omega_c)||G_p(j\omega_c)| = 1 \tag{10}$$

$$arg(G_c(j\omega_c)) + arg(G_p(j\omega_c)) + 180° = m_\varphi \tag{11}$$

In such equations, $G_c(\cdot)$ and $G_p(\cdot)$ are either $G_{ci1}(\cdot)$ and $G_{p1}(\cdot)$ if the inner loop is considered or $G_{cv2}(\cdot)$ and $\frac{G_{ci1}(\cdot)G_{p1}(\cdot)}{1+G_{ci1}(\cdot)G_{p1}(\cdot)}$ if the outer loop is considered. Equations (10) and (11) can be solved analytically. Subsequently, by means of the Bode diagrams of $G_{Fi}(s)$ and $G_{Fv}(s)$, it is verified that the gain margin is sufficiently high, typically higher than 12 dB.

Note that the crossover frequency influences the dynamic performance of the closed-loop system. In general, it must be as high as possible but at least 10 times lower than the switching frequency so that the controller does not process the switching ripple. Furthermore, for proper decoupling between the voltage and current loops, the crossover frequency of the external loop must be suitably lower than that of the internal loop. The phase and gain margins characterize the stability of the closed-loop system and affect the damping of the system response. A phase margin of 50°–60° is usually enough in the case of passive loads. Instead, active loads require a higher phase margin than 85° to ensure stability under every possible operating condition. Finally, to guarantee stability despite parameter variations, a gain margin higher than 12 dB is required for both passive and active loads.

Although the state-space model was linearized around the rated operating point, i.e., considering the rated load resistance *R*, the designed controllers are supposed to also perform well with lower loads thanks to their wide stability margins. It is also worth noting that it was $R = R_n$ in Scenarios baseline, #1 and #2. On the other hand, in Scenario #3, *R* was very low because it resulted from the parallel connection of R_n and the droop resistance R_d of the voltage generator.

The parameters of the designed controllers are summarized in Table 4. Some noteworthy remarks can be made about the controller design for Modes 3–4. The LC filter before HBC1 determined a resonance at $\omega = 1330$ rad/s with very low damping ($\zeta = 0.1$). If the related complex conjugate poles were not canceled, the achievable bandwidth was quite limited. Therefore, a PI regulator was unsuitable and, thus, a PID regulator was needed. The phase margin that resulted after satisfying all the design constraints was slightly higher than 85°, and the achievable crossover frequency could not exceed 1200 rad/s. In addition, a far pole at 10^5 rad/s should have been introduced in the current controller to decrease

the gain at the switching frequency (F_{sw} = 20 kHz). However, the controller was to be implemented in discrete form with a sampling frequency equal to F_{sw}. Thus, the previously mentioned far pole could not be implemented and had to be moved down to $4 \cdot 10^4$ rad/s.

Table 4. Parameters of the designed controllers in each scenario.

Loop Controller and Scenario	Values of ω_c, m_φ, and m_g	PI and PID Coefficients
G_{ci1} for current I_{L1} baseline, #1 (SS-GN), and #2 (SD-GN)	ω_c = 1200 rad/s m_φ = 94° m_g = ∞	K_{pi} = 4.507·10^{-3} K_{ii} = 31.2608 K_{di} = 1.711·10^{-5} N = 37.9651 + pole @ 4.0·10^4 rad/s
G_{ci1} for current I_{L1} #3 (SD-GD)	ω_c = 1200 rad/s m_φ = 89.8° m_g = ∞	K_{pi} = 3.207·10^{-3} K_{ii} = 26.6073 K_{di} = 1.343·10^{-5} N = 41.876 + pole @ 4.0·10^4 rad/s
G_{cv2} for voltage V_2 w/o FF baseline	ω_c = 100 rad/s m_φ = 120° m_g = 31 dB	K_{pv} = 0.1275 K_{iv} = 11.885 + pole @ 666 rad/s
G_{cv2} for voltage V_2 w/FF #1 (SS-GN) and #2 (SD-GN)	ω_c = 100 rad/s m_φ = 120° m_g = 29.4 dB	K_{pv} = 0.076 K_{iv} = 5.1286 + pole @ 666 rad/s
G_{cv2} for voltage V_2 w/FF #3 (SD-GD)	ω_c = 100 rad/s m_φ = 120° m_g = 43.9 dB	K_{pv} = 0.097 K_{iv} = 4.7315 + pole @ 666 rad/s

The current controller was in charge of compensating for the resonance only in the case of variations of current reference. Thus, load resistance variations had to be managed by the voltage controller alone. Such a controller was implemented as a PI regulator plus a pole at half the resonance frequency. Furthermore, the phase margin that resulted after satisfying all the design constraints was considerably higher than 85° to properly compensate for the resonance.

Referring to Table 4, all the scenarios exhibited nearly the same dynamics for I_{L1}, so the related controllers had similar coefficients. As for the voltage controller, the sensitivity of the output voltage dynamics to R was high without the FF action. On the other hand, the FF action mitigated this sensitivity. Thus, similar voltage controllers were obtained in Scenarios #1, #2, and #3 despite the different values of R.

4. Simulation Results

Several simulations were performed to test the controlled system in the considered scenarios. The circuit model of the Split-pi was realized with PLECS (blockset version) based on Figure 1 and Table 1. The default parameters were confirmed for PLECS. On the other hand, the control system was implemented in Simulink according to Figure 3 and Table 4. All the default parameters were confirmed in the Simulink environment, except for the following:

- Solver type: variable-step
- Solver: ode23tb (stiff/TR-BDF2)
- Max step size: $1/(10 \cdot F_{sw})$
- Solver reset method: robust.

The obtained simulation results are presented and commented on in the following.

4.1. Baseline Scenario and Scenario #1 (SS-GN)

In the baseline scenario, the storage converter was used to regulate the microgrid voltage at 50 V and supply a passive load alone or with the help of an external cur-

rent generator I. Furthermore, the FF action was deactivated. Before t = 0.2 s, the converter exhibited a steady-state output with $R = R_n$ and $I = 0$. Then, the values of R and I were changed every 200 ms in a stepwise fashion according to the following sequences: $R = \{2, 100, 2, 1, 2, 100, 2\} \cdot R_n$ and $I = \{0, 0, 1, 1, 1, 0, 0\} \cdot I_n$. This way, the storage system was discharged, charged, and discharged again. The waveforms of the main electrical and control variables are shown in Figures 4 and 5. At each load resistance variation, the control system recomputed the duty cycle so the inductor current quickly tracked its reference value, although with some ringing due to the resonance. The output current followed the load resistance variations and became negative when the external generator supplied excess current. The percent variation of grid voltage with respect to the nominal output voltage V_{2n} is shown in blue in Figure 5 and shows null error at a steady state. However, during transients, the undershoots and overshoots exceeded the allowed transient tolerance of $\pm 20\%$ by a large margin. Thus, the microgrid would have been automatically de-energized by the protection devices.
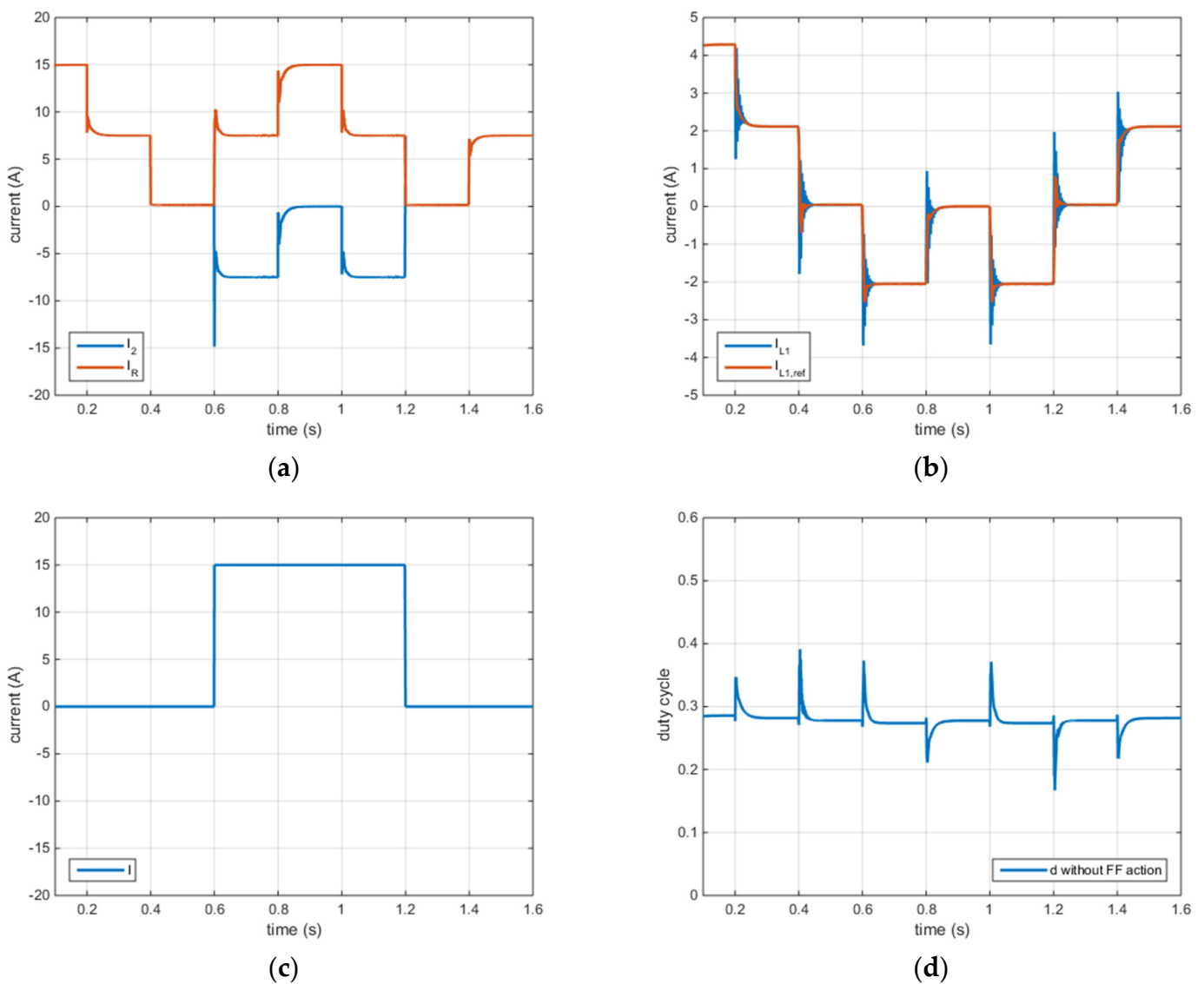

Figure 4. Simulation results in the baseline scenario without FF action: (**a**) output and load currents; (**b**) input inductor current and its reference; (**c**) external generator's current; (**d**) duty cycle.
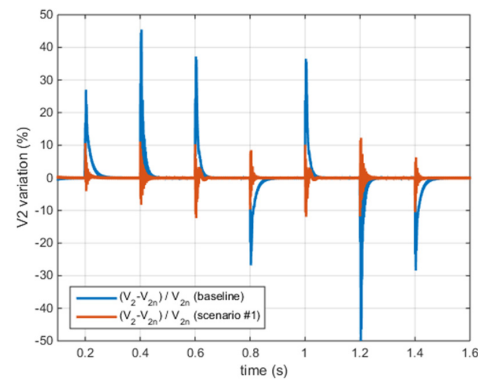
Figure 5. Grid voltage variation in the baseline scenario and Scenario #1 (SS−GN).

The FF action significantly improved the system response in Scenario #1, for which the simulation results are shown in Figures 5 and 6. The duty cycle was varied instantaneously by the FF action at each load variation. Consequently, the waveforms of I_2 and I_R were almost square waves, and the maximum percent grid voltage variation was reduced to 12.3%, as shown in orange in Figure 5.
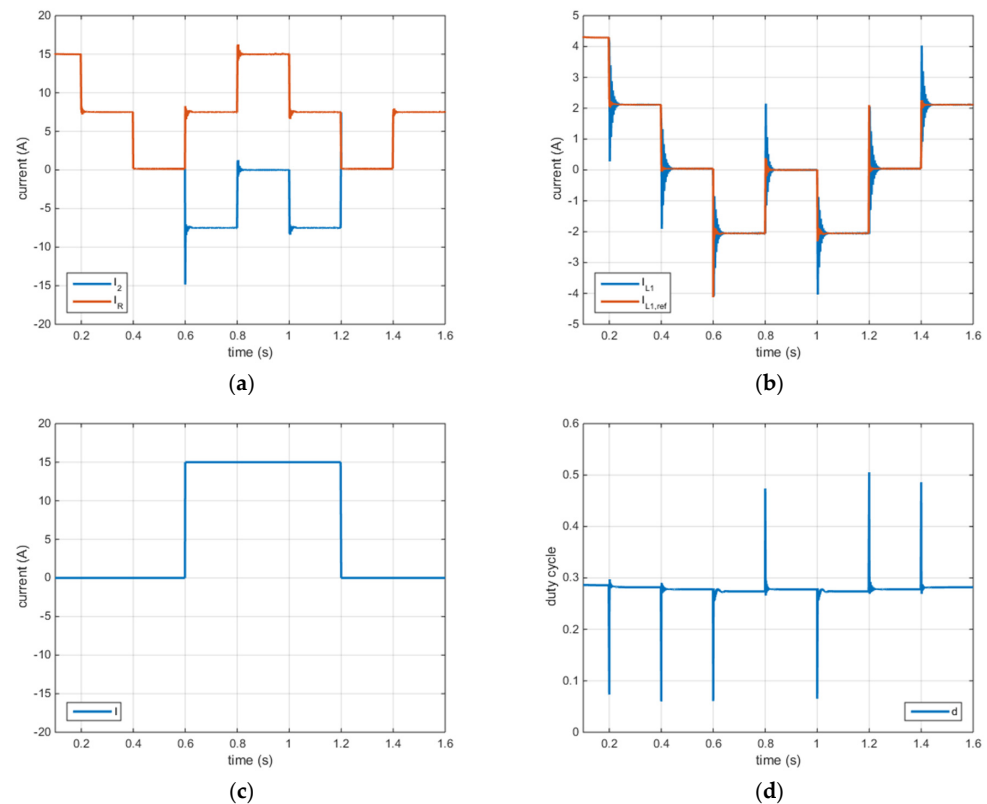

Figure 6. Simulation results in scenario #1 (SS−GN): (**a**) output and load currents; (**b**) input inductor current and its reference; (**c**) external generator's current; (**d**) duty cycle.

However, in general, the very large stepwise load variations considered in [23,24], i.e., $R_n \leftrightarrow 100 \cdot R_n$, cannot be tolerated in Modes 3 and 4. For such variations, even without the external current generator, the maximum overshoot with the FF action would be +27.3%. The only way to tolerate such perturbations would be to increase the resonance frequency and the damping factor of the LC filter by changing the values of L and C. However, the current and voltage ripple would increase as well. In any case, it is worth highlighting that stepwise variations are ideal perturbations useful for theoretical studies and are never to be

encountered in real-world applications. In fact, using the FF action, the microgrid voltage variation never exceeded ±20% in the experimental tests described in Section 5.

4.2. Scenario #2 (SD-GN)

The control scheme of Scenario #2 encompassed the FF action and a third outer loop to implement the droop characteristic besides the internal loops for I_{L1} and V_2. The same initial conditions and load sequence as in Scenario #1 were considered. The obtained results are shown in Figure 7 in terms of output voltage and output and load currents, as well as control variables (i.e., input inductor current and duty cycle). As expected, in steady-state conditions, the converter's output voltage V_2 tracked the reference voltage $V_{2,ref}$ computed according to the droop characteristic. For example, the steady-state voltage variation was −6% when the storage system was discharged at the rated power and +3% when it was recharged at half power. Even considering the overshoots, the maximum absolute grid voltage variation was 12.7% at t = 1.2 s. This result implied that the microgrid voltage stayed within +9.7% of its rated value (+3%) and was obtained despite the ideal stepwise variations of load resistance.
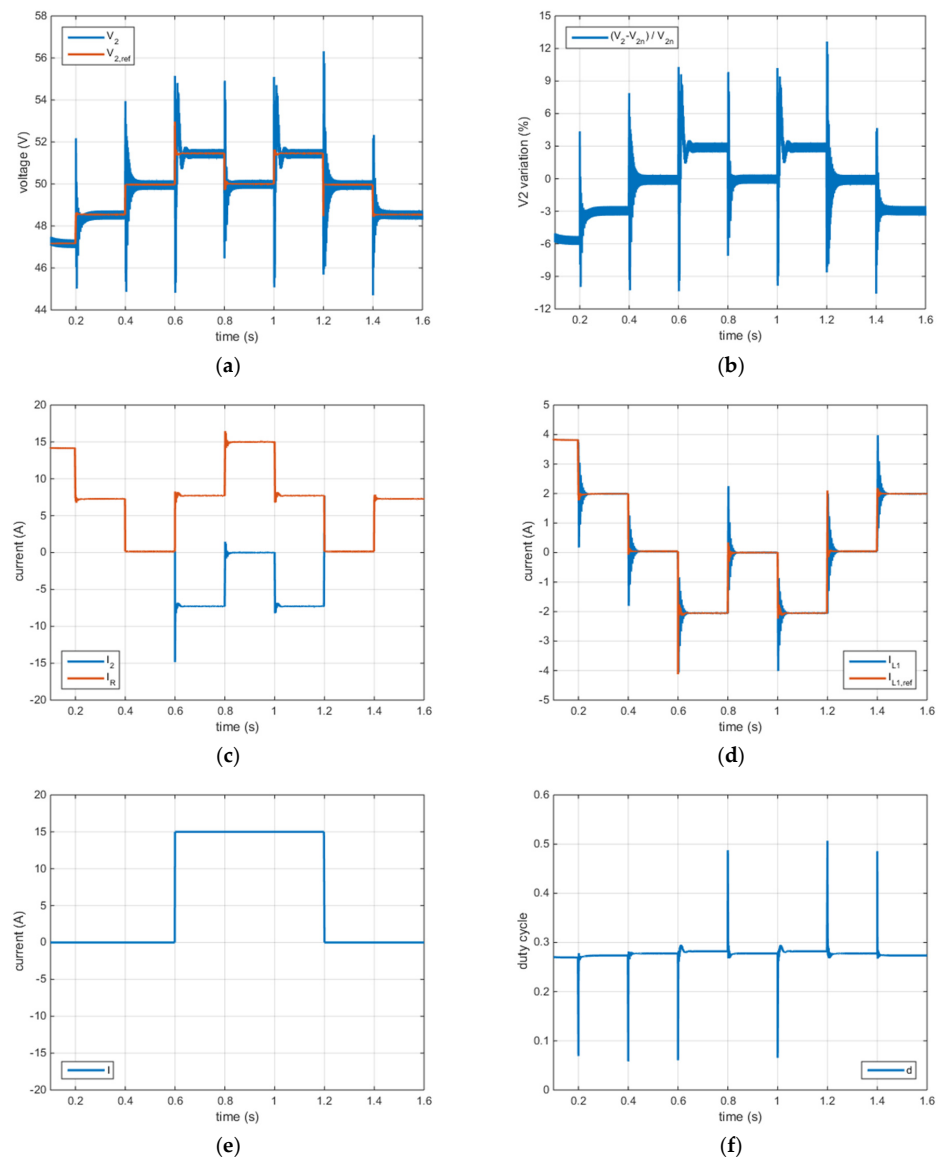

Figure 7. Simulation results in Scenario #2 (SD−GN): (**a**) actual and reference grid voltage; (**b**) grid voltage variation; (**c**) output and load currents; (**d**) input inductor current and its reference; (**e**) external generator's current; (**f**) duty cycle.

Finally, the waveforms of the output currents and the control variables were similar to those obtained in Scenario #1 (SS-GN).

4.3. Scenario #3 (SD-GD)

The ESS converter and the voltage generator of the microgrid were both controlled in droop mode in Scenario #3. The two droop resistances were chosen so that the storage converter supplied no power for 50% of the microgrid's rated load. Furthermore, a current generator I was also present in the microgrid. The waveforms of the most meaningful electrical and control quantities are shown in Figure 8. Before t = 0.8 s, the converter was in steady-state conditions with $R = 100 \cdot R_n$ (low load) and $I = 0$. The ESS was recharged at $I_d = -5.65$ A by the voltage generator, and the voltage variation was about +2%. Then, R and I were changed every 200 ms in a stepwise fashion according to the following sequences: $R = \{2, 1, 1, 2, 100\} \cdot R_n$, $I = \{0, 0, 0.457, 0.457, 0.457\} \cdot I_n$. Thus, the current of the ESS converter exhibited the following values: 0 A, 5.5 A, 0 A, −5.15 A, and −10.8 A.
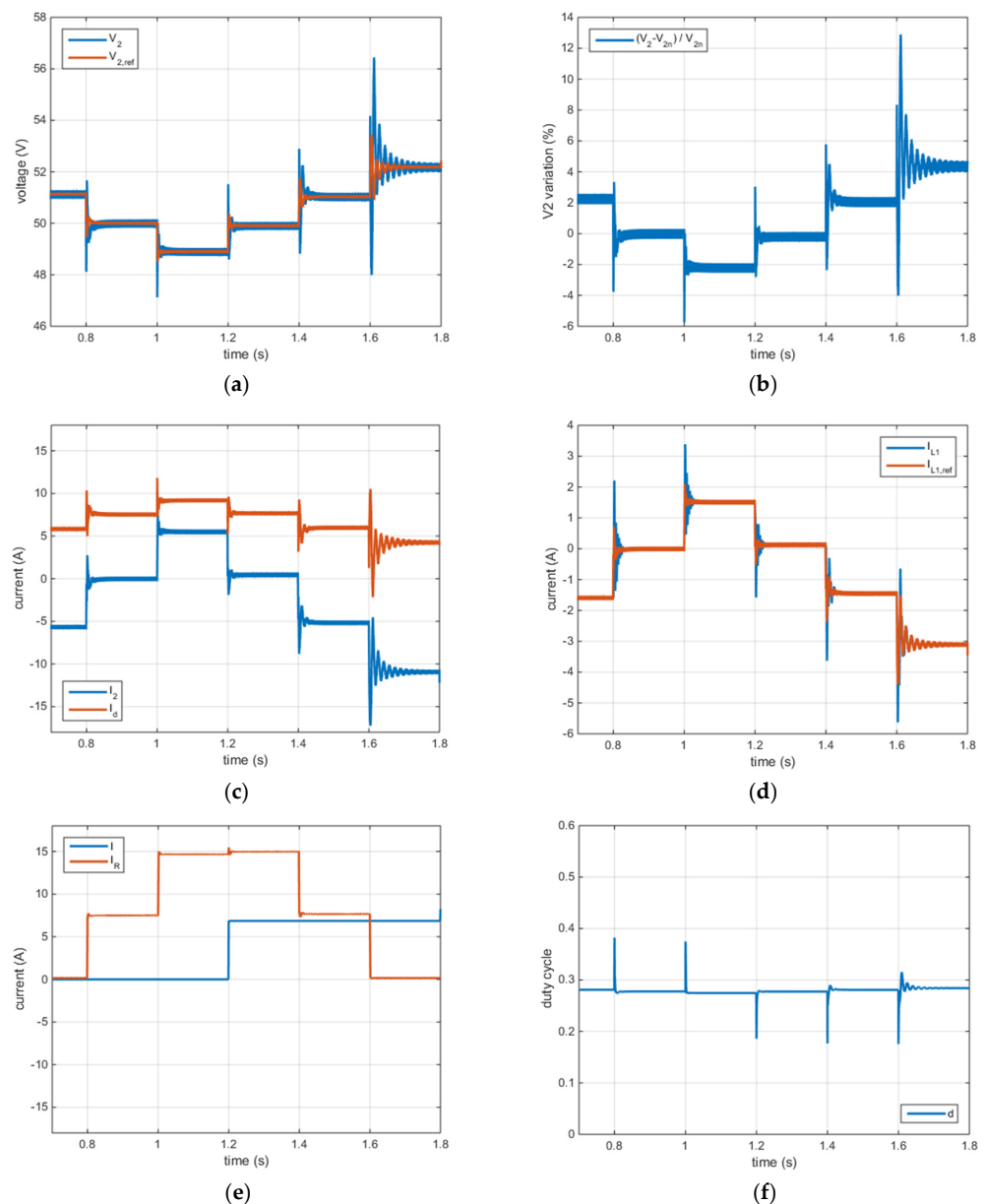

Figure 8. Simulation results in scenario #3 (SD−GD): (**a**) grid voltage and its reference; (**b**) grid voltage variation; (**c**) output current and voltage generator's current; (**d**) input inductor current and its reference; (**e**) external generator's current and load current; (**f**) duty cycle.

From Figure 8e, it is possible to evaluate the net current demand that had to be satisfied by the storage converter and the voltage generator of the microgrid. In particular, the net current was 50% of the rated value during the time intervals from t = 0.8 s to t = 1.0 s and from t = 1.2 s to t = 1.4 s. Thus, in such intervals, the current delivered by the storage converter was zero, as shown in Figure 8c, and the load was supplied only by the voltage generator. On the other hand, the battery was recharged/discharged when the net current demand was lower or higher than 50%, respectively.

The maximum absolute grid voltage variation exhibited during the test was 12.9%. Thus, it stayed well under 20%. The waveforms of the duty cycle and the input inductor current were close to those obtained in the former scenarios.

5. Experimental Validation

The details of the prototypal Split-pi converter and the related testbench were the same as in [24], but the input and output ports were exchanged. The converter prototype was based on an integrated power module STGIPS10K60A featuring a three-phase, IGBT-based H-bridge. The two inductors and the grid-side external capacitors were connected to the main board as external components. The storage system connected to the converter's input was emulated using a TDK-Lambda GEN600-5.5 power supply set to 180 V. The active load connected to the converter's output was composed of a Sorensen SLH-500-6-1800 programmable electronic load and a TDK-Lambda GEN60-40 power supply; the latter was used as a voltage generator or a current generator, depending on the scenario under test. In Scenario #3, a 1.2 Ω, 200 W power resistor was also used as the grid-side droop resistor. Figure 9 shows a photo of the whole experimental setup.
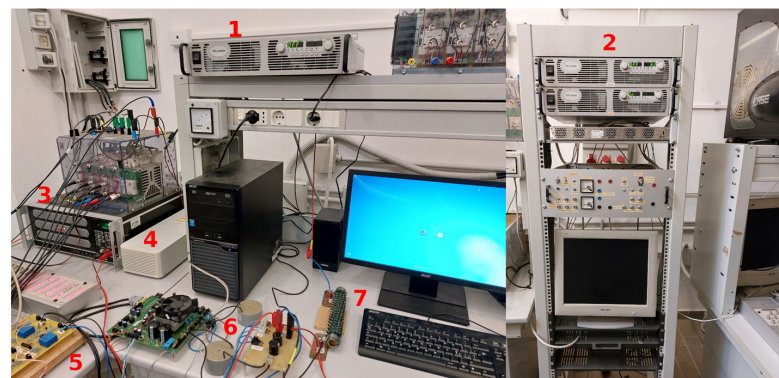

Figure 9. Photo of the experimental setup: (**1**) TDK-Lambda GEN60-40 grid-side power supply; (**2**) TDK-Lambda GEN600-5.5 storage-side power supply; (**3**) Sorensen SLH-500-6-1800 electronic load; (**4**) dSPACE DS1103 board; (**5**) LEM-based measuring circuits; (**6**) Split-pi prototype (including the inductors and the grid-side external capacitor); (**7**) droop resistor of the grid-side power supply (only used in Scenario #3).

The electrical quantities of interest were measured using LEM-based voltage and current measurement circuits. They were acquired and saved by the dSPACE DS1103 board used to control the converter implementing the designed controllers and the PWM modulator. Later, they were imported into MATLAB and plotted. The obtained results are coherent with the simulation results and are discussed in the following subsections.

5.1. Baseline Scenario and Scenario #1 (SS-GN)

In these two tests, the Split-pi was used to form a stiff microgrid encompassing an aggregated passive load. The only difference between the two scenarios was the absence or presence of the FF action. The electronic load allowed applying a stepwise load variation from 10 Ω to 20 Ω at t = 0 s. As a result, the load power instantly decreased from 250 W to 125 W, causing a voltage overshoot on V_2. The experimental results are presented in Figure 10 together with the simulation results. Each plot in Figure 10 shows that the

simulation and experimental results were in good agreement. The vertical offset that is present in Figure 10a–d is due to the higher losses of the converter prototype compared to the simulation. Thus, the input current and the duty cycle had to be increased to obtain the desired output voltage. This behavior was expected because ideal semiconductor switches and diodes were considered in the simulations.
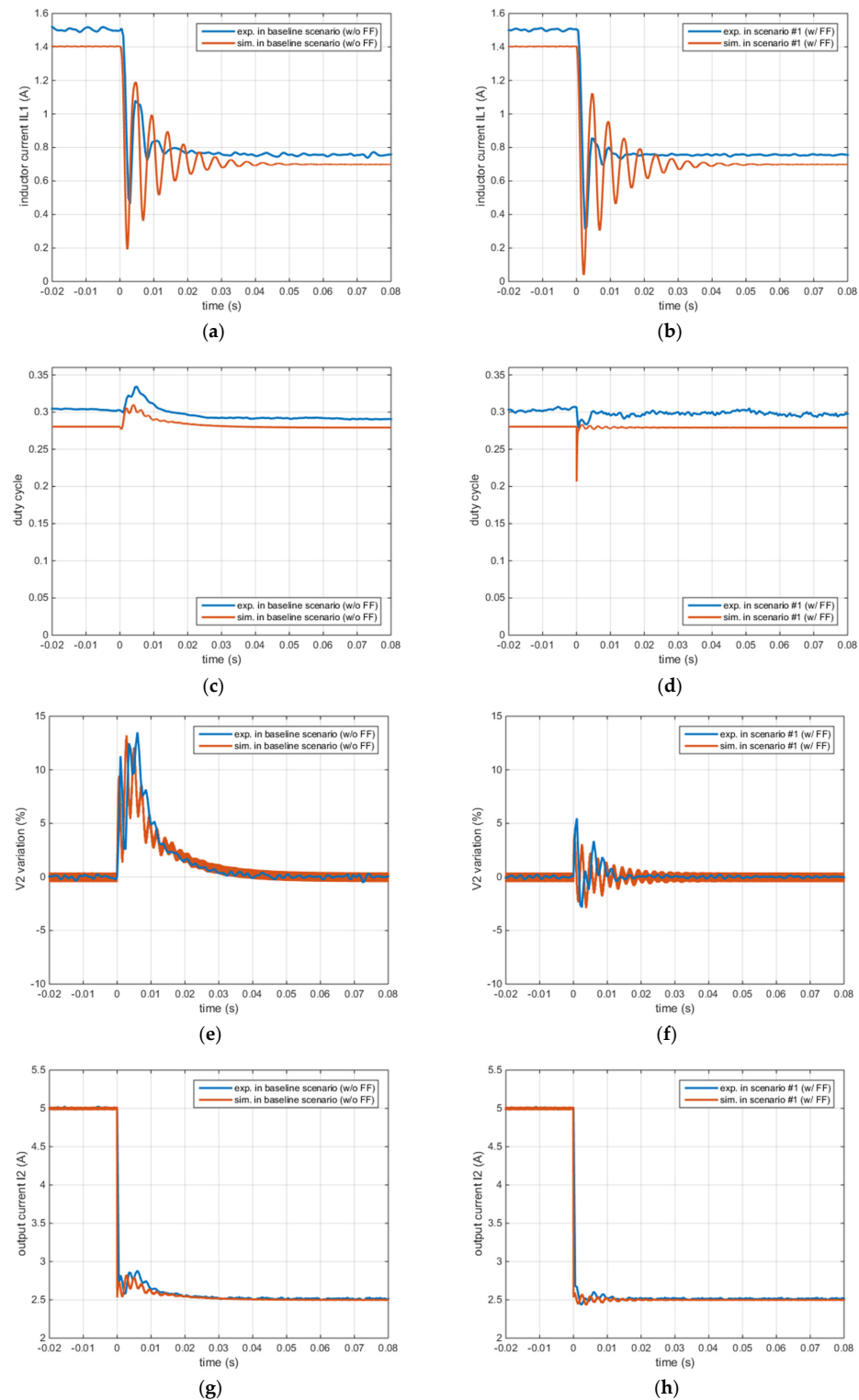

Figure 10. Comparison between simulation and experimental results in the baseline scenario (left) and Scenario #1 (SS−GN) (right): (**a**,**b**) input inductor current; (**c**,**d**) duty cycle; (**e**,**f**) grid voltage variation; (**g**,**h**) output current.

Furthermore, the comparison between the results obtained in the baseline scenario and in Scenario #1 confirmed that the FF action allowed for an instantaneous reduction of the duty cycle, which determined faster dynamics and reduced the voltage overshoot from 13.5% to 5.5%. Likewise, the undershoot on V_2 was reduced from -11.2% to -5.6% for the opposite stepwise load variation. Even higher reductions are expected for larger variations of output power which, unfortunately, cannot be tested due to the limited power of the prototype.

Using the FF action, the output current waveform was pretty squared. Furthermore, the input inductor current showed faster dynamics and more limited ringing.

5.2. Scenario #2 (SD-GN)

In this test, the Split-pi converter formed a non-stiff microgrid characterized by a no-load voltage of 50 V and a droop resistance of 1.2 Ω. The active load was composed of a 20 Ω resistance and an external current generator I_d set to 1.25 A. The latter was switched off at t = 0 s. The experimental results are shown in Figure 11 together with the simulation results. As the figure shows, before switching off the current generator, the storage converter delivered the remaining current quota needed to supply the load. Instead, when the current generator was switched off, the converter promptly supplied the entire load, as expected. According to the droop resistance value, the voltage variations with the current generator switched on and off were -3% and -5.66%, respectively. It is worth noting that the power supply was not able to impose an ideal current step. Thus, the experimental waveforms did not perfectly match the simulation results. Nonetheless, the control system instantly compensated for the actual current waveform produced by the external generator and succeeded in regulating the output voltage at the desired value.
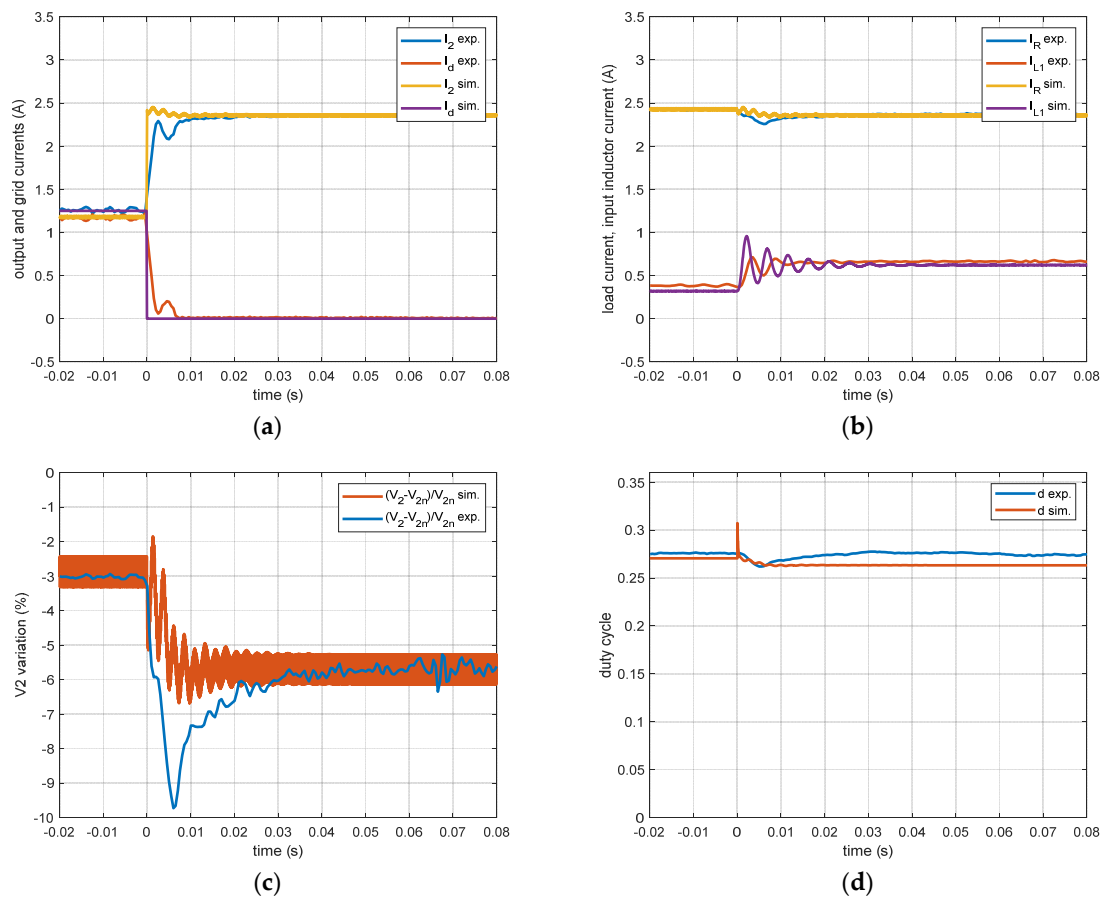

Figure 11. Simulation and experimental results in Scenario #2 (SD−GN): (**a**) output and grid currents; (**b**) load current and input inductor current; (**c**) grid voltage variation; (**d**) duty cycle.

Finally, the vertical offset in the waveforms of the input inductor current and the duty cycle was again due to the higher losses of the converter prototype compared to the simulations.

5.3. Scenario #3 (SD-GD)

During this test, the Split-pi converter and the microgrid voltage generator were controlled in droop mode with the same droop parameters (i.e., a droop resistance of 1.2 Ω and a no-load voltage of 50 V). Thus, the two devices were required to equally share the load for each value of the load resistance. The resulting microgrid was non-stiff. A stepwise variation of load resistance from 20 Ω to 10 Ω was applied at t = 0 s. The obtained waveforms are shown in Figure 12. As expected, the current sharing ratio was respected under steady-state conditions before and after the stepwise load-resistance variation.
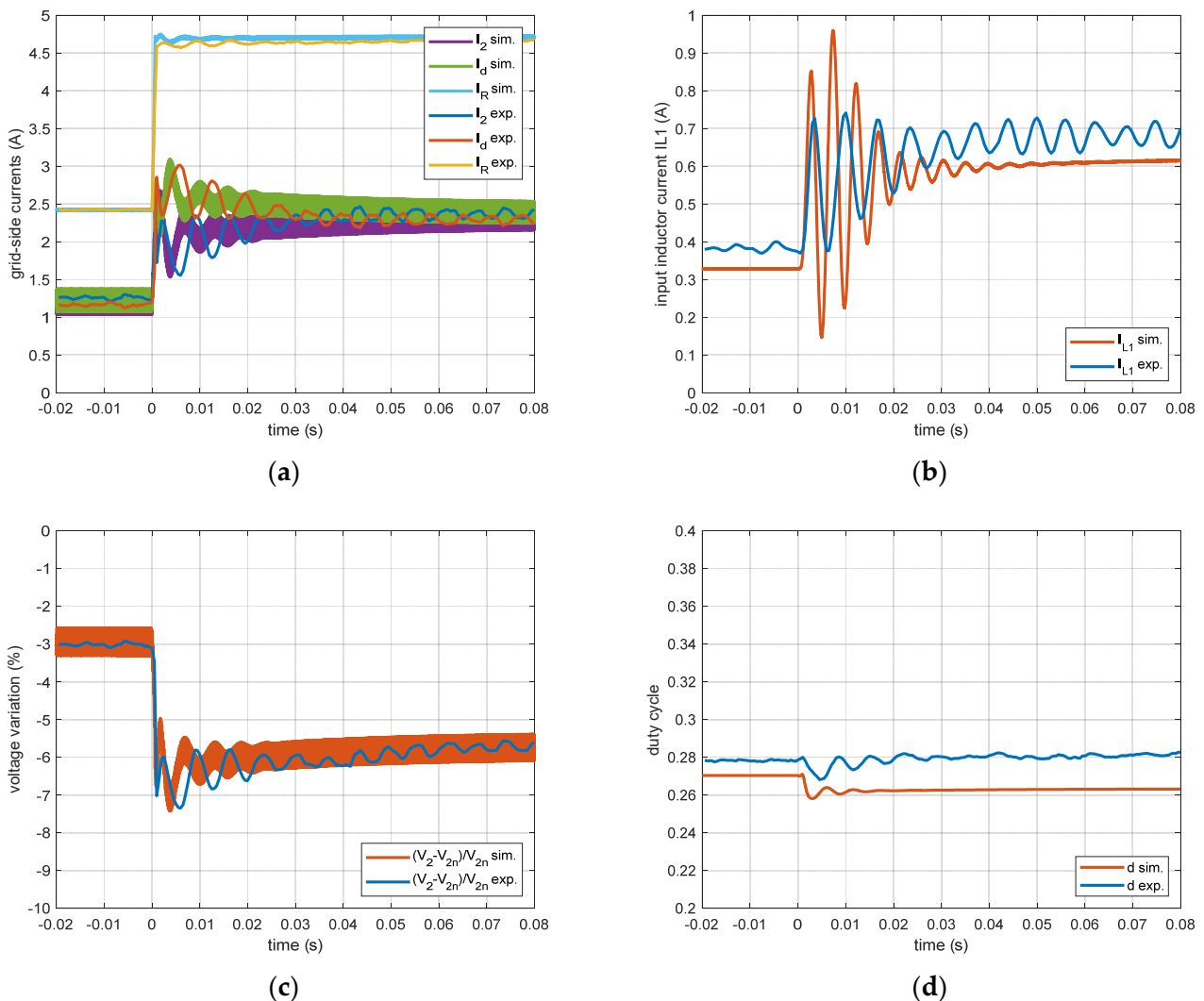

Figure 12. Simulation and experimental results in Scenario #3 (SD−GD): (**a**) grid−side currents; (**b**) input inductor current; (**c**) grid voltage variation; (**d**) duty cycle.

Furthermore, the expected voltage variation was exhibited at each power level, i.e., −3% and −5.66%. Such values did not differ between Scenarios #2 and #3 because the two steady-state values of the converter's output current in such scenarios were the same.

Finally, it is worth observing that the duty cycle variation was quite limited because the load was shared between the converter and the voltage generator of the microgrid.

By comparing the simulation and the experimental waveforms in Figure 12a,c, a good agreement can be noticed. The steady-state values and the slower time constant match. On

the other hand, the ringing frequency of the experimental waveform was slower due to the unmodeled parasitic inductance of the cables connecting the converter's output to the rest of the microgrid. Finally, Figure 12b,d again show the vertical offset in the waveforms of the input inductor current and the duty cycle, which was due to the different power losses.

6. Robustness Analysis and Limitations of the Split-Pi Converter

In order to complete the study, this section presents the results of a robustness analysis and comments on the limitations of the Split-pi converter.

6.1. Robustness Analysis

As shown by the simulation tests performed in Section 4 and confirmed by the experimental tests described in Section 5, the ESS converter under study and its control system ensured stable microgrid operation and kept the maximum absolute grid voltage variation under 20%. In particular, considering the load sequences applied in Section 4, the maximum absolute grid voltage variation was 12.3%, 12.7%, and 12.9% in Scenarios #1, #2, and #3, respectively. Since the main circuit parameters (i.e., the reactive components) can be affected by uncertainties, it is worth performing a robustness analysis of the controlled converter operating in Scenarios #1–#3. The usual tolerances on commercial inductors and capacitors are $\pm15\%$ and $\pm20\%$, respectively. The variations of the parasitic resistances are often smaller.

Based on such considerations, the robustness analysis was performed as follows. Overall, 10 significant combinations of parameter variations were considered based on the following parameters: the bulk capacitance C and the related parasitic resistance R_c; the storage-side (left) and grid-side (right) inductance L and the related parasitic resistance R_L; and the left and right capacitance C_e and the related parasitic resistance R_e. For each scenario and each parameter combination, the converter was simulated considering the controller parameters from Table 4 and the same load sequences as in Sections 4.1–4.3. Then, the stability of the response was evaluated, and the maximum absolute grid voltage variation was chosen as a metric. In particular, such a metric was computed on the whole response to the applied load sequence.

The results obtained in Scenario #1 for each combination of parameter variations are summarized in Tables 5–7. The operation was stable for all the considered parameter variations. The bulk capacitance reduction determined the worst effect: the maximum absolute grid voltage variation increased from the base value of 12.3% to 17.8%. The increase of the bulk capacitance, as well as all the considered inductance variations, produced a maximum absolute grid voltage variation of around 15%. A smaller increase of the metric was obtained for the variations of the external capacitance.

Table 5. Results of robustness analysis against variations of C and R_c in Scenario #1.

ΔC	ΔR_c	Max. $|\Delta V_2|$	Stable Operation
+20%	+10%	14.3%	yes
−20%	−10%	17.8%	yes

Table 6. Results of robustness analysis against variations of L and R_L in Scenario #1.

ΔL Left	ΔR_L Left	ΔL Right	ΔR_L Right	Max. $|\Delta V_2|$	Stable Operation
+15%	+7.5%	+10%	+5%	15.0%	yes
−15%	−7.5%	−10%	−5%	15.3%	yes
+10%	+5%	+15%	+7.5%	14.8%	yes
−10%	−5%	−15%	−7.5%	14.4%	yes

Table 7. Results of robustness analysis against variations of C_e and R_e in Scenario #1.

ΔC_e Left	ΔR_e Left	ΔC_e Right	ΔR_e Right	Max. $\mid\Delta V_2\mid$	Stable Operation
+20%	+10%	+10%	+5%	11.7%	yes
−20%	−10%	−10%	−5%	13.6%	yes
+10%	+5%	+20%	+10%	11.0%	yes
−10%	−5%	−20%	−10%	15.1%	yes

The results obtained in Scenario #2 for each combination of parameter variations are summarized in Tables 8–10. The operation was stable for all the considered parameter variations, and the droop control of the converter implied lower output voltage variations compared to Scenario #1. Again, the worst effect was caused by the bulk capacitance reduction, which produced a 16.0% maximum absolute grid voltage variation compared to the base value of 12.7%. Furthermore, the external capacitance variations produced nearly the same effect as in Scenario #1.

Table 8. Results of robustness analysis against variations of C and R_c in Scenario #2.

ΔC	ΔR_c	Max. $\mid\Delta V_2\mid$	Stable Operation
+20%	+10%	15.4%	yes
−20%	−10%	16.0%	yes

Table 9. Results of robustness analysis against variations of L and R_L in Scenario #2.

ΔL Left	ΔR_L Left	ΔL Right	ΔR_L Right	Max. $\mid\Delta V_2\mid$	Stable Operation
+15%	+7.5%	+10%	+5%	15.9%	yes
−15%	−7.5%	−10%	−5%	13.2%	yes
+10%	+5%	+15%	+7.5%	15.7%	yes
−10%	−5%	−15%	−7.5%	12.2%	yes

Table 10. Results of robustness analysis against variations of C_e and R_e in Scenario #2.

ΔC_e Left	ΔR_e Left	ΔC_e Right	ΔR_e Right	Max. $\mid\Delta V_2\mid$	Stable Operation
+20%	+10%	+10%	+5%	11.7%	yes
−20%	−10%	−10%	−5%	13.9%	yes
+10%	+5%	+20%	+10%	10.8%	yes
−10%	−5%	−20%	−10%	15.4%	yes

Tables 11–13 summarize the results obtained in Scenario #3 for each combination of parameter variations. As the tables show, the system exhibited a stable operation in most cases, but there were some exceptions. An increase of the bulk capacitance always implied unstable operation regardless of the applied load. On the other hand, the reduction of this capacitance and the inductance increase determined unstable operation only for two load conditions out of five in the load sequence: for the transition $2 \cdot R_n \rightarrow 100 \cdot R_n$ with $I = 0.457 \cdot I_n$ (i.e., between 1.6 s and 1.8 s), and for the sequence $2 \cdot R_n \rightarrow R_n$ with $I = 0$ (i.e., between 1.0 s and 1.2 s). As expected, the instability occurred for variations in the parameters of the input filter formed by the storage-side inductor and the bulk capacitor, which caused the problematic resonance discussed in Section 3.

Table 11. Results of robustness analysis against variations of C and R_c in Scenario #3.

ΔC	ΔR_c	Max. $|\Delta V_2|$	Stable Operation
+20%	+10%	not defined	never
−20%	−10%	12.8%	yes, except between 1.6 s and 1.8 s

Table 12. Results of robustness analysis against variations of L and R_L in Scenario #3.

ΔL Left	ΔR_L Left	ΔL Right	ΔR_L Right	Max. $|\Delta V_2|$	Stable Operation
+15%	+7.5%	+10%	+5%	19.2%	yes, except between 1.0 s and 1.2 s
−15%	−7.5%	−10%	−5%	12.2%	yes
+10%	+5%	+15%	+7.5%	19.3%	yes, except between 1.6 s and 1.8 s
−10%	−5%	−15%	−7.5%	11.7%	yes

Table 13. Results of robustness analysis against variations of C_e and R_e in Scenario #3.

ΔC_e Left	ΔR_e Left	ΔC_e Right	ΔR_e Right	Max. $|\Delta V_2|$	Stable Operation
+20%	+10%	+10%	+5%	12.6%	yes
−20%	−10%	−10%	−5%	13.3%	yes
+10%	+5%	+20%	+10%	12.2%	yes
−10%	−5%	−20%	−10%	13.7%	yes

Furthermore, the system was always stable for variations of the external capacitance. In the worst case, the maximum absolute grid voltage variation increased from the base value of 12.9% to 19.3%.

Overall, good results were obtained by designing classical PID controllers with suitably high phase and gain margins. Better results can be obtained only by resorting to robust control techniques.

6.2. Limitations of the Split-Pi Converter

To summarize the outcomes of the present study, it is worth highlighting the limitations of the proposed converter and the related control system. As pointed out in the introduction, the Split-pi is a non-isolated bidirectional DC/DC converter. Thus, it is not suitable for applications where galvanic isolation is required by specific technical standards. Furthermore, according to Figure 2, some switches and diodes of the Split-pi could be unused and determine unwanted losses if the input and output voltages always keep the same relationship, i.e., if the converter always operates in Modes 1–2 or 3–4. In such circumstances, the topology can be simplified by removing the unused semiconductor devices though retaining bidirectional operation.

Regarding the control performance, as discussed in Sections 3.2 and 4.1, the Split-pi exhibits an asymmetrical behavior with worse dynamic performance in Modes 3–4 compared to Modes 1–2. This result is due to the two-stage topology of the Split-pi, where the storage-side stage is affected by a poorly damped LC resonance. Single-stage topologies do not exhibit such a problem, although they have other drawbacks like a discontinuous storage current, high switch count, weak regulation capability, and, possibly, a negative output voltage compared to the input. Finally, although the present work shows that the Split-pi converter can be controlled with classic PID regulators, better performance in terms of dynamic performance and robustness to parameter variations can be obtained using more sophisticated control techniques.

7. Conclusions and Future Work

This paper presented the state-space model of the Split-pi converter operating with an ESS voltage higher than the grid-side voltage in three typical microgrid scenarios where the controlled variable was the converter's output voltage. The model considered the parasitic elements of the converter and the correct equivalent load for each scenario. Based on such a model, PI/PID controllers were designed for the current and voltage loops. It was shown that the input LC filter caused a poorly damped resonance, limiting the achievable bandwidth and making the design of the controllers more complicated than for a Split-pi operating with an ESS voltage lower than the grid-side voltage.

The study was validated through simulations and experimental tests on a lab prototype of a Split-pi that interfaced a 180 V storage system with a 48 V DC microgrid. Such a setup can represent a reduced-power prototype of terrestrial and maritime microgrids. Furthermore, the converter's robustness was assessed against variations of the main circuit parameters, and the limitations of the proposed converter were discussed.

The proposed modeling approach can also be used for other bidirectional DC/DC converters. Future work will be devoted to completing the study by modeling the Split-pi converter operating in Modes 3–4 in Scenarios #4 and #5 and designing suitable PI/PID controllers. Furthermore, it could be worth investigating whether a single unconventional control system is suitable to control the Split-pi in more than one microgrid scenario.

Nomenclature

d	Duty cycle
$\bar{d}$	Average duty cycle
m_φ	Phase margin
m_g	Gain margin
u	Input vector of the state-space model
x	State vector of the state-space model
$\bar{x}$	Average state vector for state-space model linearization
y	Output vector of the state-space model
ω_c	Crossover frequency
A,B,C,D	Matrices of the state-space model
C	Bulk capacitor
C_e	External input/output capacitors
E_d	No-load voltage of the microgrid's equivalent droop-controlled generator
E_{ds}	No-load voltage chosen to control the storage converter in droop mode
F_{sw}	Switching frequency
$G_{ci1}(s)$	Transfer function of the controller for the current loop (I_{L1})
$G_{cv2}(s)$	Transfer function of the controller for the voltage loop (V_2)
$G_{p1}(s)$	Transfer function of the process (I_{L1} vs. d)
$G_{p2}(s)$	Transfer function of the process (I_2 vs. I_{L1})

I	Current supplied by the microgrid's equivalent current generator managed by the EMS
I_1	Input current (port 1, storage-side)
I_{1n}	Nominal input current (port 1, storage-side)
I_2	Output current (port 2, grid-side)
I_{2n}	Nominal output current (port 2, grid-side)
I_d	Current supplied by the microgrid's equivalent droop-controlled generator
I_{cx}	Maximum ESS charging current
I_{dx}	Maximum ESS discharging current
I_{eq}	Microgrid's equivalent current generator considered as active load in scenarios #1–#3
I_{L1}	Current of the leftmost inductor (port 1, storage-side)
I_{L10}	Average current of the leftmost inductor (port 1, storage-side)
I_{L2}	Current of the rightmost inductor (port 2, grid-side)
I_{L20}	Average current of the rightmost inductor (port 2, grid-side)
K_{ii}	Integral gain of the PI regulator of the current loop (I_{L1})
K_{iv}	Integral gain of the PI regulator of the voltage loop (V_2)
K_{pi}	Proportional gain of the PI regulator of the current loop (I_{L1})
K_{pv}	Proportional gain of the PI regulator of the voltage loop (V_2)
L	Inductor at input/output ports
P_n	Nominal power of the storage converter
R	Equivalent load resistance considered in scenarios #1–#3
R_c	Parasitic resistance of the bulk capacitor
R_d	Droop resistance of the microgrid's equivalent droop-controlled generator
R_{ds}	Droop resistance of the storage converter
R_e	Parasitic resistance of external input/output capacitors
R_L	Parasitic resistance of input/output inductors
R_n	Nominal load resistance
V_1	Input voltage (port 1, storage-side)
V_{1n}	Nominal input voltage (port 1, storage-side)
V_2	Output voltage (port 2, grid-side)
V_{2n}	Nominal output voltage (port 2, grid-side)
V_{2ref}	Reference output voltage for the storage converter (grid-side)
V_c	Voltage of the bulk capacitor
V_{c0}	Average voltage of the bulk capacitor
V_e	Voltage of the external capacitor
V_{e0}	Average voltage of the external capacitor

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