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The effects of different anode manufacturing methods on deep levels in 4H-SiC p$^+$n diodes

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ABSTRACT

The manufacture of bipolar junctions is necessary in many 4H-SiC electronic devices, e.g., junction termination extensions and p$^+$in diodes for voltage class >10 kV. However, the presence of electrically active levels in the drift layer that act as minority charge carrier lifetime killers, like the carbon vacancy (V_C), undermines device performance. In the present study, we compared p$^+$n diodes whose anodes have been manufactured by three different methods: by epitaxial growth, ion implantation, or plasma immersion ion implantation (PIII). The identification of the electrically active defects in the drift layers of these devices revealed that a substantial concentration of V_C is present in the diodes with epitaxial grown or ion implanted anode. On the other hand, no presence of V_C could be detected when the anode is formed by PIII and this is attributed to the effects of strain in the anode region. Our investigation shows that PIII can be a useful technique for the manufacture of bipolar devices with a reduced concentration of lifetime killer defects.

I. INTRODUCTION

The use of 4H-SiC bipolar devices is an attractive option for voltage classes >10 kV due to the lower on-resistance (R_{ON}) in the drift layer than their unipolar counterparts.[1] The reason for this is that 4H-SiC bipolar devices have lower static power losses unlike unipolar devices due to conductivity modulation.[2] The presence of conductivity modulation in the drift layer of p$^+$in diodes affects the forward voltage drop, but it depends on the charge carrier lifetime (τ). This, in turn, is affected by the presence of electrically active defects which behave as lifetime killers, like the carbon vacancy (V_C) and B-related defects.[2,3]

The carbon vacancy (V_C) is a negative-U defect giving rise to two electrically active levels in the bandgap (E_{gap}) of n-type 4H-SiC, the $Z_{1/2}$ and the EH6/7 at 0.65 and 1.6 eV below the conduction band edge (E_C), respectively.[4] In particular, the $Z_{1/2}$ level is a recombination center affecting τ in bipolar devices. Under certain conditions,[3] B-related centers can also act as lifetime killers. B gives rise to two levels, a shallow acceptor, found at 0.25 eV above the valence band edge (E_V) and a deeper acceptor at E_V+0.50 eV. These are related to B in a Si substitutional site (B_{Si}) and C-site (B_C),[5] respectively, with the former having an impact on τ for temperatures below ~420 K and latter remaining active up to ~570 K.[3]

While the decrease of either [B_{Si}] or [B_C] can be achieved by acting on epigrowth parameters, e.g., a high C/Si ratio decreases (increases) [B_C] ([B_{Si}]),[3] requiring custom grown 4H-SiC epilayers, the reduction of [V_C] can be performed on any as-grown 4H-SiC epilayer. This is achieved by either oxidation[6] or diffusion of implanted C[7] or annealing (1500 °C) with the use of a C-cap.[8] All of these methods are based on the diffusion of highly mobile C interstitials (C_i) that recombine with V_C (C_i+V_C →Ø).[9,10]

If on one hand decreasing [V_C] in an as-grown homoepitaxial layer is possible, on the other, it is known that device processing steps like ion implantation or high-temperature treatments lead to either the increase of the concentration[11] or to the regeneration[12] of V_C. For instance, once [V_C] is reduced by one of the methods above and the epilayer is employed for manufacturing a p$^+$n diode, Al implantation and activation (at 1700 °C), needed for anode formation, leads to the formation of V_C in the 10^{13}–10^{15} cm^{-3} range, in the implant tail region.[11] As a consequence, τ (resistivity) in the

drift layer will be reduced (increased), making the initial V_C reduction method redundant. It is then straightforward to ask whether it is possible to manufacture a p^+n diode while keeping [V_C] low in the drift layer or whether ways to reduce [V_C] during or after device processing exist or not.

In order to understand how different anode manufacturing techniques affect the presence of V_C, we carried out an electrical characterization study of three different 4H-SiC p^+n diodes. These diodes had their anodes either (a) epitaxially grown or (b) ion implanted or (c) manufactured by plasma doping (plasma immersion ion implantation or PIII). PIII is a common doping technique for flat screen display technology and for trench doping.[13,14] In the past, investigations carried out on 4H-SiC UV photodiodes showed that PIII devices gave comparable or better response than those device treated by ion beam technology.[15]

II. EXPERIMENTAL DETAILS

One set of p^+n diodes were manufactured by epitaxially growing the Al-doped p^+ anode (2×10^{18} cm^{-3}) on a 100 μm thick N-doped homoepitaxial layer (2×10^{14} cm^{-3}). Ti/W/Al ohmic contacts were deposited on the anode and Ti/W/Ni/Au contacts on the cathode. Additional details on the fabrication can be found in Ref. 16.

A second set of p^+n diodes was manufactured by using several (5 μm thick) n-type 4H-SiC homoepitaxial layer ($\sim 10^{16}$ cm^{-3}) samples and implanting them with multiple energy Al ions (total dose $\sim 10^{15}$ cm^{-2}) at 500 °C in order to form an implant box-profile. The Al as-implanted depth profile was measured by secondary ion mass spectrometry (SIMS) on a Cameca IMS-4f installation with 8 keV O^+ primary ion beam, 125 × 125 μm^2 crater width (60 × 60 μm^2 analyzed surface), and Al yield calibrated by a SiC(Al) standard. The depth scale of each SIMS spectrum is obtained as ratio between the crater depth, measured by a mechanical stylus, and the sputtering time.

A third set was fabricated by treating the surface of (5 μm thick) n-type 4H-SiC homoepitaxial layers ($\sim 10^{16}$ cm^{-3}) by BF_3 PIII (8 keV, $\sim 10^{15}$ cm^{-2}) in vacuum at RT. Some of the PIII treated samples were analyzed by SIMS, at an external company, in order to monitor the B profile, before and after heat treatments.

After Al implantation or PIII treatment, a graphitic cap was deposited on the surface of the epilayer samples. After spinning the photoresist on the epilayers, the hard bake step was carried out for 10 min at 700 °C. The C-cap is necessary to protect the surface for the subsequent high temperature treatment. Annealing was carried out in a resistive furnace, in Ar ambient, at 1700 °C for the Al implanted samples and 1600 °C for the BF_3 ones. A lower annealing temperature was chosen in the case of B-treated samples because this corresponds to a lower B diffusivity limit,[17] while still obtaining significant B activation.[18] The annealing time was set in all cases to 30 min. After removal of the graphitic cap by ashing in O_2 plasma, the samples were cleaned in buffered HF (5%) and rinsed in de-ionized water. SIMS was also carried out on some of the PIII treated and annealed samples to monitor the B profile after annealing.

Ti/Al ohmic contacts were formed on the surface of the implanted or PIII-treated samples by e-beam deposition and sintering in a rapid thermal furnace (1 min at 1000 °C). Ag paste was employed as backside ohmic contact.

Electrical characterization was carried out by Fourier-transform deep level transient spectroscopy (FT-DLTS)[19] in the 100–650 K temperature range using a reverse bias (V_R) of −1 or −3 V and a filling pulse voltage (V_P) of 1 or 3 V applied for 50 ms. In order to detect minority carrier traps, the V_P was set to 5 or 8 V.

III. RESULTS AND DISCUSSION

In Fig. 1, we show the results of the electrical characterization carried out on p^+n diode with an epitaxially grown anode. As it can be seen, the p^+n diode reveals the presence of the $Z_{1/2}$ level (8×10^{11} cm^{-3}) and of the (unresolved) EH6/7 (at ∼650 K). On the low temperature side of the DLTS spectrum, two minor DLTS peaks can be seen. However, the high level of noise made the trap parameters difficult to evaluate. One level, labeled PB1, is found at ∼180 K and located at E_C−0.33 eV with a concentration of (1.1×10^{12} cm^{-3}). Another DLTS peak, shown as a peak shoulder next to the $Z_{1/2}$ is also detected. This is labeled PB2 and found at E_C−0.51 eV (3.5×10^{11} cm^{-3}). At ∼380 and ∼500 K, two more DLTS peaks, the ON1 and ON2, respectively, are detected. Our results show that ON1 and ON2 are located at E_C−0.85 eV and E_C−1.06 eV, respectively, with ON1 having a larger concentration than ON2 (3.5×10^{11} and 1.8×10^{11} cm^{-3}). By applying a higher V_P (hole injection), we could detect three minority carrier traps: one is the B-acceptor, located at 0.30 eV above the valence band edge (E_V), with a concentration of 1.1×10^{13} cm^{-3} and then the D-center (E_V+0.60 eV, 1.5×10^{13} cm^{-3}). A minor DLTS peak can be found at ∼165 K and labeled X (E_V+0.35 eV, 1×10^{12} cm^3).

Regarding the p^+n diode with an implanted anode, we show in Fig. 2 the simulated Al concentration profile together to the results of the DLTS measurements. In Fig. 2(a), the as-implanted

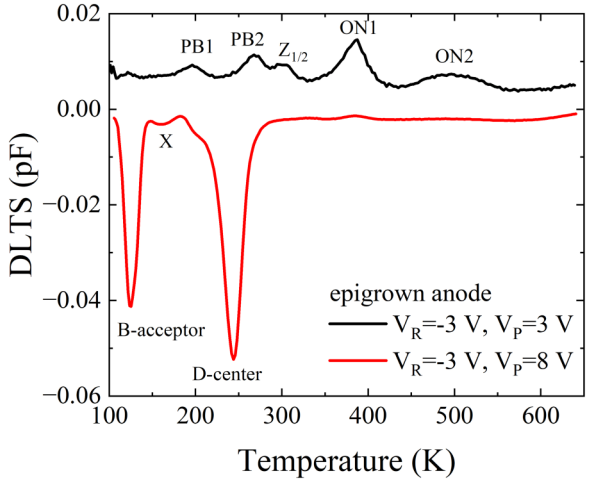

FIG. 1. DLTS spectrum of the p^+n diode with an epigrown anode, with V_P = 3 V (black solid line) and V_P = 8 V (red solid line). In the former case, the signal was magnified by ten times for visualization purposes. The period width is 0.2 s.

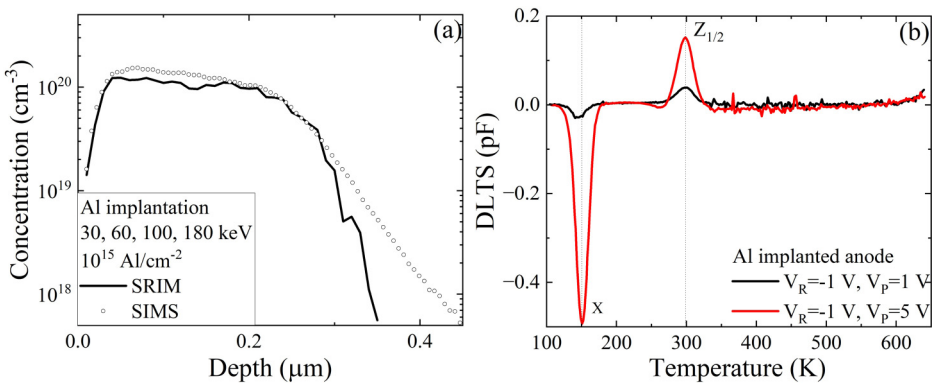

FIG. 2. (a) Simulated and measured concentration depth profile of implanted Al and (b) DLTS spectrum of the p^+n diode with an Al-implanted anode. The period width is 0.2 s.

profiles obtained by SRIM[20] and SIMS for the multiple energy Al implantation are shown. The Al profile is a box-shaped profile obtained using four different energies (total dose 1×10^{15} cm^{-2}) reaching a plateau at $\sim 10^{20}$ cm^{-3} and 0.4 μm deep. As it can be seen, a good agreement between the simulated and experimental profiles exists. In Fig. 2(b), the DLTS spectrum of the p^+n diode after implantation and annealing is displayed. As it can be seen, the DLTS reveals the presence of the $Z_{1/2}$ level (8×10^{12} cm^{-3}) and of the X center (3.4×10^{13} cm^{-3}). The same levels, with concentrations of 1.6×10^{13} and 1.7×10^{14} cm^{-3} for $Z_{1/2}$ and X center, respectively, are obtained when V_P is set to 5 V. This is consistent with the results obtained by Ayedh *et al.*[21] who observed the presence of $Z_{1/2}$ and that of a minority carrier trap, but neither B-acceptor nor D-center for increasing forward V_P. We point out that detection of minority traps during majority carrier injection can occur in the case of graded junctions.[21,22]

In Fig. 3, the B PIII concentration profile and the DLTS spectrum of the p^+n diode are shown. As it can be seen in Fig. 3(a), the PIII depth profile is different from those obtained by ion implantation. In fact, while the former can be described by using a double-exponential energetic spectrum of the boron ions,[23] the latter follows a Pearson-type distribution. As the figure shows, after PIII, the maximum B concentration reaches 10^{21} cm^{-3} at the surface of the sample and drops to 10^{16} cm^{-3} at $\sim$50 nm. In addition, very little differences are present in the B depth profile before and after annealing at 1600 °C. Figure 3(b) displays the results of the electrical characterization on the p^+n diode whose anode was formed by BF_3 PIII. The DLTS measurement reveal that no $Z_{1/2}$ level is found, whereas four levels arise at 121, 190, 380, and 490 K and identified as the OF1 (8.4×10^{11} cm^{-3}), OF2 (6×10^{11} cm^{-3}), ON1 (1.5×10^{13} cm^{-3}), and ON2 (7×10^{12} cm^{-3}). Double correlation DLTS (DDLTS) measurements (not shown) showed that the emission rates of OF1, OF2, ON1, and ON2 do not have any dependence on the electric field, in agreement with the literature. Minority carrier trap measurements show similar results to those of the epitaxially grown p^+n junction, with the presence of the B-acceptor, shoulder peak X and D-center in concentrations of 2×10^{14}, 7×10^{13}, and 3.5×10^{14} cm^{-3}, respectively.

Regarding the nature of the detected levels, the PB1 level energy position is very similar to that of the IN2 level found in dry etched 4H-SiC.[24] This level, found in the epigrown p^+n diodes, may have arisen during the use of etching for mesa formation. On the other hand, the PB2 level, which appears as a shoulder of the $Z_{1/2}$ DLTS peak, was also reported in other p^+n diodes with an epigrown anode and no hypothesis on its nature were put forward.[25]

The OF1, OF2, ON1, and ON2 are levels that are known to arise after oxidation of the epilayer. OF1 and OF2 were shown to arise after, at least, 75 min oxidation at 1290 °C and have a one-to-one correlation.[26] These two levels were associated to a

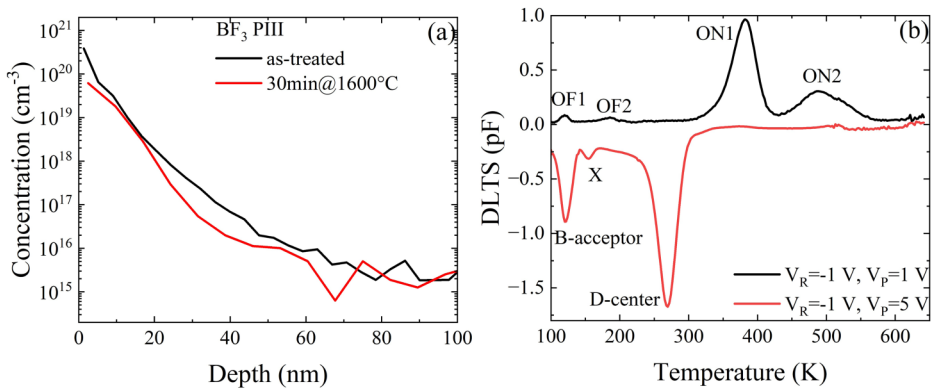

FIG. 3. (a) B concentration depth profile and (b) DLTS spectrum of the p^+n diode with a PIII-treated anode. In (b), the signal was magnified by ten times for visualization purposes. The period width is 0.2 s.

TABLE I. Summary of the majority and minority electrically active levels found in this study.

Label	Energy position (eV)	Comment
OF1	$E_C - 0.19$	Found in PIII-treated p^+n, $(C_{Si})_2$-related
OF2	$E_C - 0.24$	Idem
PB1	$E_C - 0.33$	Found in epigrown p^+n, arising after dry etching
PB2	$E_C - 0.51$	Found in epigrown p^+n, nature unknown
$Z_{1/2}$	$E_C - 0.60$	$V_C(2\text{-}/0)$
ON1	$E_C - 0.85$	Found in PIII-treated p^+n, C_i-related complex
ON2	$E_C - 1.06$	Idem
D-center	$E_V + 0.60$	B_C
X	$E_V + 0.35$	HS1 level, C_{Si}
B-acceptor	$E_V + 0.30$	B_{Si}

di-carbon antisite [$(C_{Si})2$] defect.[26] ON1 and ON2 are thermally stable up to 1700 °C, show a 1:2 concentration ratio, and have been associated to a carbon interstitial (C_i) complex defect.[27]

The level labeled B-acceptor is associated to B_{Si} and it is known to be a common impurity in 4H-SiC epilayers, originating from the graphite parts of chemical vapor deposition reactors.[3] On the other hand, the D-center was believed to be the $B_{Si}V_C$ complex.[28,29] However, recent density functional theory calculations have revealed that the D-center can be identified as the B_C.[5]

The X level can be identified as the HS1 level reported by Zhang *et al.*[30] This level was found to be suppressed for high C/Si ratio and to have a high thermal stability up to 1700 °C. The hypothesis that it could be related to a C_{Si} was also put forward.

A summary of the detected levels can be found in Table I.

Our results show the presence of the $Z_{1/2}$ level in p^+n diodes whose anode is manufactured by epigrowth or ion implantation. In both cases, since it is known that $V_C(2\text{-}/0)$ affects τ, it is desirable to avoid its presence. As expected, $[Z_{1/2}]$ is lower in the former than in the latter. This is due to Al implantation leading to a substantial concentration of V_C in the implantation tail region[11] but also to the heat treatment performed at 1700 °C that contributes to generation of V_C.[12] On the other hand, $Z_{1/2}$ is not found in the PIII-treated p^+n diode. In this diode, the OF1, OF2, ON1, and ON2 levels are also detected meaning that C_i injection has occurred in the epilayer. ON1 and ON2 were also found in the epigrown p^+n diode and, even if no details are given in Ref. 16, this may indicate that a $[V_C]$ reduction process was carried out. The presence of $Z_{1/2}$ can be attributed to processing steps like reactive ion etching for mesa formation that is known to increase $[V_C]$.[24,31]

In the case of the PIII-treated p^+n diode, the epilayers were not oxidized, so the question of the reduction of V_C arises. In order to explain this result, we consider two possibilities.

First, PIII was reported to induce strain in the PIII treated region due to the presence of interstitial species related to both B and F.[32] Strain in SiC can be correlated to the presence of native primary defects, such as vacancy and interstitials.[33] For these reasons, it can be suggested that the strain induced by PIII causes the formation of, say, C_i which diffuse in the epilayer due to high annealing temperature.

Second, PIII was followed by high-temperature annealing (but <1650 °C making thermal generation of V_C negligible[12]) with the use of a C-cap. Previous studies have shown that $[V_C]$ reduction can be achieved by C_i injection from a C-cap, even a lower annealing temperatures.[34,35]

It was reported that tensile strain can lead to a shift to lower temperature of B-related DLTS peak,[36] which is not observed in our case. This means that the present results might support the second hypothesis. However, a C-cap was also employed during annealing of the Al-implanted p^+n diode. Yet, while the presence of V_C can also be explained in terms of thermal generation,[12] the absence of both ON1 and ON2 suggests that no or rather low C_i injection has occurred. For this reason, we believe that the reduction of $[V_C]$ occurring in the PIII-treated diode might be due to a combination of the two mechanisms mentioned above.

As evident from our study, PIII can lead to the formation of p^+n diodes with low $[V_C]$ meaning that this technique can be beneficial for bipolar devices. Yet, the use of B-based PIII leads to a substantial concentration of D-center (10^{14} cm^{-3}). This level is known to also affect τ, when $[V_C]$ is low,[3] thus impacting the performance of bipolar devices. In order to overcome this issue, C-rich epilayers could possibly be employed for the manufacture of PIII p^+n diodes so that both low $[V_C]$ and $[B_C]$ could be achieved.

At last, the role of F can be discussed. The electronic properties of halogen species in 4H-SiC have not been studied in detail. It is known that Cl is a triple donor whereas F_i behaves as an acceptor.[37] Due to this, it can be thought that F_i might contribute to the formation of the p^+ layer. Unlike the case of B, not much can be said about the diffusivity of F. If this is comparable to that of Cl, annealing at 1600 °C should not contribute to the diffusion of F atoms in the epilayer.[38]

IV. CONCLUSIONS

To conclude, we compared the presence of electrically active levels in p^+n diodes whose anodes were manufactured in three different ways by epitaxial growth, ion implantation, or plasma ion implantation. We detected several majority and minority electrically active levels in the 0.19–1.06 eV below the conduction band edge and 0.3–0.6 eV above the valence band edge. It is found that the p^+n diode with an ion implanted anode reveals the highest concentration of V_C, whereas the PIII is able to decrease the concentration of V_C in the drift layer. This shows that PIII, in conjunction with annealing using a C-cap, is an effective technique for V_C reduction.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

G. Alfieri: Conceptualization (lead); Formal analysis (equal); Writing – original draft (lead); Writing – review & editing (equal). **S. Bolat:** Data curation (equal); Investigation (equal); Writing – review & editing (equal). **R. Nipoti:** Data curation (equal); Investigation (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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