Electrical probing of carrier separation in InAs/InP/GaAsSb core-dualshell nanowires

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Abstract

We investigate the tunnel coupling between the outer p-type GaAsSb shell and the n-type InAs core in catalyst-free InAs/InP/ GaAsSb core-dualshell nanowires. We present a device fabrication protocol based on wet-etching processes on selected areas of the nanostructures that enables multiple configurations of measurements in the same nanowire-based device (i.e. shell–shell, core–core and core–shell). Low-temperature (4.2 K) transport in the shell–shell configuration in nanowires with 5 nm-thick InP barrier reveals a weak negative differential resistance. Differently, when the InP barrier thickness is increased to 10 nm, this negative differential resistance is fully quenched. The electrical resistance between the InAs core and the GaAsSb shell, measured in core–shell configuration, is significantly higher with respect to the resistance of the InAs core and of the GaAsSb shell. The field effect, applied via a back-gate, has an opposite impact on the electrical transport in the core and in the shell portions. Our results show that electron and hole free carriers populate the InAs and GaAsSb regions respectively and indicate InAs/InP/GaAsSb core-dualshell nanowires as an ideal system for the investigation of the physics of interacting electrons and holes at the nanoscale.

Keywords

CORE-DUALSHELL NANOWIRES, CHARGE CARRIER SEPARATION, SEMICONDUCTOR NANOWIRES, NANOELECTRONICS

1. Introduction

In recent years, the development of III–V semiconductor nanowires (NWs) and NW heterostructures [1–4] has led to innovative building blocks to engineer unique device functionalities in nanoscale electronics, optoelectronics and photonics [1–7], exploiting for instance the high carrier mobility [8] or the possibility to engineer systems embedding tunnel junctions [9–16] or multiple tunnel barriers [17–19]. In particular, NW heterostructures with radial symmetry such as core–shell or core-multishell NWs [3, 20, 21] represent extremely promising systems for next generation electronic and optoelectronic nanodevices [22–27]. In these systems, the tunability of the band alignment by the application of a source-drain voltage and by field effect modulation opens the way to the exploration of broken-gap systems and band-to-band tunneling in Esaki diodes [23–25], as well as to the study of spin-orbit interaction [26–28]. In particular, a strong and tunable negative differential resistance (NDR) was recently demonstrated in InAs/GaSb core–shell NWs embedding a radial broken-gap heterojuction [23]. NDR is a common fingerprint of electron tunneling across a broken gap heterostructure, and it can find application in tunnel field effect transistors [13, 14] and tunnel diodes [15, 16]. In general, the availability of radial heterostructures where mobile electrons and holes coexist at equilibrium without any need of an external electric field—mimicking a bilayer system[29, 30] with circular symmetry—could open the way to novel fundamental studies on Coulomb drag phenomena in low dimensions [31] as well as to novel schemes for the detection of indirect excitons [32]. In this work, we build on our experience on core–shell nanostructures and explore the possibility to engineer and control two closely-spaced, but electrically-separated regions hosting electrons and holes. To this end, a thin InP layer was epitaxially grown between the InAs core and the GaAsSb shell, implementing a core-dualshell (CDS) NW geometry, in order to electrically insulate n-type and p-type conduction in the core and outer shell, respectively. The occurrence and magnitude of NDR is used to assess the presence of radial tunneling across the broken gap heterojunction. First, we exploit the same experimental configuration used in Ref. [23] and study the impact of the

thickness of the InP barrier on the NDR suppression. Then, we develop a fabrication protocol allowing us to selectively contact the core and the shell of the device and we fabricate NW-based devices enabling multiple measurement configurations: shell–shell (S–S), core–core (C–C), and core–shell (C–S). This allows us to measure radial and axial charge transport in the same nanostructure, and to evidence that a 10 nm-thick InP barrier effectively suppresses radial tunneling. Our experimental findings indicate a promising nanoscale system for the investigation of the coexistence of electrons and holes and of their Coulomb pairing.

2. Experimental

2.1 Growth of the core-dualshell nanowiress

Catalyst-free InAs/InP/GaAsSb CDS NWs were grown on Si(111) substrates by chemical beam epitaxy (CBE) in a Riber Compact-21 system, following the growth protocol described elsewhere [21]. In particular, we have grown two samples characterized by different thickness of the InP shell. The latter was measured using transmission electron microscopy (TEM), exploiting a JEOL JEM-2200FS microscope operated at 200 keV, equipped with an in-column Ω filter. Imaging was performed either in high resolution TEM mode combined with zero-loss energy filtering or in scanning (STEM) mode using a high angle annular dark field (HAADF) detector leading to atomic number (Z) contrast. For STEM observation, the NWs were mechanically transferred to carbon-coated copper grids. The average length of the NWs was 1.8 ± 0.2 μm. The resulting thicknesses of InP and GaAsSb shells measured from STEM images, were 5 ± 1 nm and 34 ± 4 nm for sample A, and 10 ± 1 nm and 32 ± 4 nm for sample B. Average edge-to-edge InAs core diameter was 165 ± 4 nm (facet-to-facet diameter was 143 ± 4 nm).

The chemical and structural analysis of our CDS NWs revealed that there is an As incorporation in both shells, due to the residual As background in the growth chamber while growing the shell materials [21]. This As incorporation is ≤ 10% into the InP shell, neither affecting significantly the lattice parameter nor the band structure, while it is ~ 40% in the GaSb shell, so that the actual shell composition is $GaAs_{0.4}Sb_{0.6}$. However, even if the presence of As substantially changes the GaSb lattice parameter, it does not affect significantly bandgap and band alignment. Indeed, building on the results reported in Ref. [33] we estimated low temperature bandgap and valence band offset for $GaAs_{0.4}Sb_{0.6}$ (GaSb) as 750 meV (812 meV) and −80 meV (−30 meV), respectively. Details of our calculation can be found in the Electronic Supplementary Material (ESM).

2.1 Device fabrication and architectures

InAs/InP/GaAsSb CDS NWs were dry-transferred onto a SiO_2/Si^{++} (300 nm/500 μm) substrate and electrical contacts were fabricated using aligned electron beam lithography (EBL). We fabricated a first set of devices with a pair of electrodes placed onto the GaAsSb shell, enabling the configuration of measure hereby referred to as "shell–shell" (S–S). Native oxide was removed from the contact areas of the nanostructure using a $HCl:H_2O$ (1:2) wet etching step (lasting for 30 s, stopped in H_2O); Ni/Au (10/300 nm) electrodes were deposited by thermal evaporation. Successively, we fabricated a second set of devices equipped with four electrodes, enabling in the same nanostructure three possible configurations of measurement, hereby referred to as "shell–shell", "core–core" (C–C), and "core–shell" (C–S). To this end, we developed a fabrication protocol including an additional etching step to remove the GaAsSb shell and the InP barrier from both ends of the NW, uncovering the InAs core (see Section 2.3). After this etching step, we used $HCl:H_2O$ (1:2) to remove the native oxide in one single step from four selected areas, namely two areas on the GaAsSb shell and the two ends of the InAs core. Finally, we evaporated the metallic electrodes. This allowed us to selectively and independently contact the core and the shell of our InAs/InP/GaAsSb CDS NWs.

2.2 Etching protocol

The etching step mentioned in the previous section was crucial to the fabrication of the four electrical contacts allowing for different configurations of measurement (S–S, C–S and C–C). In order to develop a successful etching protocol, one has to take into account several aspects including the NW geometry, the resist adhesion and type. In general, relatively long-time etching is undesirable, since it increases the probability of etchant infiltration under the resist that should protect the NW regions from the chemical etching. In our case, this effect can be even exacerbated by the geometry of our CDS NWs that typically display twelve facets [21], yielding to a relatively small contact area between the NW and the Si/SiO_2 substrate. In the following, we report in detail the entire etching protocol used in

this work. The SiO_2/Si^{++} substrate used for device fabrication was baked at 180 °C for 15 min; then, an adhesion layer (AR 300-80) was spin-coated, baked at 150 °C for 2 min, then soaked in acetone for 4 min in order to reduce its thickness and remove the molecules unbound to the substrate, and finally baked a second time at 150 °C for 5 min (to desorb residual moisture and volatile residuals). NWs were dry- transferred onto the substrate, and an additional layer of adhesion promoter AR 300-80 was spin-coated and baked afterward. Finally, a layer of CSAR 62 resist was spin coated, and EBL was used to define the areas that have to be exposed to the etching solution. Our choice of the resist was motivated by the empirical observation that both basic and acidic solutions of etching display marked tendency to react destructively with conventional electron beam resist (PMMA AR-P 679.04). After EBL, CSAR 62 was developed in AR 600-546 for 1 min and then baked at 130 °C for 1 min. This baking step was found to be crucial to minimize the infiltration of the etchant underneath the resist mask. Finally, the NW regions, not protected by the resist mask, were exposed to $HCl:H_2O_2:H_2O$ (5:2:50) for 1 min and rinsed in H_2O for 30 s. This procedure allows to remove both GaAsSb and InP shells in a single step. We calibrated the etching time by monitoring the NW thickness with scanning electron microscopy (SEM) during a sequence of etching steps. In general, HCl-based etchant solutions typically display higher selectivity to GaSb with respect to InAs [34]. Keeping all this into account, we etched the NW selected areas down to a diameter of approximately 150 nm: In this way we avoid detrimental effects on the InAs core morphology.

3 Results and discussion

Charge transport in our InAs/InP/GaAsSb CDS NW-based devices was measured between room temperature (RT) and 4.2 K. Current–voltage (*I*–*V*) characteristics were measured using a DL1211 current preamplifier, while a Keithley 2614B power supply was used to control the back gate voltage bias.

3.1 Charge transport in two-contact devices: role of the InP barrier thickness

To investigate the impact of the InP shell on the electronic transport in our InAs/InP/GaAsSb CDS NWs (Fig. 1(a)), we first measured two-terminal devices fabricated with individual NWs from the two samples (referred to as sample A and B) grown with different InP-barrier thicknesses. Figures 1(b) and 1(c) display STEM micrographs of InAs/InP/GaAsSb CDS NWs from sample A and sample B, characterized by 5 nm-thick and 10 nm-thick InP barriers, respectively. A false color SEM micrograph of one of our prototypical devices is shown in Fig. 1(d): Two electrical contacts (yellow colored) were evaporated onto the outmost GaAsSb shell (pink colored), enabling the measurement of electrical transport in the S–S geometry. Figure1(e) shows a schematic of the device architecture as well as the setup used to measure the *I*–*V* characteristics of the device in S–S configuration. The two electrodes allow to measure the electrical resistance and to estimate the impact of a voltage bias applied to the degenerately-doped Si^{++} back-layer of the SiO_2/Si^{++} substrate. The latter acts as a back-gate and modulates the transport properties of the heterostructure. The *I*–*V* characteristics measured at RT in the S–S geometry in all our devices were linear in a drain-source voltage $|V_{SD}|$ range well exceeding 200 mV; the electrical resistance was ranging typically from 10 to 70 kΩ in different devices, indicating a very good quality of the metal-semiconductor interface; the resistance of devices with 10 nm InP barrier was slightly higher with respect to that of the devices with a 5 nm InP barrier (see the ESM).

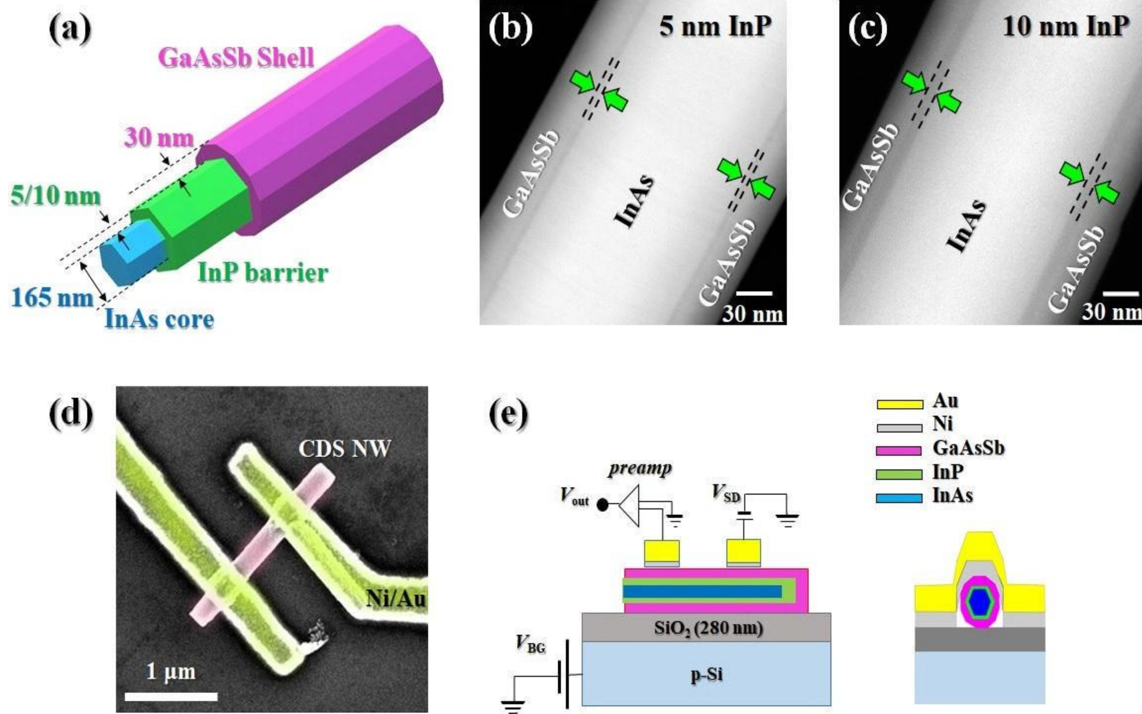

Figure 1 (a) Schematic of InAs/InP/GaAsSb core-dualshell (CDS) nanowire. STEM micrographs of CDS NWs with (b) 5 ± 1 nm and (c) 10 ± 1 nm-thick InP barrier; arrows highlight the thickness of the InP shell. (d) Top view SEM image of one of our shell-shell devices fabricated onto a SiO_2/p-Si substrate. Purple and yellow colors correspond to GaAsSb shell and Au electrodes, respectively. (e)-left: schematic of the device architecture, with the circuit for transport experiments in shell–shell configuration (two-wires) depicted in overlay. (e)-right: schematic of a contact cross-section.

Figure 2(a) reports a set of I–V characteristics measured at 4.2 K in the S–S geometry for NWs from sample A (5 nm-thick InP shell) in the V_{SD} range from −0.75 V to +0.75 V, for different applied back-gate voltages V_{BG} in the range from −40 to + 40 V. The I–V curves reveal the occurrence of NDR at $|V_{SD}| \approx 0.6$V: this phenomenology can be ascribed to the Esaki effect in presence of direct tunneling through the thin InP barrier. In particular, the observation of NDR for both positive and negative values of V_{SD} is consistent with the presence of two radial back-to-back Esaki-like diodes, as widely discussed for InAs/GaSb NW-based devices in our previous work [23]. In the present case, however, the nonlinear feature (NDR) occurring in the I–V curves is quantitatively different with respect to the case of InAs/GaSb NWs. In fact, at $V_{BG} = 0$ V the NDR occurs at larger source-drain bias voltage ($|V_{SD}| \approx 0.6$ in Fig. 1(a)), while the overall impact of the application of a back-gate voltage is significantly weaker. Indeed, both the position of the NDR as well as the peak-to-valley ratio (PVR) are poorly modulated by the application of a back-gate voltage, ranging from $V_{SD} = 0.52$ V and PVR = 1.16 at $V_{BG} = -40$ V to $V_{SD} = 0.60$ V and PVR = 1.13 at $V_{BG} = +40$ V. We notice a V_{BG} dependence consistent with a p-type semiconductor. We will address this point in more detail later in Section 3.2. In all our devices we observed this behavior, with NDR occurring in the range $|V_{SD}| \approx$ 0.3–0.6 V and weak PVR (see the ESM). We rationalize these experimental evidences taking into account that the InP barrier introduces an additional load resistance in series with the non-linear components (InAs-GaAsSb junction), setting NDR at larger source-drain bias with respect to the case of study reported in Ref. [23], and reducing the impact of the field effect. Regarding the different features of the NDRs reported for opposite V_{SD} in Fig. 2(a), these can be tentatively ascribed to non-idealities of the heterojunctions. In an ideal device, one could feature a uniform band alignment along the azimuthal angle of the NW, yielding to identical NDR features for

opposite V_{SD}. In a real device, any local built-in disorder or slight asymmetry in the electrical contacts may lead to nonuniformities of the junctions or to NDR conditions locally occurring at different values of V_{SD}. On top of this, nonuniformity in the junction can be affected by the back-gate, due to its asymmetry with respect to the NW center that yields to a different impact on the NW facets for a given S-D bias (particularly in the case of the top and bottom facets).

Figure 2(b) reports two *I–V* curves at 4.2 K and V_{BG} = 0 V, measured in the V_{SD} range from −0.8 V to +0.8 V in the S–S configuration for two different devices: the black curve refers to a device fabricated with a 5 nm-barrier CDS NW (sample A), while the red curve corresponds to a 10 nm-barrier CDS NW (sample B). We estimated the device resistance from the linear fit of the two *I–V* characteristics for $|V_{DS}|$ > 0.6 V, and we obtained ~ 2 MΩ for device with type A NW and 5 MΩ for device with type B NW. The key qualitative difference between the black and red curves concerns the presence of NDR: increasing the InP shell thickness is found to completely suppress this characteristic nonlinear feature. At 4.2 K, we measured more than 10 devices for both samples. We systematically observed that devices with NWs of sample B are more resistive (by factor two or three) with respect to devices with NWs of sample A. Besides, they did not show NDR but a monotonic increase of $|I_{SD}|$ for increasing $|V_{SD}|$. Moreover, we measured the *I–V* characteristics of devices with NWs of sample B as a function of temperature, and we observed that NDR was quenched in the entire temperature range from 300 to 4.2 K. A selection of these results is reported in the ESM.

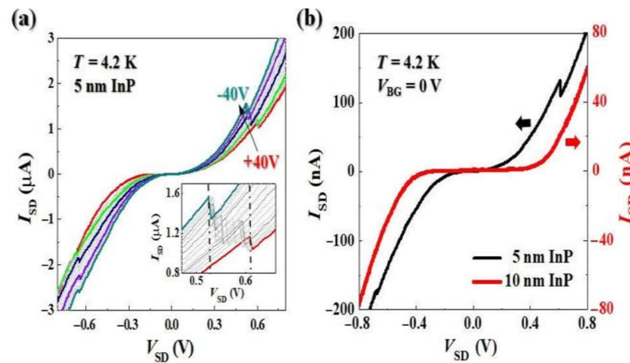

Figure 2 Transport properties of InAs/InP/GaAsSb CDS NW-based devices measured in S-S geometry at 4.2 K. (a) *I–V* characteristic of a NW-based device with 5 nm-thick InP, at different back gate voltages. (Inset) Magnification of *I–V* curves in the V_{SD} region displaying negative differential resistance. (b) The comparison between the *I–V* characteristics of devices characterized by 5 nm-thick (black curve) and 10 nm-thick (red curve) InP shell, with V_{BG} = 0V.

On the one hand, our results suggest the absence of tunneling across the 10 nm-thick InP shell (sample B) and consequently indicates that only the GaAsSb shell contributes to the conduction. On the other hand, in general when measuring two-contact devices in the S–S configuration, it is not trivial to exactly visualize the charge trajectories, identifying the possible contributions to the current arising from the GaAsSb shell, the InAs core and the InP barrier. In order to tackle this point, starting from InAs/InP/GaAsSb CDS NWs of sample B, as already mentioned we fabricated four-terminal devices that allow us to measure independently in the same nanostructure the electrical resistance of the InAs core (C–C), of the GaAsSb shell (S–S), and across the InAs/InP/GaAsSb heterojunction (C–S).

3.2 Charge transport in four-contact devices with 10 nm InP barrier

We exploited the methods and protocols detailed in Section 2 to fabricate four-contact devices, enabling to measure charge transport in a single InAs/InP/GaAsSb CDS NW of sample B using multiple configurations. This target was achieved by selectively exposing to the etching solution both ends of the InAs/InP/GaAsSb CDS NW. Figure 3(a) shows the pictorial view of a CDS NW before (left panel) and after (right panel) the etching step. Preliminary to the fabrication and measurement of four-contact devices, we apply our etching protocol to remove both GaAsSb and InP shells exclusively from one end of InAs/InP/GaAsSb CDS NWs. Figure 3(b) reports the SEM

micrograph (top view) of a CDS NW where, at one end, the InAs core (blue colored area) is set free from the InP barrier and the GaAsSb shell (violet colored area). Noticeably, the minimized etchant infiltration allows to remove the shells from well-defined regions and with a relatively sharp interface between the pristine and etched regions. Figure 3(c) reports a top-view SEM micrograph of an InAs/InP/GaAsSb CDS NW where GaAsSb shell and InP were removed at both ends of the CDS in a single etching step, and shows the high control of the etching procedure on selective areas of InAs/InP/GaAsSb CDS NWs. This provided the key step for the fabrication of four- contact devices allowing to probe the charge transport in the InAs core, in the GaAsSb shell and across the series of radial heterojunctions (InAs/InP and InP/GaAsSb).

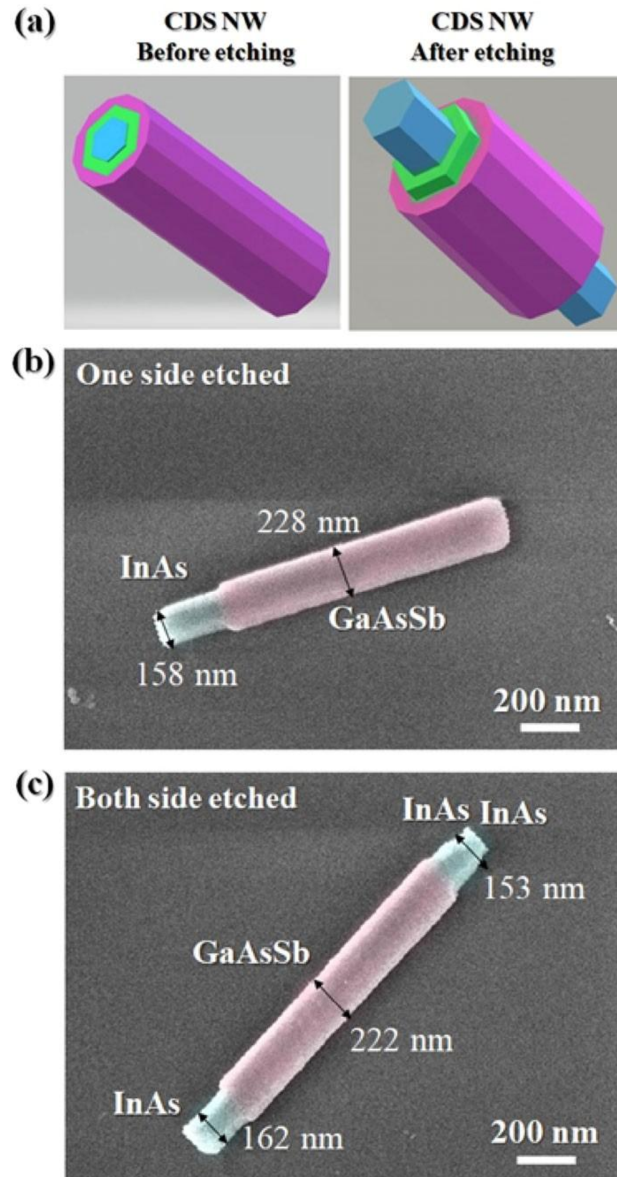

Figure 3 (a) Sketch of CDS NWs with 12 facets, before (left panel) and after (right panel) etching. SEM images of (b) one side etched and (c) two sides etched nanowires used for the fabrication of multiple electrodes device architectures; pink and blue colors correspond to GaAsSb shell and InAs core, respectively.

Figure 4(a) reports a false color SEM micrograph (top-view) of one of our four-contact devices fabricated starting from individual InAs/InP/GaAsSb CDS NWs of sample B. Electrodes 1–4 provide electrical contact to the bare InAs core, while contacts 2–3 are connected to the GaAsSb shell. Two different cross-sectional views of our devices are schematically depicted in Fig. 4(b), with color code accounting for the different materials. With this device architecture, in the same CDS NW, axial charge transport can be measured across the GaAsSb shell using contacts 2–3 and across the InAs core using contacts 1–4, while radial transport across the multiple heterojunction can be measured using contacts 1–2 (or 3–4). Besides, the application of a voltage bias to the degenerately doped silicon of the SiO_2/Si^{++} substrate allows to probe field-effect modulation in any of the three configurations mentioned above.

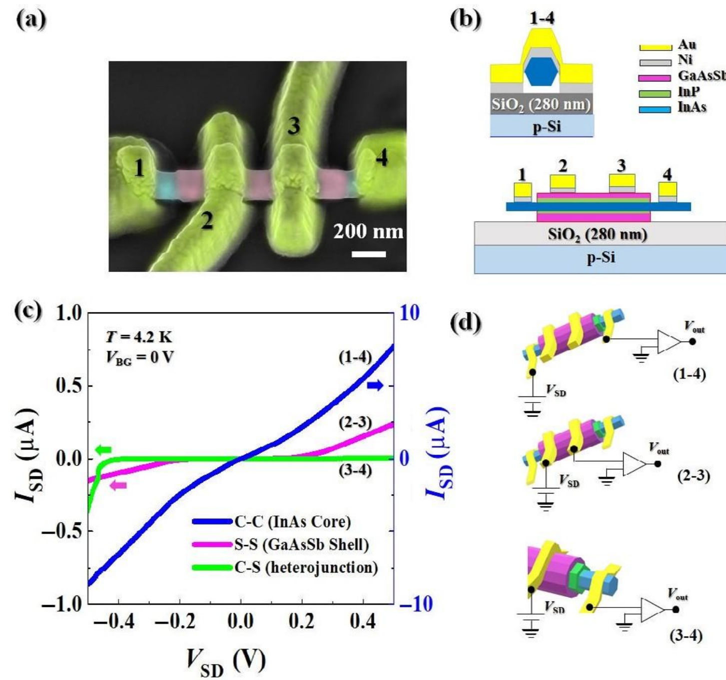

Figure 4 (a) SEM image of one of the investigated InAs/InP/GaAsSb CDS NW-based devices allowing measurements with multiple contact configurations in the same nanostructure. Purple, green, blue and yellow colors correspond to GaAsSb shell, InP barrier, InAs core and metallic electrodes, respectively. (b) Schematic of device architecture and a device cross-section. (c) *I*–*V* characteristics measured in the same nanostructure with different configurations, namely core–core (blue curve), shell–shell (pink curve) and core-shell (green curve), at $V_{BG} = 0$ V and at 4.2 K the left *y*-scale corresponds to the S–S and C–S curves, while the right *y*-scale is related to the C–C curve. (d) Device architecture with circuit in overlay, corresponding to the three different configuration of measurement.

Figure 4(c) reports three different *I*–*V* characteristics, measured at 4.2 K with applied V_{SD} in the range from −0.5 to +0.5 V, in the same InAs/InP/GaAsSb CDS NW-based exploiting the three different measurement geometries enabled by our device architecture; the left *y*-scale corresponds to the S–S and C–S curves, while the right *y*-scale is related to the C–C curve; the circuits corresponding to the different geometries are schematically depicted in Fig. 4(d). The blue curve shown in Fig. 4(c) was measured in the InAs core (C–C) using contacts 1–4 and displays a symmetric and almost-linear behavior. It corresponds to a relatively low resistance (60 kΩ). The pink curve is measured in the GaAsSb shell (S–S configuration) using contacts 2–3, and in the linear region for $|V_{SD}| > 0.3$ V corresponds to a resistance of about 1 MΩ. The green curve is measured in C–S configuration using contacts 3–4 and it displays marked asymmetry as well as significantly higher resistance: In this configuration charge carriers must cross the insulating InP barrier.

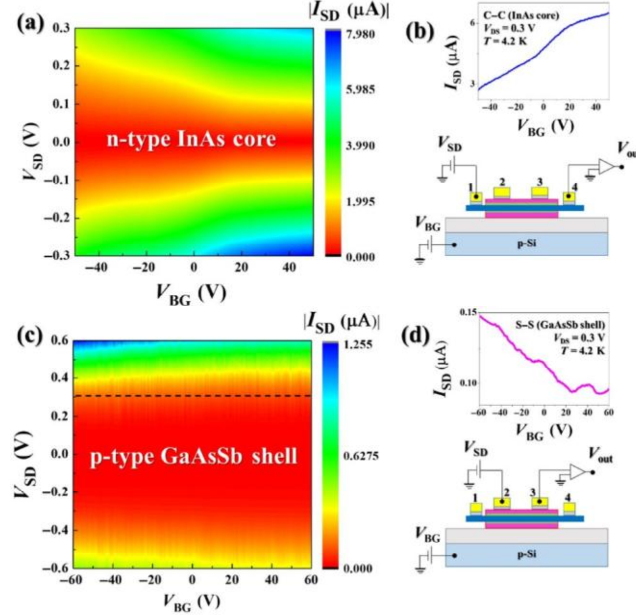

Figure 5 (a) Current map measured in the InAs core (C–C configuration) as a function of V_{BG} and V_{SD} at 4.2 K. (b)-top: n-type transconductance curve extracted from the map in panel (a) for V_{SD} = 0.3 V. (b)-bottom: schematic of the C–C measurement configuration. (c) Current map measured in the GaAsSb outer shell (S–S configuration) as a function of V_{BG} and V_{SD} at 4.2 K. (d)-top: p-type transconductance curve extracted from the map in panel (c) for V_{SD} = 0.3 V. (d)-bottom: schematic of the S–S measurement configuration.

The back-gate modulation of charge transport in the InAs core and in the GaAsSb shell is reported in Fig. 5, and clearly reveals that InAs is n-type while GaAsSb is p-type. Figures 5(a) and 5(c) show two current maps measured at 4.2 K in the same InAs/InP/GaAsSb CDS NW-based device, respectively with C–C and S–S measurement configuration, as function of the V_{SD} and applied V_{BG}. The circuits used to measure the two current maps in the two configurations are schematically depicted in Figs. 5(b) and 5(d). The InAs core clearly behaves as a n-type field effect transistor: its transconductance curve measured at V_{SD} = 0.3 V is reported in Fig. 5(b)-top graph. The GaAsSb shell exhibits instead a behavior consistent with a p-type doping, as results from the transconductance curve measured at V_{SD} = 0.3 V reported in Fig. 5(d)-top. Interestingly, the observation of almost linear *I*–*V* curves for the C–C configuration (with low electrical resistance at 4.2 K), together with the opposite behavior observed for C–C versus S–S configuration upon the application of V_{BG}, are consistent with the occurrence of good ohmic contacts between the evaporated metals and the InAs semiconductor.

4 Conclusions

In conclusion, starting from catalyst-free InAs/InP/GaAsSb CDS NWs, we fabricated two-probe and four-probe electronic devices allowing to investigate the impact of InP barriers on the charge-transport properties of the nanostructures. Measuring in shell–shell geometry, we showed that a 10 nm-thick InP barrier effectively suppressed the conduction band-to-valence band tunneling between the InAs core and outer GaAsSb shell. Thanks to the four-terminal device architecture, in the same nanostructure we independently measured charge transport across the outer GaAsSb shell, the inner InAs core, and across the radial heterojunction. Our results obtained in C–S geometry proved that radial tunneling across the InP barrier yielded asymmetric *I*–*V* curves and high electrical resistance, impressively larger respect to the resistance measured axially in the InAs core and in the GaAsSb shell of the NW. Moreover, field effect modulation of charge transport in our devices indicates n- and p-type nature of the InAs core and the GaAsSb shell, respectively. The present results demonstrate that a thin radial insulating barrier epitaxially grown between the n-type core and the p-type shell of a CDS NW efficiently quenches the tunnel coupling between electrons and holes located in the two axial channels. The InAs/InP/GaAsSb CDS-NW-based device reported hereby behaves as a multifunctional device that allows for axial transport in two parallel semiconductor channels with opposite doping, together with radial transport across the two channels. This result suggests that our

InAs/InP/GaAsSb CDS NW-based devices may represent a suitable platform for engineering Coulomb-coupled electron-hole systems in individual nanostructures.

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Electronic Supplementary Material: Supplementary material (*I–V* characteristic of two-contact devices with 5 and 10 nm InP barrier as a function of temperature and back gate, SEM images, Bandgap and valence band offset calculations) is available in the online version of this article at https://doi.org/10.1007/ s12274-020-2745-5.

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