RESEARCH ARTICLE | OCTOBER 07 2024

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AIP Advances 14, 105109 (2024)
https://doi.org/10.1063/5.0228323

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Cite as: AIP Advances 14, 105109 (2024); doi: 10.1063/5.0228323
Submitted: 2 August 2024 • Accepted: 18 September 2024 •
Published Online: 7 October 2024

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ABSTRACT

Vertical Metal–Insulator–Semiconductor (MIS) capacitors with an Al_2O_3 thin film as a gate insulator have been fabricated on homoepitaxial GaN-on-GaN samples. The effect of the annealing treatments on the MIS characteristics has been investigated exploring two different approaches: Post-insulator-Deposition-Annealing (PDA) and Post-gate-Metallization-Annealing (PMA), i.e., annealing on the bare Al_2O_3 layer and annealing after the gate metallization deposition on Al_2O_3. The direct comparison between PDA and PMA is crucial to understand the impact of the metal/dielectric interface quality on the behavior of the Al_2O_3/GaN MIS capacitors. The efficacy of annealing has been monitored as a function of metal gates having different work functions: nickel (Ni), molybdenum (Mo), and tantalum (Ta). It has been found that both PDA and PMA approaches are equally able to improve the Al_2O_3/GaN interface electrical quality. However, the PMA demonstrates an additional beneficial effect on the metal/Al_2O_3 interface. In particular, the possible chemical reactions activated by the annealing process at the metal/dielectric interface can perturb the known metal/dielectric dipole responsible for Fermi-level pinning phenomena, causing a positive shift of the flat voltage (V_{FB}), which depends on the metal, and approaching the theoretical value in the case of Mo and Ta.

Gallium nitride (GaN) and related materials have attracted the interest of the power electronics community for more than a decade. In particular, lateral devices based on AlGaN/GaN heterojunctions have been extensively explored because of the peculiar high-density and high-mobility two-dimensional electron gas (2DEG).[1–3] However, the lateral topology of GaN-based transistors grown on foreign substrates (e.g., Si, SiC, and sapphire) exhibits some inherent limitations related to the high on-resistance (R_{ON}), low breakdown (V_{BD}) and threshold (V_{th}) voltages, current collapse phenomena at surface states, etc.[4–7] For this reason, at present, an increasing attention is focused on the development of vertical devices based on homoepitaxial GaN-on-GaN,[8,9] due the superior crystal quality and lower dislocation density (<10^6 cm^{-2}) compared with heteroepitaxial GaN.[10–12]

In vertical GaN devices, the breakdown voltage (also exceeding 1 kV) is sustained by tens of micrometers thick drift layers, and the maximum electric field is vertically distributed far from the surface, thus significantly reducing trapping phenomena and dynamic on-resistance effects due to surface states. Moreover, vertical GaN transistors may provide a high positive threshold voltage (V_{Th}) and high current density, whereas the uniformly distributed electric field and current spread result in better heat dissipation.[13–17]

In this context, the development of vertical GaN power metal oxide semiconductor field effect transistors (MOSFETs) passes through the availability of a good dielectric/GaN interface, characterized by low defect density in order to guarantee a high channel mobility and device reliability. Unfortunately, GaN has no good quality native oxide, and hence, deposited oxides must be adopted. A high dielectric constant (κ), high critical breakdown electric field E_{BD}, and large band offset to the GaN are the requirements of the ideal gate insulator to effectively limit leakage current and, finally, power dissipation.[18–20] In this context, Al_2O_3 is a particularly promising dielectric due to its relatively high relative permittivity κ (κ = 9), high breakdown electric field (7–8 MV/cm), and suitable conduction band offset to GaN (1.6 eV).[21,22] Atomic layer deposition (ALD), with its nanometric thickness control, uniformity, and conformity, is undoubtedly the ideal technique to grow insulating layers inside the grooved vertical GaN trench-MOSFET[14] and FinFET.[23] However, the as-deposited Al_2O_3 on GaN by ALD is known to suffer from the presence of charges and interface traps, which affect the electrical behavior of metal/Al_2O_3/GaN metal–insulator–semiconductor (MIS) devices in terms of both flat-band voltage (V_{FB}) shift and stretching of the capacitance–voltage (C–V) characteristics.[21,24–25] To mitigate these issues, various thermal annealing strategies are currently explored at different stages of the MIS device fabrication, either after the ALD deposition[18] [Post-Deposition-Annealing (PDA)] or after the deposition of the metal gate [Post-Metallization-Annealing (PMA)].[19]

Tadmor *et al.*[26] suggested that the annealing process of Al_2O_3/GaN systems should not exceed 550 °C to avoid the Al_2O_3 degradation as the CV-instability demonstrated. In this perspective, Hashizume *et al.*[20,27] treated the Al_2O_3/GaN system to a PMA process at 300–400 °C in N_2, demonstrating that such a treatment is beneficial for the electrical performance of the dielectric/GaN system inducing a notable decrease in the interface trap density (D_{it}). Similarly, Ando *et al.*[28] found that PMA treatments at 400 °C in N_2 are effective to reduce D_{it} at the Al_2O_3/GaN interface. Moreover, Hung *et al.*[29] found that the reduction in the interface charges by PMA treatments also results in the decreasing gate leakage current. Other studies demonstrated the beneficial effect of PMA treatments to minimize the interface trap states at the Al_2O_3/GaN interface.[25,30,31] However, they only focused on the properties of the Al_2O_3 layer and Al_2O_3/GaN interface, without investigating the possible effects that the PMA approach can have on the metal and on the metal/Al_2O_3 interface of the MIS capacitor.

In this context, it is clear that a unique path toward an ideal Al_2O_3/GaN interface is not yet set. In particular, the comprehension of each single effect that may impact the electrical properties of the Al_2O_3/GaN MIS structure is not yet obtained.

In this article, the direct comparison between PDA and PMA allowed us to highlight the impact of the metal/dielectric interface quality on the behavior of Al_2O_3/GaN MIS capacitors. This aspect is often underrated and only partially addressed. In particular, the comparison among metal gate contacts with different work-functions and electro-affinities [nickel (Ni), molybdenum (Mo), and tantalum (Ta)] enabled us to distinguish the charge-trapping phenomena occurring inside the insulator and at the interface with the semiconductor but also the annealing treatment effect on the metal/dielectric interface as a function of the metal nature.

Vertical MIS capacitors [Fig. 1(a)] have been fabricated on an n-type GaN epitaxial layer ($N_D \sim 2 \times 10^{16}$ cm^{-3}) grown on 5 μm of conductive GaN bulk substrate ($N_D \sim 10^{19}$ cm^{-3}). The epitaxial layer was grown by MOCVD (Metal Organic Chemical Vapor Deposition) in a close-coupled showerhead reactor, using ammonia, trimethylgallium, and hydrogen carrier gas. The x-ray diffraction rocking curves confirmed the lattice matching between the epilayer and the substrate, being the full width at half maximum (FWHM) of the (103) diffraction peak less than 120 arcsec. A Ti/Al/Ni/Au Ohmic contact has been formed on the substrate's back side using DC magnetron sputtering followed by annealing at 800 °C.[32] After the cleaning of the GaN surface in a HF:HCl mixture (essential to remove both native oxide and carbon contaminations), ~30 nm of Al_2O_3 has been grown by plasma enhanced atomic layer deposition (PE-ALD). Deposition details and process parameters have been already reported in Ref. 22.

According to the schematic flowchart reported in Fig. 1(c), PDA and PMA have been carried out at 400 °C in N_2 for 5 min immediately after Al_2O_3 deposition and metal sputtering, respectively. Different dimensions (side square of 100, 200, 300, and 400 μm) of Ni, Mo, and Ta metal gates [Fig. 1(b)] have been defined by optical photolithography and lift-off. The electrical behavior of the MIS capacitors has been evaluated by capacitance–voltage (C–V) measurements in a CASCADE

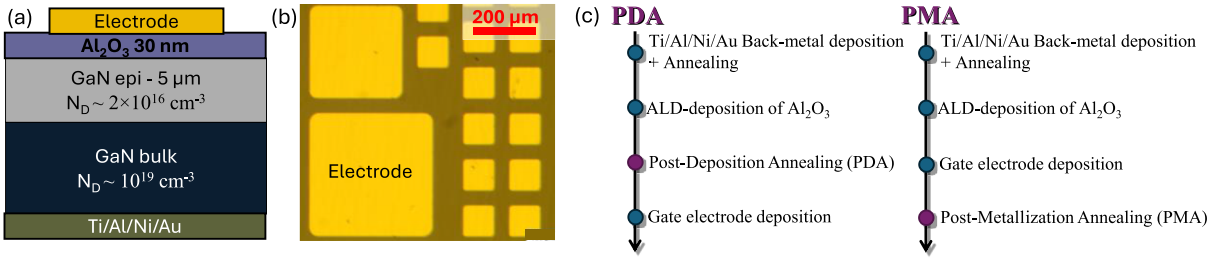

FIG. 1. Schematic cross section of the metal/Al_2O_3/GaN-on-GaN MIS capacitor (a), top-view optical microscopy image of different size MIS capacitors (b), and schematic flow chart of PDA and PMA treatments (c).

Microtech probe station, using a Keysight B1505A parameter analyzer.

The C–V curves of the MIS capacitors acquired at a frequency of 1 kHz, before (As-Dep) and after PDA and PMA, are displayed in Fig. 2, for different metal gates: Ni (a), Mo (b), and Ta (c). These graphs report also the theoretical C–V curves calculated by assuming the GaN electron affinity of 4.1 eV, and the commonly reported metal work functions (Φ_{Ni} = 5.15 eV, Φ_{Mo} = 4.6 eV, Φ_{Ta} = 4.25 eV).[33] The values of the metal work function were experimentally verified by the Kelvin-probe force microscopy measurements, reported in the supplementary material (see Fig. S1). All three as-deposited systems exhibit C–V curves characterized by an evident hump between −2 and −1 V, which disappears after either PDA or PMA treatments. Hence, this hump that stretched the C–V curves can be attributed to charge trapping occurring at the Al_2O_3/GaN interface whose quality clearly improves after the application of a thermal budget (regardless of PDA or PMA).[19,20,28,29] This is quantitatively illustrated in Figs. 2(d)–2(f), reporting the energy distribution of the interface trap densities (D_{it}), calculated by Terman's method on 1 kHz C–V curves.[33] Interestingly, the distribution of the interface state density exhibits the same behavior independently of the metal gate, and it is characterized by a notable decrease in D_{it} at about 0.2 eV below the GaN conduction band edge. In fact, D_{it} decreases from 1 × 10^{13} cm^{-2} eV^{-1} down to 3.5–4 × 10^{12} cm^{-2} eV^{-1}, with a minimum value of 9–7 × 10^{10} cm^{-2} eV^{-1}, for all systems after both annealings. These findings are in agreement with previous studies demonstrating that, regardless of the annealing atmosphere, the thermal treatments of oxide/GaN systems are able to improve the interface quality by saturating the Ga-dangling bonds left during the superficial cleaning process of GaN[34,35] and that occurring during the early stage of the ALD growth.[36]

Moreover, paying attention to Figs. 2(a)–2(c), it is possible to observe that both the as-deposited and PDA C–V curves are negatively shifted compared to the theoretical ones. This shift of the flat band voltage V_{FB} can be justified in different ways. A first and straightforward explanation for the V_{FB} shift would be entirely due to the presence of positive fixed charges inside Al_2O_3.

However, the flat band V_{FB} is a function of different parameters as described by the following relation:

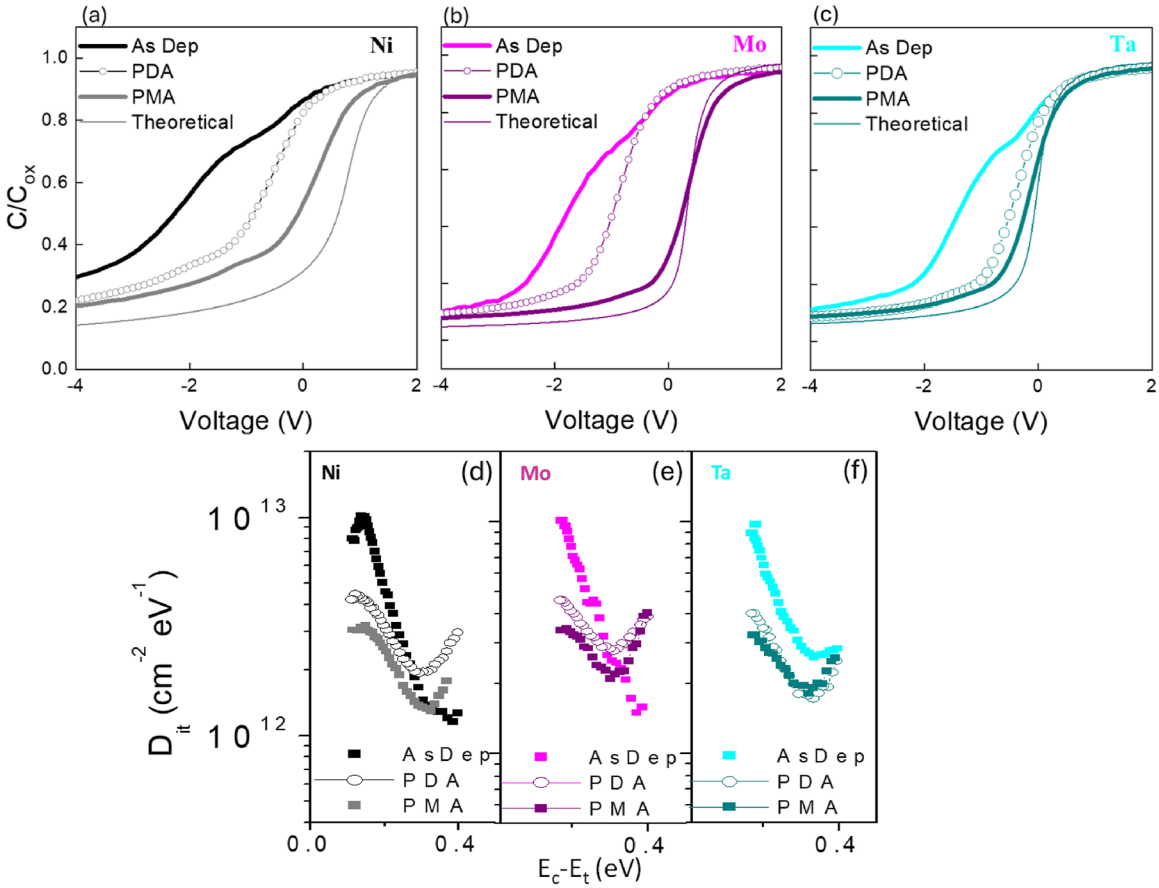

FIG. 2. C–V curves of As-Dep (solid line), PDA (circle line), and PMA (dashed line) metal/Al_2O_3/GaN-on-GaN capacitors with nickel (a), molybdenum (b), and tantalum (c) as a metal gate. Interface state density D_{it} distribution of As-Dep, PDA, and PMA metal/Al_2O_3/GaN-on-GaN MIS capacitors with nickel (d), molybdenum (e), and tantalum (f) as a metal gate.

$$V_{FB} = \Phi - (\chi + E_g/2 + 0.0259 \ln(N_D/n_i)), \quad (1)$$

where Φ is the metal work function, χ is the GaN electronic affinity, E_g is the GaN bandgap, and N_D and n_i are the GaN epilayer donors' concentration and the intrinsic carrier concentration, respectively. Accordingly, another possibility to justify the V_{FB} shift could be also an effective metal work function ($\Phi_{Eff,M}$) different from the vacuum work functions (Φ_{ThM}), which has been used to calculate the theoretical C–V curves.

It should be noted that if the negative V_{FB} shift would be only due to positive fixed charges inside the dielectric, an identical V_{FB} shift should be expected for all three metal gate electrodes, since the Al_2O_3 layer has been deposited under the same conditions and annealed using the same operative parameters, for all three systems. However, as can be seen by Table I, the shifts change as a function of the metal gate electrode. This suggests that besides that the fixed charge inside the dielectric also the charges at the metal/dielectric interface affect the V_{FB} shift.

In this regard, Yeo *et al.*[37] clearly demonstrated that the work function of a metal gate electrode in contact with a high-k dielectric is not the same vacuum work function, but its value changes from the theoretical ones. In fact, when a metal approaches a dielectric material, it produces the so-called "metal-induced gap states" in the bandgap of the dielectric.[38] The charge transfer phenomena at these interfaces create an interfacial dipole that drives the band alignment between the metal and dielectric until a zero-dipole charge position is reached so that the Fermi level E_F of the metal moves toward the charge neutrality level E_{CNL} of the dielectric (Fermi-level pinning). Therefore, the effective metal work function differs from the vacuum metal work function and, consequently, the experimental V_{FB} is shifted with respect to the theoretical one.[37–39]

Based on this phenomenon, also our experimental C–V curves, negatively shifted with respect to the theoretical ones, can be explained by the Fermi-level pinning simply occurring for the contact between the metal and dielectric. Moreover, carefully looking at our experimental As-Dep and PDA C–V curves, they overlap from the accumulation to the onset of the above-described hump, beyond which the PDA capacitor appears more positively shifted. The presence of this hump does not actually allow to us evaluate if a real V_{FB} shift between the As-Dep and PDA devices exists. Instead, the C–V curves of PMA are evidently positively shifted,[19,20] and more importantly, they tend to approach the V_{FB} of the theoretical curves (V_{ThFB}). The possible reason is schematically illustrated in Figs. 3(a) and 3(b). As cited above,[37–39] when metal gate electrodes are in contact with high-K dielectrics [Fig. 3(a)], the dipole generated at the interface produces Fermi-level pinning and the effective work functions $\Phi_{Eff,M}$ differ from their vacuum work function $\Phi_{Th,M}$; thus, the V_{FB} shift is a direct consequence. As can be observed in Fig. 3(a), all three metal gate electrodes used in this work are characterized by reduced $\Phi_{Eff,M}$ than $\Phi_{Th,M}$. Moreover, they tend toward a similar energy level value, which should be the E_{CNL} of the dielectric. However, when PMA processes are carried out, the possible chemical reactions activated at metal/oxide interface can perturb the interfacial dipole, partially or totally removing the Fermi-level pinning phenomena [Fig. 3(b)] and finally restoring the V_{FB} toward the theoretical value. However, the V_{FB} shift toward the theoretical value changes as a function of the metal gate electrode (Table I). While

TABLE I. PDA-Th V_{FB} shift and PMA-Th V_{FB} shift of all three metal gates: Ni, Mo, and Ta.

System	PDA-Th ΔV_{FB} (V)	PMA-Th ΔV_{FB} (V)
Ni	1.4	0.3
Mo	1.1	0
Ta	0.5	0

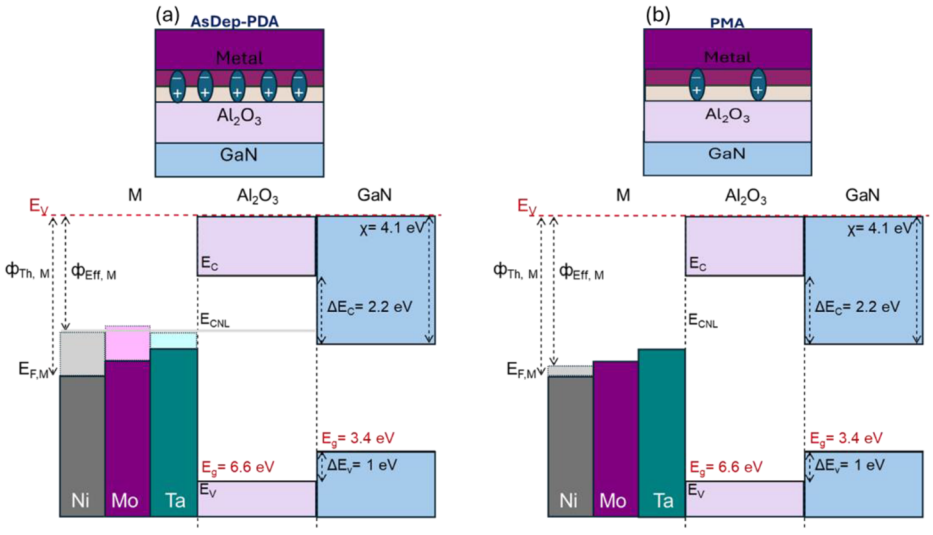

FIG. 3. Schematic of the interfacial metal/Al_2O_3 dipole and of the consequent Fermi-level pinning for the as-deposited and PDA systems (a). Schematic of the perturbed interfacial metal/Al_2O_3 dipole and of the consequent partially or totally removed Fermi-level pinning after PMA treatment (b).

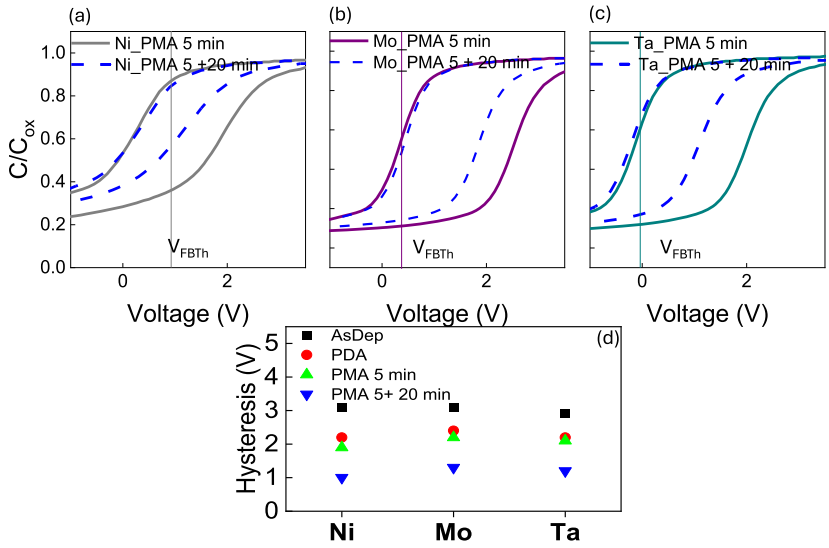

FIG. 4. C–V curves of 5 min and 5 + 20 min PMA of metal/Al_2O_3/GaN-on-GaN MIS capacitors with Ni (a), Mo (b), and Ta (c) as a metal gate. Summary of the C–V hysteresis amount between the different treatments and metals (d).

for Mo and Ta metal gate electrodes, the PMA treatment is able to almost totally restore the theoretical V_{FB}, for Ni, it occurs only partially [Fig. 2(a)]. This different behavior can be correlated with the different nature of the metal gate electrode. In this regard, it has been demonstrated that metals characterized by high work function do not easily react with oxygen.[40] This suggests that Ni, characterized by higher work function than Mo and Ta, poorly react with the underlying oxide layer during the annealing process, producing a less effective perturbation of the dipole and finally of the V_{FB} shift.

The possible impact of longer PMA treatments (5 + 20 min) on the V_{FB} shift has been also investigated for all three systems, and the corresponding C–V curves are shown in Figs. 4(a)–4(c). Interestingly, for all three metals, the C–V curves remain almost unchanged in terms of V_{FB}, independent of the annealing time (5 min or 5 + 20 min).

On the other hand, the PMA duration strongly impacts the hysteresis value of C–V curves acquired considering forward and backward sweep. As clearly reported in Fig. 4(d), the As-Dep capacitors exhibit a significant hysteresis around 3 V because of the charge-trapping phenomena by the electrically active defects inside the high-κ and at the interface, generally known as oxide-charge traps.[41,42] PDA and PMA approaches are similarly beneficial to reduce the hysteresis phenomena toward a value of about 2 V. This means that, regardless of the procedure, the annealing process is useful to suppress oxide-charge traps and finally to mitigate the charge trapping phenomena. Moreover, increasing the PMA period up to 20 min, the hysteresis value is further reduced by about 1 V for all metal gate electrodes. Hence, considering that the C–V hysteresis is ascribable to the quality of the entire dielectric layer, it cannot be ruled out that a further increase in the annealing time may lead to an additional reduction of the trapping phenomena.

In conclusion, in order to understand the impact of the metal/dielectric interface quality on the behavior of the Al_2O_3/GaN MIS capacitors, two different annealing approaches have been investigated: PDA and PMA, i.e., annealing on the bare Al_2O_3 layer and annealing after the gate metallization deposition on Al_2O_3. Both PDA and PMA showed similar improvements of the Al_2O_3/GaN interface quality, by reducing the D_{it} values, and they also improved the dielectric quality, decreasing the hysteresis. However, differently from PDA, the PMA treatment gives an additional beneficial effect on the metal/dielectric interface. In fact, PMA approaches have been found to be able to stabilize V_{FB}, shifting this toward the theoretical value. We attribute this beneficial effect to the possible chemical reactions activated by the annealing process at the metal/dielectric interface, which can perturb the known metal/dielectric dipole responsible for Fermi-level pinning phenomena and consequently the V_{FB} shift than the theoretical value. However, the response to PMA treatment is a function of the used metal gate. In this regard, we found that the Ni metal gate, characterized by higher work function than Mo and Ta, does not reach the theoretical V_{FB} even after 5 + 20 min long PMA treatment. This could be due to its lower tendency to react with the underlying oxide during the annealing process.

The supplementary material provides the values of the metal work function experimentally verified by the Kelvin-probe force microscopy measurements.

This work was carried out in the framework of the European Project GaN4AP (Gallium Nitride for Advanced Power Applications), receiving funding from the Electronic Component Systems for European Leadership Joint Undertaking (ECSEL JU), under Grant Agreement No. 101007310. Moreover, partial support by the European Union (NextGeneration EU), through the MUR PNRR project SAMOTHRACE (Grant Nos. PNRR-M4C2 and ECS00000022), is acknowledged.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Emanuela Schilirò: Conceptualization (equal); Data curation (equal); Investigation (equal); Methodology (equal); Writing – original draft (equal). **Giuseppe Greco**: Investigation (equal); Methodology (equal). **Patrick Fiorenza**: Conceptualization (equal); Investigation (equal); Methodology (equal). **Salvatore Ethan Panasci**: Investigation (equal). **Salvatore Di Franco**: Investigation (equal). **Yvon Cordier**: Visualization (equal). **Eric Frayssinet**: Visualization (equal). **Raffaella Lo Nigro**: Conceptualization (equal); Methodology (equal); Writing – review & editing (equal). **Filippo Giannazzo**: Conceptualization (equal); Methodology (equal); Writing – review & editing (equal). **Fabrizio Roccaforte**: Conceptualization (lead); Funding acquisition (lead); Methodology (lead); Project administration (lead); Resources (lead); Supervision (lead); Validation (lead); Writing – review & editing (lead).

DATA AVAILABILITY

The data that support the findings of this study are available within the article and its supplementary material.

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