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RESEARCH ARTICLE

# Investigating Mesa Structure Impact on C-V Measurements

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**ABSTRACT** Capacitance-voltage (C-V) measurements play a crucial role in evaluating semiconductor device performance by revealing vital parameters such as doping levels and charge carrier behavior. This study specifically investigates the impact of mesa structures on C-V measurements in 4H-SiC PiN vertical diodes. Our analysis uncovers distinct capacitance values per unit area among diodes with varying diameters within the same diode family. These findings underscore the limitations of conventional capacitance equations formulated for planar devices when extended to mesa-structured devices. To separate the capacitance portion dependent solely on the PN junction's area from the overall depletion capacitance, which is influenced by the device's geometry, we applied a methodology involving multiple C-V measurements across diodes with differing diameters and validated the experimental outcomes through rigorous calculations. This enables the utilization of standard capacitance equations. Neglecting the impact of device geometry has the potential to introduce significant inaccuracies in critical device parameters. The proposed methodology addresses these limitations, offering valuable insights to enhance the accuracy of extracted quantities from C-V measurements. Furthermore, it provides guidance for interpreting experimental data obtained from devices incorporating mesa structures.

**INDEX TERMS** Capacitance-voltage measurements, depletion capacitance, doping estimation, diode, mesa structures, PN junction, silicon carbide.

## I. INTRODUCTION

Capacitance-Voltage (C-V) measurements play a crucial role in semiconductor device characterization, offering insights into key performance parameters such as interface quality, depletion region properties, charge carrier behavior, doping levels, and built-in potential [1]. The diverse techniques within C-V measurements, ranging from evaluating doping profiles [2] and band-offsets [3] to analyzing steady and transient capacitance for deep-level impurity characterization [4], [5], share a common underlying necessity: they require the assessment of capacitance arising from charge within the space charge region at specific voltage levels.

Furthermore, it is crucial to acknowledge that the capacitance can be affected by the existence of a mesa structure within the device, which is the central focus of this study.

More specifically, we delve into the effects of the mesa structure on the distribution of charges within the device and how this, in turn, influences the resulting capacitance values. Consequently, this influence directly affects the precision of estimates derived from this capacitance for various quantities. For instance, the built-in voltage and the doping level, as well as quantities indirectly dependent on them, such as estimating defect concentration through DLTS measurements [6] or transient CV measurements, which necessitate knowledge of the substrate doping, or in assessing the distribution of the reduced lifetime region in irradiated diodes [7].

To enhance the precision of these evaluations, we have introduced a method involving multiple C-V measurements across diodes with varying diameters and validated the experimental procedure results with calculations.

## II. DEVICE UNDER STUDY

The studied devices are vertical mesa PiN diodes of cylindrical shape with anode diameters varying from 200 to 700 $\mu$m

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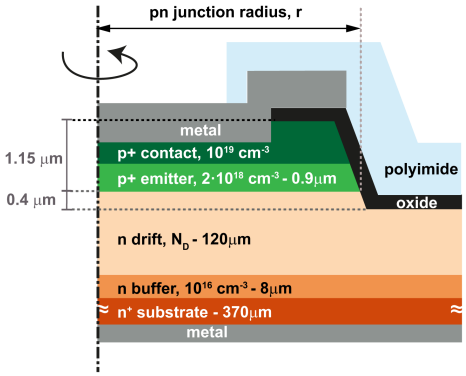


**FIGURE 1.** Cylindrical diodes' half cross-section, with a dash-dot line denoting the central axis of symmetry. Mesa etchings along the diode periphery and the anode are identified through SEM observations.

fabricated on homo-epitaxial 4H-SiC wafer housed in 2.5 mm × 2.5 mm square chip [8]. Half the cross-section of the diode, as determined through analysis using Secondary Electron Microscopy (SEM) of a cross-sectioned specimen, is sketched in Fig. 1. The doping values and types of the homo-epitaxial and bulk layers were obtained from the SiC wafer data sheet.

We performed C-V measurements on diodes of different diameters, in the bias range from −20 V to +2.4 V, using an HP4284A LCR meter operating at a frequency of 1 MHz, with an oscillator level of 200 mV, and with a residual stray capacitance estimated to be < 0.1 pF. All measurements were conducted at 20±2°C.

C-V measurements were conducted to assess the doping profile of the n-type epilayer and the built-in potential values.

## III. RESULTS AND DISCUSSION

### A. C-V CURVES

As known, the depletion-layer capacitance of a PN junction with uniform doping profiles, can be calculated using the following formula [9]:

$$C(V) = AC_A(V) = A\left[\frac{q\varepsilon_{SiC}}{2\left(\frac{1}{N_D}+\frac{1}{N_A}\right)(\varphi_{bi}-V)}\right]^{\frac{1}{2}} = A\frac{\varepsilon_{SiC}}{X_D} \quad (1)$$

here $\varepsilon_{SiC}$ is the electrical permittivity of the semiconductor, $q$ the electron charge, $\varphi_{bi}$ the built-in potential, $X_D$ the depletion region width, $A$ the junction area, $C_A$ the depletion-layer capacitance per unit area, V the reverse bias voltage.

If the doping is uniform, the slope of $1/C^2$ versus the reverse bias voltage should be a straight line whose slope is relate to the doping, whereas the intercept of the straight line with the voltage axis should give the $\varphi_{bi}$.

For one-sided abrupt junction, that is a strongly asymmetric junction, i.e., $N_A \gg N_D$ as for diodes in this study, the doping of the n-side of the junction can be calculated from (1) as:

$$N_D = -\frac{2}{\varepsilon_{SiC}q}\left[\frac{d\left(1/C_A^2\right)}{dV}\right]^{-1} \quad (2)$$

Equation (1) employs the parallel plate capacitor approximation, treating the depletion region as a capacitor formed between P-type and N-type semiconductor regions. This model assumes a uniform depletion region with a constant electric field across the entire width [6]. However, the diodes under examination have a mesa structure (refer to Fig. 1).

Our main objective was to assess the suitability of equation (1) in interpreting C-V measurements for mesa-structured diodes under study.

We initiated the analysis by examining the capacitance values obtained at V = 0 V in diodes of different diameters, C(V = 0V).

If (1) were valid, the ratio of C(V = 0 V) to A (with A representing the junction area calculated as $\pi r^2$, and r the radius shown in Fig. 1), would have remained constant, since C(V = 0 V)/A coincided with $C_A$ in (1).

However, the data presented in Table 1 clearly demonstrate that this is not the case.

**TABLE 1.** Measured capacitance-to-area-ratio for diodes of various diameters calculated at 0 V.

| Radius, r (μm) | P-N junction area A= πr²(x10⁻³ cm²) | C(V=0V)/A (nF/cm²) |
|---|---|---|
| 100 | 0.314 | 3.95 |
| 150 | 0.706 | 2.90 |
| 200 | 1.256 | 2.52 |
| 250 | 1.962 | 2.32 |
| 300 | 2.826 | 2.23 |
| 350 | 3.846 | 2.18 |

To investigate the potential impact of the device geometry on the C-V characteristics, we graphed C(V)/A ratio against 1/r, as depicted in Fig. 2 for the two cases of 0 V and −3 V. Remarkably, the experimental data points align very well with a parabolic function described by the equation:

$$C(V)/\pi r^2 = \alpha(V) + \frac{\beta(V)}{r} + \frac{\gamma(V)}{r^2} \quad (3)$$

The identical correlation holds for negative applied voltages. The parameters $\alpha$, $\beta$ and $\gamma$ exhibit voltage dependency, as demonstrated in table 2; derived through interpolation of experimental results using (3) at various voltage levels.

In (3), the term $\alpha$ corresponds to the depletion-layer capacitance component that is solely dependent the PN-junction area, i.e. $C_A(V)$ in (1), while the terms $\beta$ and $\gamma$ are dependent on the device's geometry. At V = 0 V, the obtained $C_A = 1.95$ nF/cm².

To establish a link between the experimental law and the diode's geometry, we calculated the diode capacitance by accounting for a generic mesa structure depicted in Fig. 3,

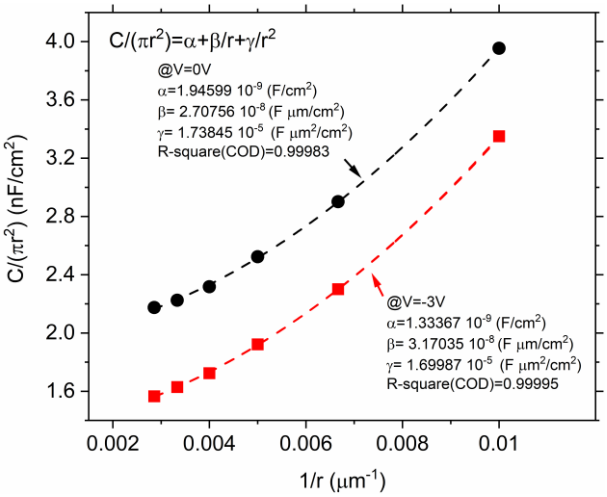


**FIGURE 2.** Measured capacitance at 0V (dots) and −3V (squares) over the junction area in diodes of different diameters, versus 1/r, with r the PN junction radius, and fitting equation $\alpha + \beta/r + \gamma/r^2$ (dashed lines).

**TABLE 2.** Fitting parameters obtained from the interpolation of the measured capacitances at different voltages with (3).

| Voltage (V) | α (nF/cm²) | β (nF·μm/cm²) | γ (μF·μm²/cm²) |
|---|---|---|---|
| 0 | 1.95 | 27.1 | 17.4 |
| -0.5 | 1.78 | 29.0 | 17.2 |
| -1 | 1.65 | 30.3 | 17.2 |
| -1.5 | 1.55 | 31.1 | 17.1 |
| -2 | 1.46 | 31.7 | 17.0 |
| -2.5 | 1.39 | 31.7 | 17.0 |
| -3 | 1.33 | 31.7 | 17.0 |

which also includes the parameters used in the computation. The calculation steps are detailed in the appendix.

Below, the resulting equation is provided for the case of $X_n > h$ as for diodes of this study:

$$\frac{C(V)}{\pi \cdot r^2} = \alpha(V) + \frac{\beta(V)}{r} + \frac{\gamma(V)}{r^2} = \frac{\varepsilon_{SiC}}{X_D} + \frac{qN_D X'_D(\pi(X_D - h) + 2l)}{r} + \frac{qN_D X'_D(\pi(X_D - h)l + l^2)}{r^2} \quad (4)$$

where $X'_D$ is the derivative of the depletion region width, $X_D$, with respect to voltage (the expressions of $X_D$ and $X'_D$ are reported in the appendix), while l and h are parameters associated with the mesa's geometry, as depicted in Fig. 3.

$C_A(V)$, which coincides with $\alpha(V)$ in (4), can therefore be calculated as:

$$C_A(V) = \frac{C(V)}{\pi \cdot r^2} - \frac{\beta(V)}{r} - \frac{\gamma(V)}{r^2} \quad (5)$$

### B. DOPING EXTRACTION

The doping concentration $N_D(V)$ can be determined by (2) based on the values of $C_A(V)$. However, to obtain $C_A(V)$ from (5) would require extract $\beta$ and $\gamma$ at all voltages, that would make the process challenging to implement. One viable approach could be to use for both $\beta$ and $\gamma$ the values calculated at 0 V, neglecting their dependency on voltage.

Using measured data in table 2, we calculated the relative error incurred when calculating $C_A(V)$ with (5) accounting for the dependency of $\beta$ and $\gamma$ on voltage compared to assuming $\beta$ and $\gamma$ remain constant at V = 0 V, finding a maximum relative error < 1%.

Hence, we compute the value of $C_A(V)$ based on (5), while assuming the values of $\beta$ and $\gamma$ at 0 V; that $C_A(V)$ is finally used to calculate the doping $N_D(V)$ with (2).

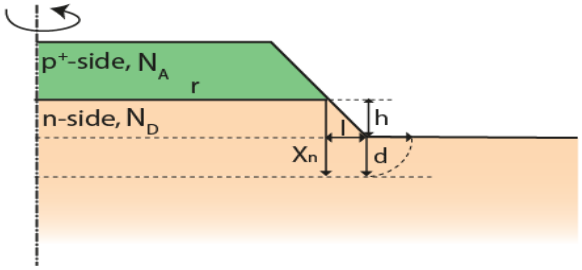


**FIGURE 3.** Cross-sectional view of the diode region with the PN junction, illustrating the extension of the n-side depletion region (d = $X_n$-h) both vertically and laterally beyond the mesa etch surface for depletion capacitance computation.

Fig. 4 illustrates the doping concentration $N_D(V)$ for diodes of largest and smallest diameter calculated with the described procedure (solid lines) and the standard approach (dashed lines).

As the forward bias approaches the $\varphi_{bi}$, the significance of the diffusion capacitance renders the employed capacitance model and the corresponding $N_D$ invalid.

With the proposed approach, the calculated doping concentration in the epilayer for both diode diameters closely approximates $N_D \sim 1.5 \cdot 10^{14}$ cm$^{-3}$ and remains uniform for negative applied biased, that is, increasingly deeper into the epitaxial layer (solid lines).

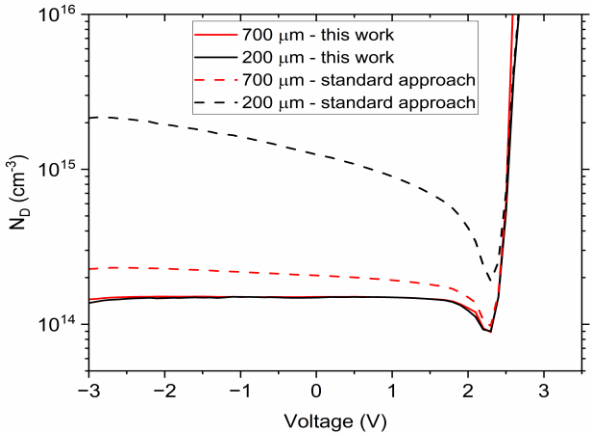


**FIGURE 4.** Doping concentration within the epilayer, $N_D(V)$, versus voltage, computed directly from measured capacitance C(V) (standard approach), or derived from $C_A(V)$ using (2) (this work).

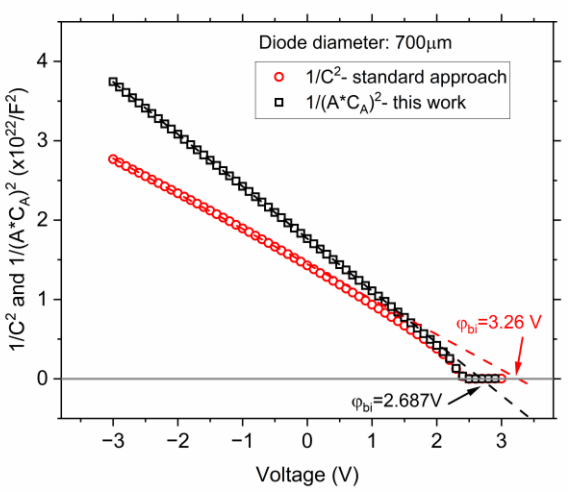


**FIGURE 5.** Built-in potential, $\varphi_{bi}$, computed directly from measured capacitance, $1/C^2$ (red circles, standard approach), or derived from $1/(A{\cdot}C_A)^2$ using (2) (black squares, this work). C represents the measured capacitance, whereas $C_A$ represents the depletion-layer capacitance component solely dependent on the PN-junction area, calculated using (5).

However, disregarding the contribution to depletion-layer capacitance associated with the diode's geometry, such as in the case of measuring a single-diameter diode, would result in the doping profiles shown by the dashed lines in Fig. 4. Notably, doping appears to be non-uniform within the epitaxial layer, also exhibiting different values for the two diodes.

The largest error in doping estimation is observed in the case of the smaller diameter diode, where factors like $\beta/r$ and $\gamma/r^2$ in (5) exert a more significant influence, leading to an ∼700% error in doping estimation at 0 V. This error diminishes in the larger diameter diode scenario but remains at approximately 33% at 0 V.

### C. BUILT-IN VOLTAGE EXTRACTION

Similarly, we computed the built-in potential by plotting $1/C^2$ versus the reverse bias voltage utilizing both the measured capacitance and the $C_A(V)$ calculated as in (5): the extrapolation of $1/C^2$ to 0 should provide the built-in potential. Fig. 5 illustrates the plotted curves for a diode measuring 700 $\mu$m in diameter. Disregarding the influences tied to the diode's geometry results in a relative error of ∼22% in estimating the built-in potential.

## IV. CONCLUSION

During our investigation into reverse-bias capacitance measurements in SiC vertical PiN diodes of varying diameters and featuring mesa structures, we observed the limitations of employing the traditional voltage-dependent capacitance equation designed for planar device in doping extraction. Notably, distinct values of capacitance per unit area (C/A) were obtained in diodes of different diameters within the same sample.

To explore the potential influence of device geometry on the measured capacitance (C), we plotted the C/A ratio against the reciprocal of the PN junction radius (1/r). This analysis revealed a quadratic relationship between these parameters, enabling the determination of the depletion capacitance component solely associated with the PN junction area. This approach allows for the extraction of doping and built-in potential parameters using standard expressions calculated for a planar device.

To interpret the observed experimental trend, we derived expressions for capacitance as functions of geometric parameters. These calculations provide a valuable tool for interpreting experimental data obtained from devices featuring mesa structures.

Furthermore, we demonstrated that neglecting the impact of device geometry can introduce significant errors in doping estimation and the evaluation of the built-in potential. This oversight potentially compromises the accuracy of parameters dependent on these quantities. To address these limitations, we propose a methodology to mitigate such errors.

## APPENDIX
## DEPLETION-LAYER CAPACITANCE VS VOLTAGE CALCULATION

The methodology employed to derive the mathematical expression for interpreting experimental capacitance values is detailed in the following.

Fig. 3 illustrates half of the cross-section of the cylindrical diodes along the longitudinal axis of symmetry, displaying the PN junction and the mesa structure. $N_A$ and $N_D$ are the p- and n-type doping, $r$ the PN junction radius, $X_D$ the depletion region width, $d$ denotes the portion of the depletion region extending both laterally and vertically beneath the mesa etching surface.

The depletion region width of a planar PN junction is a function of the applied reverse-bias voltage, V, and can be calculated as [9] and [10]:

$$X_D(V) = \left[\frac{2\varepsilon_{SiC}}{q}\left(\frac{1}{N_D}+\frac{1}{N_A}\right)(\varphi_{bi}-V)\right]^{1/2} \tag{A1}$$

where $\varphi_{bi}$ is the built-in voltage, $q$ the elementary electron charge, and $\varepsilon_{SiC}$ the dielectric constant of semiconductor, the Silicon Carbide for the studied devices.

In the case of an asymmetrical junction, as in the studied diodes, the depletion region primarily extends into the low-doped side of the junction, namely the n-side, $X_n(V)$, of expression:

$$X_n(V) = \frac{X_D(V)}{1+\frac{N_D}{N_A}} \tag{A2}$$

Under the approximation of fully depleted region [9], [10], the total charge of depletion region in the n-side of the diode can be calculated as $Q_{TOT} = q{\cdot}N_D{\cdot}V_{TOT}$, where $V_{TOT}$ is the total volume depleted of charge.

$V_{TOT}$ can be calculated as the sum of different contributions, as sketched in Fig. 6. We considered two main cases:

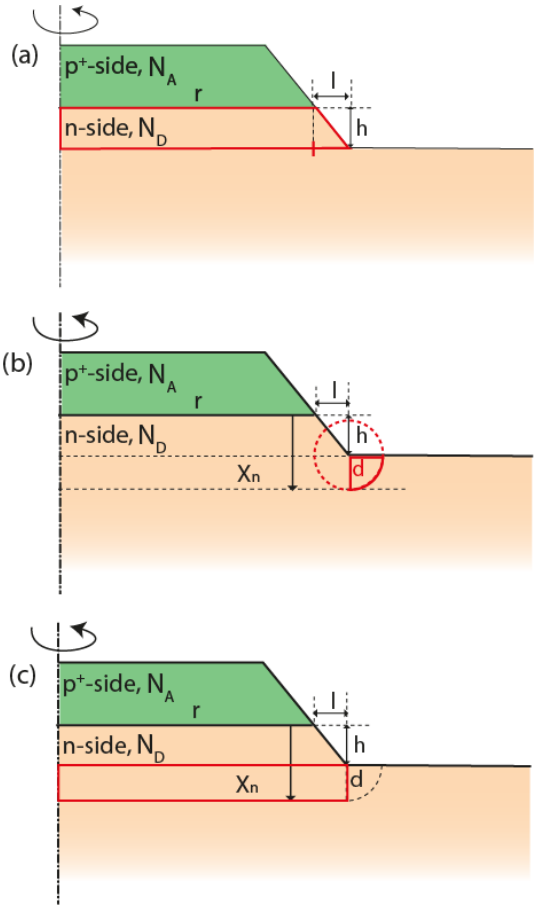


**FIGURE 6.** Half-section of the diode region featuring the PN junction: the actual 3D structure is formed by rotating this section around the longitudinal axis of the cylindrical diode (dashed-dotted line). In the figure $X_n > h$, and $d = X_n - h$.

### A. $X_n > h$

The first volume contribution is from the truncated cone formed by rotating a trapezoid with bases of lengths r and R (where R = r + l) and a height of h, as highlighted in Fig. 6(a):

$$V_{TC} = \frac{\pi h(r^2 + R^2 + rR)}{3} \tag{A3}$$

The second contribution stems from rotating a circle, centered at R (= r + l) with a radius of d as depicted in Fig. 6(b), which forms a torus. As only a quarter of the circle, highlighted in continuous line in Fig. 6(b), contributes to the depleted region, the second addition to $V_{TOT}$ is determined as follows:

$$V_T = \frac{\pi^2 R d^2}{2} \tag{A4}$$

The third contribution arises from rotating a rectangle with sides of length R (= r + l) and d around the vertical longitudinal axis of symmetry, as illustrated in Fig. 6(c). This rotation generates the volume of a cylinder, which is:

$$V_C = \pi R^2 d \tag{A5}$$

Summing up the three contributions results in $V_{TOT} = V_{TC} + V_T + V_C$.

The capacitance can be calculated as the derivative of the total charge in the n-side with respect to voltage [10], that is:

$$C = \left|\frac{dQ_{TOT}}{dV}\right| = \left|\frac{qN_D dV_{TOT}}{dV}\right| = \left|qN_D\left[\frac{dV_{TC}}{dV} + \frac{dV_T}{dV} + \frac{dV_C}{dV}\right]\right| \tag{A6}$$

where:

$$\frac{dV_{TC}}{dV} = \frac{d}{dV}\left[\frac{\pi h(r^2 + (r+l)^2 + r(r+l))}{3}\right] = 0 \tag{A6a}$$

$$\frac{dV_T}{dV} = \frac{d}{dV}\left[\frac{\pi^2 (r+l)(X_n - h)^2}{2}\right] = \pi^2 (r+l)(X_n - h) X_n' \tag{A6b}$$

$$\frac{dV_C}{dV} = \frac{d}{dV}\left[\pi (r+l)^2 (X_n - h)\right] = \pi (r+l)^2 X_n' \tag{A6c}$$

From (A1) and (A2) derive that:

$$X_n' = \frac{\frac{dX_D}{dV}}{1 + \frac{N_D}{N_A}} = -\frac{\varepsilon_{SiC}}{qN_D X_D} \tag{A7}$$

The depletion-layer capacitance per unit area is thus calculated from (A6) divided by the junction area, $\pi \cdot r^2$, after replacing the derivatives with the results in (A6a), (A6b) and (A6c).

After isolating the terms dependent on 1/r and $1/r^2$, and those unaffected by the PN junction radius, the following expression emerges:

$$\frac{C(V)}{\pi r^2} = \left|qN_D\left[X_n' + \frac{X_n'}{r}(\pi (X_n - h) + 2l) + \frac{X_n'}{r^2}\left(\pi (X_n - h) l + l^2\right)\right]\right| = \alpha + \frac{\beta}{r} + \frac{\gamma}{r^2} \tag{A8}$$

In particular:

$$\alpha = qN_D |X_n'| = \frac{\varepsilon_{SiC}}{X_D} = C_A(V) \tag{A8a}$$

$$\beta = qN_D |X_n'| (\pi (X_n - h) + 2l) \tag{A8b}$$

$$\gamma = qN_D |X_n'| \left(\pi (X_n - h) l + l^2\right) \tag{A8c}$$

where $\alpha$ is the component of the capacitance per unit area, $C_A$, which is independent of $r$.

Under the premise of an abrupt junction, specifically with $N_A \gg N_D$, (A2) reduces to (A9) [9]:

$$X_n(V) = \frac{X_D(V)}{1 + \frac{N_D}{N_A}} \approx X_D(V) \approx \left[\frac{2\varepsilon_{SiC}}{q}\left(\frac{1}{N_D}\right)(\varphi_{bi} - V)\right]^{1/2} \tag{A9}$$

Consistently, the expressions (A8a), (A8b) and (A8c) can be expressed as a function of the depletion depth as:

$$\alpha = \frac{\varepsilon_{SiC}}{X_D} \tag{A9a}$$

$$\beta = \frac{\varepsilon_{SiC}}{X_D}(\pi (X_D - h) + 2l) \tag{A9b}$$

$$\gamma = \frac{\varepsilon_{SiC}}{X_D}\left(\pi (X_D - h) l + l^2\right) \tag{A9c}$$

### B. $X_n \leq h$

When X≤h, d becomes zero because the depletion region on the n-side of the junction does not reach beyond the lower surface of the mesa etching. In this scenario, the only contribution to depletion charge comes from $V_{TC}$ in (A3) that transform into $V^*_{TC}$:

$$V^*_{TC} = \frac{\pi X_n (r^2 + R^2 + rR)}{3} \tag{A10}$$

whereas the associated capacitance is

$$\frac{C\,(V)}{\pi r^2} = \left| qN_D \left[ X'_n + \frac{X'_n l}{r} + \frac{X'_n l^2}{3r^2} \right] \right| = \alpha^* + \frac{\beta^*}{r} + \frac{\gamma^*}{r^2} \tag{A11}$$

and

$$\alpha^* = qN_D \left| X'_n \right| = \frac{\varepsilon_{SiC}}{X_D} = C_A(V) \tag{A11a}$$

$$\beta^* = qN_D \left| X'_n \right| l = \frac{\varepsilon_{SiC}}{X_D} l \tag{A11b}$$

$$\gamma^* = qN_D \left| X'_n \right| l^2 = \frac{1}{3} \frac{\varepsilon_{SiC}}{X_D} l^2 \tag{A11c}$$

From (A11a), (A11b), (A11c), it is evident that when l = 0, the typical expression for a parallel plate capacitor is restored.

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## REFERENCES

[1] D. K. Schroder, *Semiconductor Material and Device Characterization*. Hoboken, NJ, USA: Wiley, 2006, doi: 10.1063/1.2810086.

[2] G. Sozzi, M. Lazzarini, R. Menozzi, R. Carron, E. Avancini, B. Bissig, S. Buecheler, and A. N. Tiwari, "A numerical study of the use of C-V characteristics to extract the doping density of CIGS absorbers," in *Proc. IEEE 43rd Photovoltaic Specialists Conf. (PVSC)*, Jun. 2016, pp. 2283–2288, doi: 10.1109/PVSC.2016.7750043.

[3] C.-L. Zhong, R.-H. Yao, and K.-W. Geng, "An improvement of the capacitance-voltage method to determine the band offsets in a-Si:H/c-Si heterojunctions," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 394–399, Feb. 2014, doi: 10.1109/TED.2013.2295459.

[4] S.-S. Huang, R. Lopez, S. Paul, A. T. Neal, S. Mou, M.-P. Houng, and J. V. Li, "$\beta$-$Ga_2O_3$ defect study by steady-state capacitance spectroscopy," *Jpn. J. Appl. Phys.*, vol. 57, no. 9, Sep. 2018, Art. no. 091101, doi: 10.7567/jjap.57.091101.

[5] F. C. Beyer, C. G. Hemmingsson, H. Pedersen, A. Henry, J. Isoya, N. Morishita, T. Ohshima, and E. Janzén, "Capacitance transient study of a bistable deep level in $e^-$-irradiated n-type 4H-SiC," *J. Phys. D, Appl. Phys.*, vol. 45, no. 45, Nov. 2012, Art. no. 455301, doi: 10.1088/0022-3727/45/45/455301.

[6] P. Blood and J. W. Orton, *The Electrical Characterization of Semiconductors: Majority Carriers and Electron States*. New York, NY, USA: Academic, 1992.

[7] P. Hazdra, P. Smrkovský, J. Vobecký, and A. Mihaila, "Radiation resistance of high-voltage silicon and 4H-SiC power p-i-n diodes," *IEEE Trans. Electron Devices*, vol. 68, no. 1, pp. 202–207, Jan. 2021, doi: 10.1109/TED.2020.3038713.

[8] K. Tian, J. Xia, K. Elgammal, A. Schöner, W. Kaplan, R. Karhu, J. Ul-Hassan, and A. Hallén, "Modelling the static on-state current voltage characteristics for a 10 kV 4H-SiC PiN diode," *Mater. Sci. Semicond. Process.*, vol. 115, Aug. 2020, Art. no. 105097, doi: 10.1016/j.mssp.2020.105097.

[9] S. M. Sze, *Physics of Semiconductor Devices*, 3rd ed. Hoboken, NJ, USA: Wiley, 2007. [Online]. Available: https://onlinelibrary.wiley.com/doi/book/10.1002/0470068329

[10] R. S. Müller and T. I. Kamins, *Device Electronics for Integrated Circuit*, 3rd ed. Hoboken, NJ, USA: Wiley, 2002.

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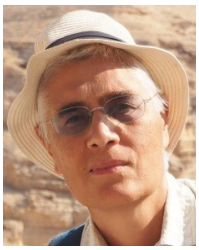

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