Silicene Applications in Nanotechnology: From Transistors to Bendable Membranes

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(Review Paper)

***Abstract*—Two-dimensional (2D) materials are today potential candidates for next generation ultra-scaled devices. After the boost provided by graphene, the 2D materials family is still quickly expanding and it is now clear that their properties may suit specific target applications but not all of them as originally expected by device engineers. Among them, a silicon-based 2D material, i.e., silicene, might represent the last frontier of the long shrinking journey of silicon throughout the semiconductor roadmap. Here, we review two applications based on the integration of silicene in field-effect transistors and bendable membranes, demonstrating that, with carefully engineered processes, silicene can be used in specific nanotechnology applications. We then briefly introduce other Xenes, the 2D materials family composed of single-element graphene-like lattices whose silicene is the frontrunner, and finally we provide an outlook on the future improvements to overcome the current roadblocks (large-scale growth and device standardization) towards a lab-to-fab transition towards Xenes integration into the silicon-based complementary metal-oxide-semiconductor technology.**

***Index Terms*—2D materials, electronics, field-effect transistor, flexible, membrane, piezoresistor, silicene, Xenes.**

I. Introduction

THE advancements in the electronics field are undoubtedly related to one single material: silicon. After many years our everyday life devices are still based on silicon technology, thus demonstrating that a silicon successor today has not showed up yet. A silicon successor has been long sought because since the beginning of the electronics era it was clear that within the Moore scaling law, silicon would not have lasted forever if more and more devices must fit to the same chip. The urgent need to keep on downscaling the devices dimensions fuelled the race to find viable solutions to replace silicon involving III-V semiconductors and carbon nanotubes before, and two-dimensional (2D) materials now [1]. However, silicon is so ubiquitously invasive in the electronic device architectures that before replacing it with other candidates, some technological roadmaps still foster the chance of a smart integration of 2D materials with the already existing silicon technology [2], [3]. In the 2D materials framework, after the outstanding properties of graphene [4], a new life for silicon in the shape of its 2D allotrope mimicking or expanding the graphene properties began in 2012 and this new material was termed silicene [5]. On the one hand, silicene is a fascinating option to bridge the 2D materials' world with silicon technology, but, on the other hand, silicene is also important as it paved the way for a new family of 2D materials coined Xenes after it, namely the graphene-like lattices made of X atoms other than carbon, where the X elements belonged to group 14 in a first place but progressively extended to nearby groups of the periodic table [6]. Hence, the silicene discovery encouraged many researchers in the effort to widen the class of 2D elemental materials beyond graphene, and today the *Xenes periodic table* ranges from borophene to tellurene grown by different physical and chemical methods [7], [8], [9], [10]. Combining experiments and theoretical calculations makes possible to demonstrate that the Xenes show different properties and then the current challenge is to find the best applications they look promising for [6]. Silicene, as other Xenes, was theoretically predicted well-before its experimental discovery. The freestanding silicene lattice is stable with a low buckling (0.44 Å), i.e., top and bottom silicon atoms are not on the same plane, that anyway does not affect the presence of Dirac fermions close to K point where energy and momentum have a linear dispersion relation (Fermi velocity $\sim 10^6$ m/s), even if the spin-orbit coupling opens a small bandgap (up to 1.55 meV) making silicene a quantum spin Hall insulator [11], i.e., a topological material. The main features of the freestanding silicene lattice are summarized in Table I [11], [12], [13], [14].

TABLE I
Structural and Electronic Parameters of Freestanding Silicene From Ab Initio Calculations

Parameter	Value	Ref.
Lattice constant	3.868 Å	[13]
Bond length	2.23 /2.28 Å	[11, 12]
Buckling	0.44 Å	[12,13]
Fermi velocity	0.53×10^6 m/s	[12]
Bandgap	0.65 / 1.55 meV	[11, 12]
Effective carrier mass	0.0005 m_e	[12]
Mobility	1200 cm^2/Vs	[14]
Saturation velocity	3.9×10^6 cm/s	[14]

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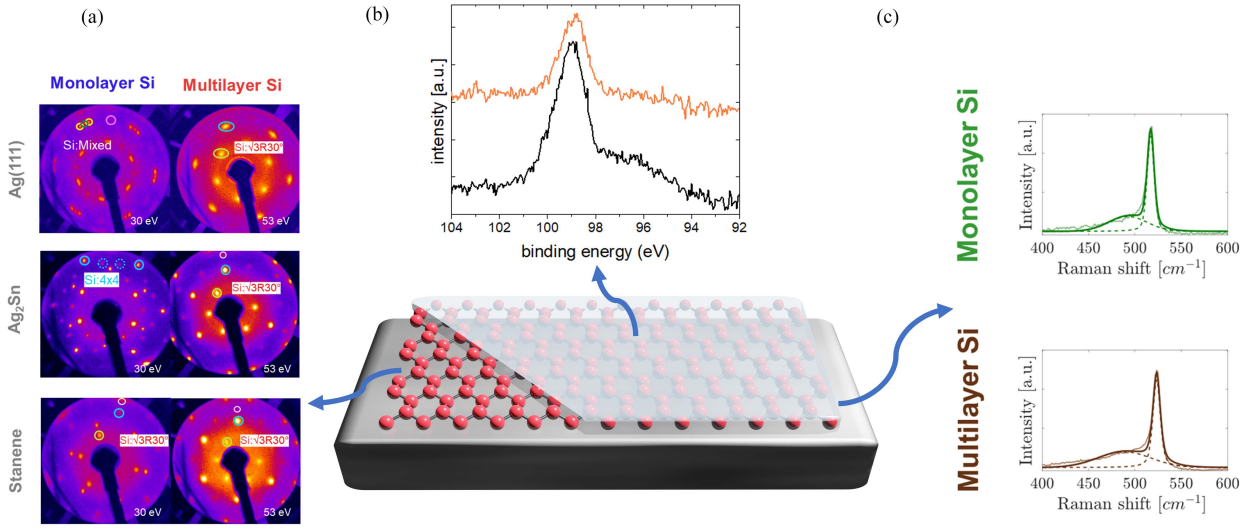

Fig. 1. Sketch of silicene sandwiched in between silver substrate and the Al_2O_3 protective layer. (a) LEED patterns of the different configurations used for template engineering the single-layer (left column) and multilayer (right column) silicene growth: Ag(111) (top), Ag_2Sn-Ag(111) (middle), and stanene on Ag(111) (bottom). (b) X-ray photoelectron spectroscopy of the Si 2*p* core level (at binding energy of ∼99 eV) of the freshly as-grown silicene (black) and after deposition of the Al_2O_3 protective layer and exposure to air (orange). (c) Raman spectra of the encapsulated single-layer (top) and multilayer (bottom) silicene showing characteristic Raman modes, close to 520 cm^{-1}. Adapted from Refs [21], [22], [25].

Stimulated by this theoretical background, many attempts to synthesize silicene culminated with the compelling evidence of this novel allotropic phase of silicon followed by the other Xenes [7]. Here, we review some practical applications in this respect which mostly involve silicene and prove how silicene, but quite straightforwardly all the Xenes, can be considered as nanotechnology player provided that some precautions on its handling are taken into account. In particular, for silicene, two applications like transistors and bendable membranes suggest that silicene itself might be a leading character in electronics still keeping silicon on the stage after all. Other applications based on Xenes out of silicene will be briefly outlined and finally a perspective on the tasks needed to favor the lab-to-fab transition will be proposed.

II. Silicene Out of Vacuum

In the molecular beam epitaxy (MBE) framework, the key for arranging silicon atoms in a graphene-like lattice consists of using commensurate substrates, e.g., the (111) surface of silver, and specific growing conditions, e.g., the substrate temperature. Practically speaking, out of an ultra-high vacuum environment silicene does not survive because its metastable nature makes it interacting with the supporting substrate as well as the surrounding environment, thus demanding for a protective layer [15]. Concomitantly, the use of bulk and metallic crystals for the silicene growth makes its exploitation in devices difficult and expensive. Here, two paths enabling the silicene handling in ambient conditions are briefly summarized in Fig. 1 and they constitute the starting configuration for the silicene-based devices discussed below.

The bottom side of silicene is typically supported by a hosting metallic substrate that is necessary to stabilize the silicene lattice. Although non-metallic substrates can be used as well (e.g., sapphire [16]), template engineering the silver substrate paves the way for the silicene decoupling from the pristine substrate [15]. First, a thin (300 nm-thick) silver film can be epitaxially grown on mica on which silicene shows the same surface reconstructions of the bulk silver crystal as demonstrated by low-energy electron diffraction (LEED) patterns in Fig. 1(a) top row, where, for the single-layer case, the typical coexistence of different silicene phases (mostly 4×4 and $\sqrt{13}\times\sqrt{13}$ superstructures) is observed. Second, the Ag(111) surface termination can be further modified by carefully tuning the deposition of an additional element, e.g., tin, aiming at engineering a functional buffer layer, i.e., an extra layer added in between to modify the silicene properties while favoring its decoupling from the silver substrate. Recently the buffer layer concept strongly benefitted of the renewed interest in the heterostructures as well as the remote epitaxy concept [17], [18]. Indeed, the sequential stacking of the same or different 2D materials, including Xenes, gives rise to new phenomena but can be also intended as a way to protect a 2D material with another one [19]. For the specific case of the silicene-stanene heterostructures [20], in an MBE framework, a further fine control of the deposition even in a sub-monolayer tin regime turns out into a silver surface modification depending on the amount of tin deposited (Fig. 1(a)) [21]. In this latter case, the role of tin is twofold: the Ag_2Sn alloy (1/3 monolayer tin deposition) and stanene (1 monolayer deposition on top of the Ag_2Sn alloy) templates allow filtering the subsequently grown silicene phases (Fig. 1(a)) on top and also decoupling silicene from silver (as detailed below in the all-around encapsulation scheme) [22], as the silicon-silver interaction has been proved to be not negligible from optical spectroscopy experiments [23].

The top side of silicene demands for a protective encapsulation as silicene undergoes oxidation in environmental conditions. Indeed, the mixed sp^2/sp^3 hybridization, resulting from the substrate-induced stabilization, makes silicene prone to chemical reactivity [24]. To prevent oxidation, silicene is encapsulated with a protective layer like Al_2O_3 [25], or graphene [26], or hBN [27], [28], or CaF_2 [29]. The use of graphene or hBN flakes has the main drawback to protect limited area of the

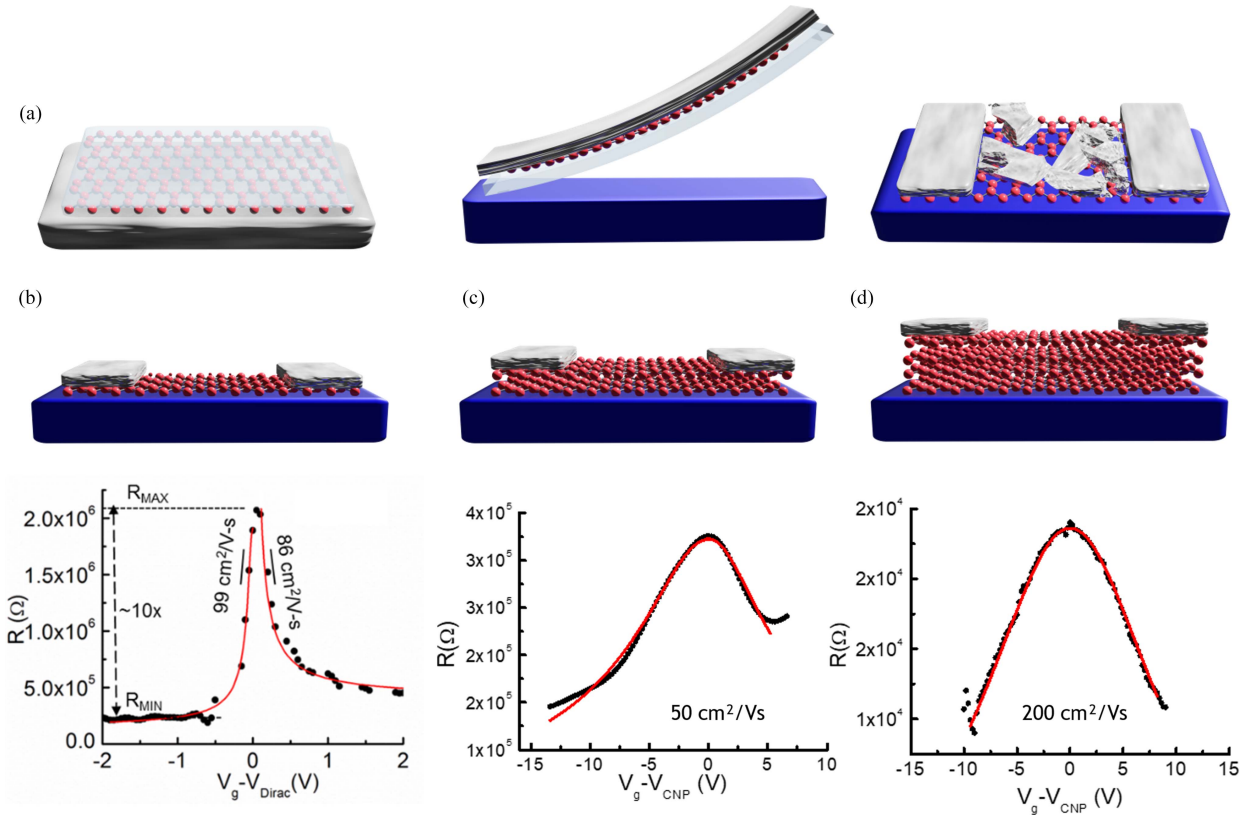

Fig. 2. Silicene-based FETs fabricated using the native silver substrate to design by lithography source and drain electrodes when the encapsulated silicene is transferred from the Al_2O_3 side onto a SiO_2/Si substrate serving as bottom gate electrodes. (a) The SEDNE process starts with the 'silicene sandwich' where silicene is embedded in between the Al_2O_3 capping layer on top and the thin silver substrate at the bottom (left), then it is placed upside down on a SiO_2/Si^{++} substrate serving as a bottom gate electrode (middle) and finally silver is etched away (using KI and I_2 solution) to create the channel and the source and drain electrodes (right). (b) Single-layer silicene FET resistance plot vs. voltage overdrive. The red curve is the ambipolar diffusive model fit used for extracting mobility values for electrons and holes [34]. (c) 10 monolayers and (d) 24 monolayers silicene FETs fabricated with the encapsulation-free SEDNE and fit with the ambipolar diffusive model (red curve). Adapted from Refs. [32], [36].

underlying silicene [26], [28], whereas the intercalation under hBN [27] or the epitaxial growth of Al_2O_3 or CaF_2 are fully compatible with the need to cover wafer-scaled area of silicene as well as other Xenes (e.g., germanene [25], [29], [30]). Among these available options, the choice of Al_2O_3, combined with the use of thin metal films on mica, is particularly suitable for processes, enabling the realization of devices discussed in the following sections. Indeed, 5 nm-thick Al_2O_3 film grown by molecular beam deposition turns out to be effective in protecting silicene as confirmed by X-ray photoelectron spectroscopy (Fig. 1(b)) [25] and Raman spectroscopy (Fig. 1(c)) [22], [24]. Fig. 1(b) shows the Si 2*p* core level of silicene before (black) and after (orange) air exposure, demonstrating the chemical status of silicene is unchanged. As Raman spectroscopy is a quick and reliable tool for studying 2D materials [31], the evidence of a clear Raman mode for single and multilayer silicene, reported in Fig. 1(c) and characterized by an intense mode at ∼520 cm^{-1} and a lower frequencies modes forming the shoulder from 450 to 500 cm^{-1} (mostly related to the non-planar hexagons of the silicene lattice [24]), can be taken as a fingerprint for monitoring the silicene status outside of vacuum environment [24] and in particular for all the processes necessary for the silicene integration in a device layout [22].

III. Silicene Field-Effect Transistors

The first example of application is the fabrication of silicene-based transistors. The exploitation of silicene for this kind of device is made possible by starting with the encapsulated configuration described before (Fig. 1), where silicene is sandwiched in between the Al_2O_3 capping layer on top and supporting silver on mica at the bottom. Yet again the silicene instability in air demands also for dedicated device processing and this task is achieved by implementing the silicene encapsulated delamination with native electrodes (SEDNE) process, where the encapsulation elements turn out be re-used for the device fabrication process [32]. The SEDNE process, illustrated in Fig. 2(a), flips upside down the silicene sandwich in Fig. 1 and makes use of the Al_2O_3 capping layer as the oxide gate (by placing the sample on SiO_2/Si^{++} substrate, where the heavily doped silicon serves as bottom gate electrode) and of the native silver thin film as source and drain electrodes by lithographic patterning (after removing the mica by mechanical exfoliation). The final outcome of the SEDNE process, therefore, is a bottom gate field-effect transistor (FET) based on a silicene channel (Fig. 2).

The electrical measurements on the silicene FETs give charge carriers transport similar to graphene [33]. The typical bell-shaped resistance plot (Fig. 2(b)) can be fitted by the

well-accepted ambipolar diffusive model typically used for graphene FETs [34], which gives mobility of about 100 cm^2/Vs. This ambipolar transport can be explained by the predicted bandstructure of silicene, where a Dirac cone is expected after the removal of the silver substrate [35]. The measured mobility is one order of magnitude lower than theoretical predictions for freestanding silicene (see Table I) and is likely to be limited by acoustic phonon scattering, electron-phonon coupling, and scattering at grain boundaries of the silicene domains. The channel opening operation leaves silicene exposed to ambient conditions, after the silver removal (Fig. 2(a) right), and is responsible for the short lifetime of the silicene FETs that, after about two minutes, stops operating due to environmental degradation of the uncovered silicene in the channel [25], [32]. As only an all-around encapsulation of silicene, i.e., a top and bottom faces protecting scheme (see below), could be effective in protecting both sides during the process, an intriguing option for longer stability is provided by multilayer silicene. Multilayer silicene (schematically depicted as an integer number of silicene layers in Fig. 2(c) and (d), for 10 and 24 monolayers respectively) is not a layered van der Waals crystal, at variance with graphite, because it is characterized by a layer-plus-island (Stranski-Krastanov) growth mode with a unique surface reconstruction for all the layers beyond the first one [36]. Typically, multilayer silicene thickness is expressed in terms of number of monolayers depending on the growing time in the MBE deposition. Intriguingly, multilayer silicene hosts Dirac fermions like the single-layer but, due to its bulky nature (obviously depending on the number of layers), is proven to last in ambient conditions without protecting layer for longer time in comparison with the single-layer [37]. Hence, multilayer silicene FETs can be fabricated with a modified SEDNE process. In details, the modified process does not include the use of an additional capping layer (i.e., the Al_2O_3 top layer), but it take advantages of the multilayer character of the sample where the top and bottom layers protect the inner ones from oxidation [36]. Fig. 2(b) and (c) show the thickness-dependent resistance plots for two multilayer silicene FETs with channels made of 10 and 24 monolayers, respectively. The ambipolar diffusive model used for the single-layer case enables to extract charge carriers' mobility values up to 200 cm^2/Vs (for the 24 monolayers silicene FET in Fig. 2(d)), two times higher than the single-layer FET device. Interestingly, a lower mobility is measured for the intermediate case of 10 monolayers (Fig. 2(c)), the minimum thickness which provided an operating device, and this can be related to the peculiar morphology of multilayer silicene, where the layer-plus-island growth mode makes possible the formation of disconnected channels thus limiting the overall transport [36]. However, the three-dimensional structure of multilayer silicene improves the stability of the related FETs up to two days before degrading like the single-layer silicene-based FET. Interestingly, mobility of the charge carriers increases with thickness of the channel keeping the ambipolar transport but, conversely, the on/off current ratio diminishes from 10 to 2. Silicene FETs can be improved by protecting the exposed channels and developing *ad hoc* transfer processes [38]. However, the 'silicene sandwich' configuration might turn out to be further optimized by changing the metal, provided that silicene growth is accomplished, in particular in case of a very low-contact resistance, and by improving the crystalline quality of protective layer with 2D oxide grown by low temperature MBE or atomic layer deposition. Indeed, such a configuration not only still includes both the electrodes and the gate oxide but also enables the device fabrication with few lithographic steps and a minimum damage for silicene.

IV. All-Around Encapsulation

Further optimization of silicene stability can be achieved in an all-around encapsulation silicene framework where both the silicene sides are likewise protected [22]. At variance with the Al_2O_3 capping layer that requires no stringent epitaxial conditions for being grown on the top face of silicene, the bottom side is more critical because silicene needs a commensurate substrate to grow on top of, thus stressing out the importance of template engineering (see Fig. 1(a) where silver has been properly modified by tin for such a purpose). In this context, 2D materials-based heterostructures assembled by combining either manually or by sequential growth two or more 2D materials on top of each other is a possible solution. The idea here is to extend the 'silicene sandwich' concept adding external layers whose role is in first place to keep silicene safe. In particular, on the Ag(111) thus far the following Xenes have been reported: borophene, silicene, germanene, stanene, blue-phosphorene, antimonene, and bismuthene [39]. Hence, silver looks like a versatile template for hosting concomitantly two different Xenes, like silicene and stanene [5], [40]. On Ag(111), for the silicene and stanene case, it turns out that the silicon and tin growth order is exchangeable providing in both cases two heterostructures made of crystalline components [20]. However, theoretical calculations demonstrate that only the stanene on silicene sequence preserve two buckled honeycomb lattices in a pure Xene heterostructure while, conversely, the reversed order, i.e., silicene on stanene, breaks the stanene symmetry into a distorted lattice without any chemical intermixing between silicon and tin and then this configuration can be considered as a pseudo Xene heterostructure (Fig. 1(a)) [20]. By the way, the pseudo Xene heterostructure configuration makes possible to insert an additional layer (no matter of its crystal shape for the purpose illustrated below) in between silicene and silver with a twofold consequence [20]. First, silicene turns out to be decoupled from the pristine substrate therein bypassing the hybridization issue in the directly grown silicene on silver [23], [41] and thus making it interesting for the characterization of its opto-thermal [42] and mechanical [43] properties. Second, after silver removal (in Fig. 2(a) right) the silicene bottom face is now protected by a sacrificial layer preventing degradation, thus targeting the all-around encapsulation silicene configuration long sought. Indeed, inserting the stanene layer in between silicene and silver, when silver is etched away and Raman spectroscopy is performed from the bottom side (Fig. 3(a)), both single and multilayer silicene show no significant changes in the shape profile or wavenumber positions of the modes in the measured Raman spectra in a timescale of months (Fig. 3(b)), so the stanene layer effectively serves as a sacrificial layer to protect silicene from degradation [22].

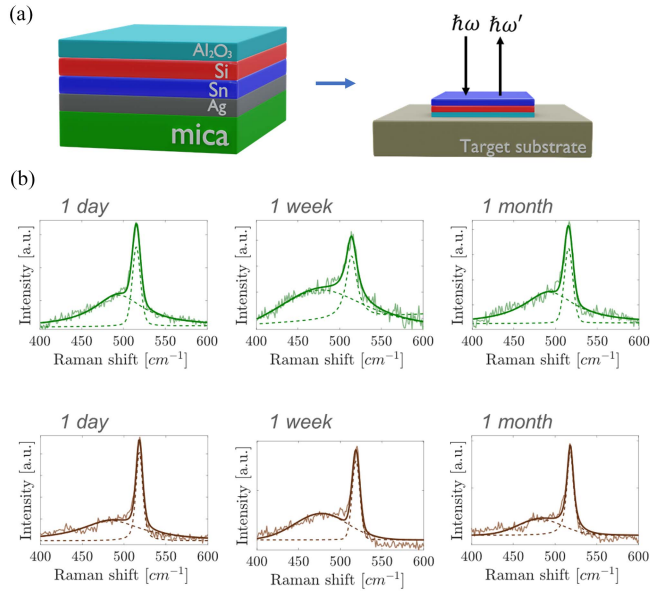

Fig. 3. (a) Building block scheme for silicene embedded in between Al_2O_3 capping layer and stanene on Ag(111)/mica substrate (left) and after transfer, mica peeling, and silver etching onto a target substrate for aging characterization (right). (b) Raman spectroscopy investigation of single (top row) and multilayer (bottom row) silicene from the bottom side after one day, one week, and one month air exposure (from left to right). Adapted from Ref. [22].

V. Silicene Membranes

When the electronic and mechanical interactions of silicene and the supporting silver substrate are weakened by the introduction of a buffer layer like stanene, the opto-thermal and mechanical properties of silicene can be eventually studied [42], [43]. In the former case, 2D materials are excellent thermal conductors and therefore they can be exploited to enhance the reliability and extend the lifetime of devices and integrated circuits (ICs) as heat is a typical failure issue for conventional ICs [44], [45]. In the latter case, the second application of silicene relies on the fabrication of bendable silicene membranes [43]. On the one hand, the bendable silicene membranes allow to study the mechanical properties of silicene when an external strain is applied and, on the other hand, their configuration is also prone for being integrated into device layouts for flexible electronics using the process developed for the silicene transistors, benefitting of the low thickness of the protective layers introduced by the all-around encapsulation scheme (Fig. 3). A conventional approach to study strain in 2D materials consists of bending, in a controlled manner, the material under investigation in a Raman spectroscopy setup for monitoring the evolution of the representative Raman modes when increasing the tensile and compressive strain [46]. Indeed, Raman spectroscopy is found to be very sensitive to strain, as demonstrated for graphene [47]. Lifting of degenerated modes, red and blueshifts as well as studying Grüneisen parameters can quantitatively determine the strain applied to the crystal. Indeed, the application of uniaxial strain removes the degeneracy of the representative in-plane Raman mode of graphene, thus resulting into sub-bands with distinctive shifts as a function of the strain amplitude. Quantitatively, the effect can be assessed by calculating the Grüneisen parameters of the individual Raman modes. In the silicene case, when increasing the applied uniaxial strain, the vibrational frequency of the silicene Raman mode is expected to redshift, i.e., move towards lower energy, because of the increase of the Si-Si bond length and the concomitant decrease of the atomic interaction. The evolution of the Raman spectra, with and without stanene, shows marked differences in the vibrational response of the silicene-based membranes under the application of a tensile strain (Fig. 4). For comparison purpose, single and multilayer silicene grown on Ag(111) and stanene-Ag(111) were studied aiming at understanding the role played by the stanene buffer layer. Without stanene, the Raman mode in single-layer silicene on silver shows a weak sensitivity, i.e., -0.9 cm^{-1}/%, to the applied strain up to 0.6% (Fig. 4(a) left column). A little higher strain sensitivity (-2.8 cm^{-1}/%) is observed in the case of multilayer silicene on silver (Fig. 4(a) right column). However, when stanene is introduced in between silicene and silver, even much higher strain sensitivity occurs for both single and multilayer silicene with larger shifts of the Raman mode position in the same strain range (Fig. 4(b), left column for single-layer silicene, right for multilayer silicene). Moreover, the response of the silicene-stanene heterostructures is more interesting because it is characterized by a bimodal regime, namely there are two different slopes with a threshold at 0.1% strain for single-layer and at 0.2% strain for multilayer silicene (see red arrows in Fig. 4(b) bottom row). It can be noticed that, for both single and multilayer silicene, the slopes values before (-5.5 and -7.7 cm^{-1}/%) and after (-1.7 and -4.3 cm^{-1}/%) the threshold are larger with respect to the same configurations without stanene in between (-0.9 and -2.8 cm^{-1}/%). Therefore, by comparison, the mechanical properties of silicene are strongly affected by the interaction with the substrate. In particular, for the silicene-stanene heterostructures, a strain field can be released more effectively to silicene in case of stanene buffering as proven by the steeper behaviour of the Raman shift with the applied bending and it can be related to a pure geometrical pairing with the stanene buffer layer [21].

In light of their strain-responsive behaviour, the bendable silicene membranes can be introduced into a technology-oriented process flow. In particular in flexible nanoelectronics, 2D materials take advantage from their ultimate thickness combined with outstanding mechanical properties over conventional thin films [45], [48]. The transfer processes developed for the specific silicene case (but equally extendable to all the Xenes, as there is no chemical sensitivity for this process, as demonstrated for blue-phosphorene [49]) enable two different approaches for micro and nanofabrication of a device pattern on silicene samples that can be defined before or after the transfer of the membrane incorporating an all-around encapsulated silicene, i.e., on the same stacking including, from top to bottom, Al_2O_3 capping layer, silicene, stanene, silver, and mica. In the former case, a device pattern, for example a microheater in Fig. 5 (picture on the left), can be defined on the Al_2O_3 face before the mica delamination and then transferred on a target substrate. In this way the advantage relies on the easier lithographic steps provided by the stiffness of the sample (because of the thick mica layer supporting the stack). The device can be integrated into any arbitrary rigid or flexible substrate, e.g., a polyethylene terephthalate (PET) polymer and a commercial paper sheet as reported in Fig. 5 (pictures on the right) [43]. In the latter approach, the membrane is transferred with the silver on top

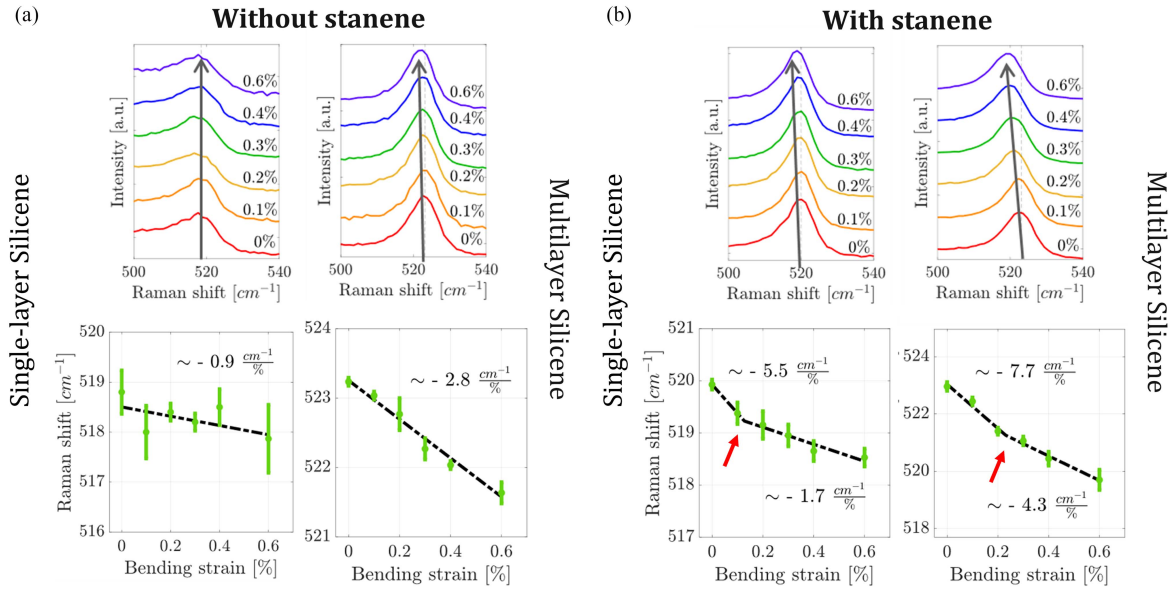

Fig. 4. Raman spectroscopy of the bendable membranes based on single and multilayer silicene without (a) and with (b) the stanene layer to form the heterostructure as a function of the applied strain. The top row shows the evolution of the Raman modes of single and multilayer silicene whereas the bottom row displays the Raman wavenumbers of the Raman modes from 0% to 0.6% uniaxial applied strain. Red arrows indicate the threshold for the bimodal regime in the silicene-stanene heterostructures strain-response. Adapted from Ref. [43].

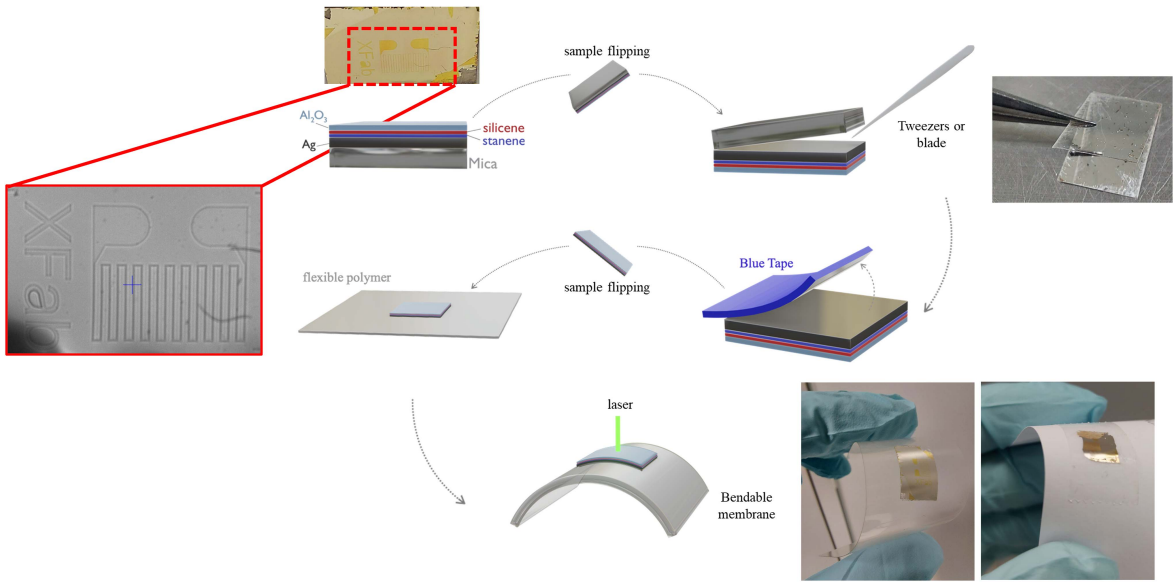

Fig. 5. Design of a device pattern before the transfer of the silicene-based membranes. The desired device, e.g., a microheater as in the picture on the left, is patterned on the top face, i.e., Al_2O_3, and then the sample is flipped upside down for the mica removal using tweezers and blue tape (Nitto tape 3M). The so-obtained membrane is flipped back and transferred onto a flexible substrate, e.g., a PET or a paper sheet as in the picture on the right, where a device on a flexible substrate is ready to use. Adapted from Ref. [43].

and the electrical contacts are designed by lithography on the native silver layer after the transfer and directly on the flexible substrate using the SEDNE process illustrated in Fig. 2(a) for the silicene-based FETs (Fig. 6(a)). This two-terminal passive device can be therefore tested as a piezoresistor, where the electrical resistance is measured as a function of the applied strain. An increment of the electrical resistance is observed in real-time by applying three different strain values (0.4%, 0.5%, and 0.6%) in a sequence of bending cycles (Fig. 6(b)), where the initial value of resistance at zero strain (R_0) is recovered after each bending cycle thus demonstrating a smooth operation of the proposed device [43]. Of course, in both the approaches, the choice of the device is not limited to a microheater or a piezoresistor, but all the devices compatible with the encapsulated scheme are possible, like FET, phototransistor, and so on (see Table II for the possible applications involving silicene).

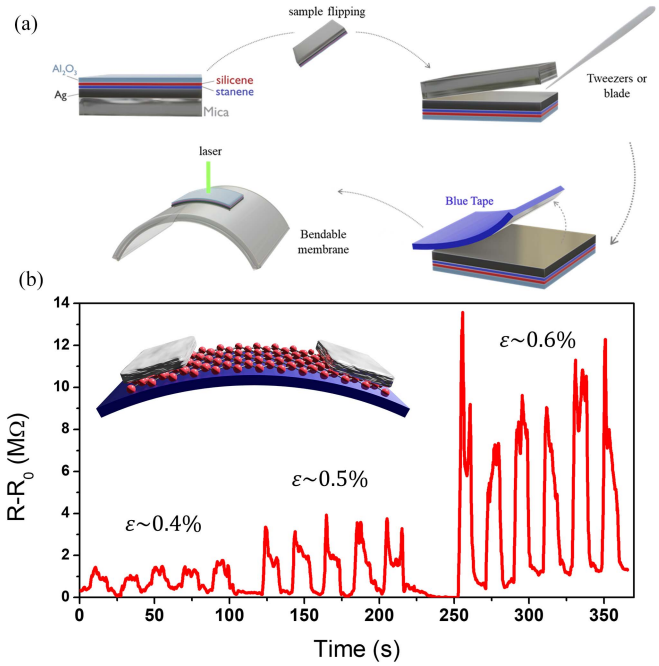

Fig. 6. Design of a device pattern after the transfer of the silicene-based membranes. (a) The process of Fig. 5 is slightly modified and after the mica removal using tweezers and blue tape (Nitto tape 3M), the electrical pads are designed by lithography with the SEDNE method directly on the flexible substrate for the realization of a device, e.g., a piezoresistor. (b) The so-fabricated piezoresistor is tested with bending cycles at different strain values (0.4%, 0.5%, and 0.6%) where the initial value of resistance at zero strain (R_0) is recovered after each bending cycle. Adapted from Ref. [43].

TABLE II
THEORETICALLY PREDICTED OR EXPERIMENTALLY DEMONSTRATED APPLICATIONS FOR SILICENE

Application	Status	Ref.
FET	Experiment	[32], [36], [50], [51]
Membrane	Experiment	[43]
Topological FET	Theory	[52]
Supercapacitor	Experiment	[53], [54]
Battery	Theory /Experiment	[55] [56]
Neuromorphic	Experiment	[57]
Thermoelectricity	Theory	[58]
Gas sensor	Theory	[59]
Gas storage	Theory	[60]
Biomedicine	Theory / Experiment	[61], [62]
Photodetector	Experiment	[63]
DNA sequencing	Theory	[64]

VI. SILICENE COUSINS

The applications involving silicene are only two examples in the burgeoning field of the Xenes where there is tremendous interest for other applications or interesting phenomena. The fabrication process and characterization methodology illustrated thus far for silicene can be potentially extended to all the Xenes provided that the substrate is made thin enough and the protective capping layer is used before taking them out of vacuum [38]. More stable than Xenes in ambient conditions are the Xanes, namely the hydrogenated counterpart of the Xenes, following the nomenclature introduced for graphene with graphane [65]. Silicane and germanane FETs were fabricated by liquid exfoliation method and mechanical cleaving of $Li_{13}Si_4$ and $CaGe_2$ powders, respectively, showing carriers mobility of 1.8 cm^2/Vs (hole) and 70 cm^2/Vs (electron and hole), respectively [50], [51]. Even though these are modest values, their cost-effective synthesis methods strongly suggest further optimization of their production, now limited to micro-scaled flakes. From chemical deintercalation of $CaSi_2$ powder, it is also possible to obtain silicon nanosheets for supercapacitor applications characterized by fast-charging, high areal capacity (up to 14 mF/cm^2), and excellent capacity retention after 10000 cycles [53], [54] as well as for neuromorphic computing applications in devices showing hysteretic characteristics and memristor-like behavior [57]. Out of standard integration of Xenes into a classical FET architecture, their topological properties are promising for establishing non-conventional devices where the more efficient and low power working mechanism should bring energetic and environmental benefits while keeping the performances beyond the state-of-the-art [66]. For instance, the discovery of superconductivity in few-layer stanene paves the way for the foundation of topological superconducting devices [67]. Moreover, the experimental observation of the 2D topological state, i.e., the quantum spin Hall insulator state, in germanene and bismuthene, where a sizeable body bandgap coexists with robust metallic edges, is of paramount importance for the topological FET, i.e., a FET where the on and off states are ruled by the topological states of the channel [68], [69]. In particular, for germanene, it has been demonstrated that the topological state can be switched by an electric field, thus being the proof-of-concept of the topological FET [69]. Among the Xenes, tellurene deserves particular attention as it is gaining increasing interest, mostly because it can be synthesized by physical and/or chemical vapour deposition or liquid exfoliation methods [70], [71], [72], that makes it the Xene looking more similar to the transition metal dichalcogenides (TMDs). Recently, the ease in the tellurene synthesis allowed for the fabrication of some prototypical devices, including FET [73], [74], [75], diode [76], photodetector [77], [78]. Moreover, quantum Hall effect of Weyl fermions in n-type tellurene has been reported by dielectric doping p-type tellurene [79]. Such a behavior was unexpected due to the semiconducting character of tellurene without crossing bands as in semimetals. On the other hand, p-type FETs obtained by evaporating tellurium on different substrates (like glass and plastic) represent an intriguing option in designing logic circuits thus complementing the multiple n-type options still available in the 2D materials portfolio [73]. The effective hole mobility measured is up to 35 cm^2/Vs with an on/off current ratio of 10^4 at room temperature showing no degradation in air without any protective layer for 30 days. The tellurium FETs were fabricated on flexible substrates (e.g., PET or Kapton) and interestingly the device mobility and on/off current ratio did not significantly change loading a tensile strain up to 0.63% (comparable to the stain applied to the silicene membranes in Fig. 4) and for a slightly lower value, i.e., 0.42%, they stay unaltered after 500 bending cycles. Beyond this threshold the device performance changes and becomes an open circuit when strain is 1.5% which is non-recoverable. Alternatively, solution-grown tellurene can be used to fabricate p-type FETs (with peak field-effect mobility up to 700 cm^2/Vs and on/off current ratio of 10^5) demanding anyway further work for large-scale assembly, for instance, via ink-jet printing [70]. However, as per TMDs, although using simpler and lower temperature growing methodologies

than other Xenes, even for tellurene, or generally speaking low-dimensional tellurium, it is urgent to standardize the growth on a large scale to favor the lab-to-fab transition [72]. Although silicene attracts major interest due to the natural compatibility with the semiconductor industry, other elements when reshaped as Xenes might be functional for some niche applications or targeted tasks, e.g., the need of p-type transistors. Moreover, the silicene-stanene heterostructures further prove that coupling Xenes might provide a different way to strengthen their properties and, in particular, their weaknesses, e.g., the air stability.

VII. What to Do Now

Silicene and the Xenes-based devices show enormous potential for future applications in different fields. Similar to the more mature 2D materials like graphene and TMDs, the Xenes need to step over the prototypical devices illustrated above and face the two following significant challenges. First, continuous effort in the growing methodologies for achieving the wafer-scale film quality, benchmarking to chip-grade single-crystalline silicon, is needed. The growing methodologies require understanding how the three thin-film growth modes, i.e., island (Vollmer-Weber), layer-plus-island (Stranski-Krastanov), and layer by layer (Frank-van der Merve), can be adapted at the Xenes scenario and in order to achieve uniform and continuous growth of the desired Xene at a wafer scale, with minimal grain boundary and other defects [80]. In this framework, the recent results of silicene growth are promising as the use of a properly functionalized or engineered substrate, e.g., the Ag_2Sn (Fig. 1(a)), turns out to be useful for 'silicene phase filtering' and then pointing to single crystal growth [21]. This aspect is therefore crucial as evidenced by the considerations on the mobility values of the silicene FETs, where the main deviations to the predicted values (Table I) can be plausibly related to morphological issues of the deposited silicene layers, like grain boundaries for the single-layer or incomplete layer formation for the multilayer silicene case. Although some substrates are non-conventional for applications, the use of thin films on more conventional substrates, e.g., silicon, complemented with dedicated transfer protocols is a viable route for this purpose. For silicene, the deposition of the thinnest possible layer of silver on top of a silicon substrate would represent a remarkable achievement within the SEDNE process [81]. Second, benefitting from the previous experience on graphene and TMDs, standardized protocols for full (mostly electrical, but not limited to) characterization of the Xenes-based devices aiming at the development of ICs in a silicon technology framework are definitely urgent [82]. Hitherto, less attention has been dedicated to these aspects for the Xenes mainly because they are studied by fewer research groups around the world. Recently, a protocol based on four milestones such as yield, variability, reliability, and stability of 2D materials based solid-state electronic devices, has been proposed and its application to silicene and the Xenes should be recommended [83]. In the next five years, it is expected that pilot demonstration of simple Xenes-based or hybrid (complemented by other 2D materials) ICs will rely on using one or a few modules, like FETs, memristors, diodes, and then their combination is also expected to provide a higher circuit-level performance and functionalities although in a low integration density framework. For these reasons, future studies on Xenes-based devices should include deeper statistical analysis focusing on the most relevant figures of merit and parameters. As these recommendations hold for all the 2D materials, what really makes Xenes more intriguing with respect to the other 2D materials should be their versatility. Indeed, Xenes are an open playground from the materials science point of view as their freestanding lattices are typically distorted when accommodated on a substrate which in turn modifies their properties. For instance, the silicene reconstructions observed on the Ag(111) surface are different from those on Al(111) or Ir(111), even if they originated from the same freestanding lattice [5], [84], [85]. Hence, it is possible to leverage on the Xenes properties to artificially create the best candidate for the specific target applications. A synergistic cooperation between theory and experiments is here necessary to drive research towards the most promising configuration regarding Xenes on substrates, as recently occurred even for the forerunner graphene whose lack of bandgap has been eventually surmounted [86]. Although such a Xenes engineering is the desired outcome, it should be pointed out that even integrating Xenes in the silicon-based ICs could be a viable option to perform secondary tasks (e.g., heat dissipation) or boosting performance of the overall systems [82].

VIII. Conclusion

In summary, some possible applications for silicene and the Xenes have been reviewed. In particular for silicene, its affinity with the ubiquitous silicon in nanotechnology makes it the strongest candidate among the Xenes. In the first application, a silicene transfer methodology is proposed for transistor fabrication where single and multilayer silicene transistors show ambipolar behavior at room temperature with modest mobility of the charge carriers. Further optimization is needed, especially to improve the transistor's lifetime, and the all-around encapsulation of silicene based on the silicene-stanene heterostructures is a viable route in this direction. Concomitantly, functionalization strategies can be also adopted to boost the performance of the silicene channel. In the second application, bendable silicene membranes can be obtained starting from the silicene-stanene heterostructure configuration, where stanene enhances the mechanical transfer of the applied strain as demonstrated by the largest shift of the Raman wavevectors observed in the heterostructures when compared to silicene directly grown on silver substrate. With the process developed for the silicene transistors the fabrication of devices like a microheater or a piezoresistor on flexible substrates is possible. Of course, these applications can be merged together into a framework where silicene-based transistors are fabricated on flexible substrate thus looking promising for applications in flexible, wearable, and biomedical electronics. Finally, the proposed process flow is not limited to silicene but can be extended to the whole class of the epitaxial Xenes, in particular for those supported by the silver substrate, which is quite a universal template for Xenes growth. The wealth of properties of the Xenes thus further encourages research aiming at contributing to the fourth industrial revolution, keeping in mind that the choice of a specific Xene depends on the target application.

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REFERENCES

[1] Y. Liu, X. Duan, H.-J. Shin, S. Park, Y. Huang, and X. Duan, "Promises and prospects of two-dimensional transistors," *Nature*, vol. 591, no. 7848, pp. 43–53, Mar. 2021.

[2] D. Akinwande et al., "Graphene and two-dimensional materials for silicon technology," *Nature*, vol. 573, no. 7775, pp. 507–518, Sep. 2019.

[3] S. Wang, X. Liu, M. Xu, L. Liu, D. Yang, and P. Zhou, "Two-dimensional devices and integration towards the silicon lines," *Nature Mater.*, vol. 21, no. 11, pp. 1225–1239, Oct. 2022.

[4] K. S. Novoselov et al., "Electric field effect in atomically thin carbon films," *Science*, vol. 306, no. 5696, pp. 666–669, Oct. 2004.

[5] P. Vogt et al., "Silicene: Compelling experimental evidence for graphene-like two-dimensional silicon," *Phys. Rev. Lett.*, vol. 108, no. 15, Apr. 2012, Art. no. 155501.

[6] A. Molle and C. Grazianetti, in *Xenes - 2D Synthetic Materials Beyond Graphene*. Sawston, U.K.: Woodhead Publishing, 2022.

[7] C. Grazianetti and C. Martella, "The rise of the xenes: From the synthesis to the integration processes for electronics and photonics," *Materials*, vol. 14, no. 15, Jul. 2021, Art. no. 4170.

[8] N. R. Glavin et al., "Emerging applications of elemental 2D materials," *Adv. Mater.*, vol. 32, no. 7, Feb. 2020, Art. no. 1904302.

[9] A. J. Mannix, B. Kiraly, M. C. Hersam, and N. P. Guisinger, "Synthesis and chemistry of elemental 2D materials," *Nature Rev. Chem.*, vol. 1, no. 2, pp. 1–14, Jan. 2017.

[10] M. E. Dávila and G. Le Lay, "Silicene: Genesis, remarkable discoveries, and legacy," *Mater. Today Adv.*, vol. 16, Dec. 2022, Art. no. 100312.

[11] C.-C. Liu, W. Feng, and Y. Yao, "Quantum spin hall effect in silicene and two-dimensional germanium," *Phys. Rev. Lett.*, vol. 107, no. 7, Aug. 2011, Art. no. 076802.

[12] L. Matthes, O. Pulci, and F. Bechstedt, "Massive dirac quasiparticles in the optical absorbance of graphene, silicene, germanene, and tinene," *J. Phys.: Condens. Matter*, vol. 25, no. 39, Oct. 2013, Art. no. 395305.

[13] M. Houssa et al., "Theoretical aspects of graphene-like group IV semiconductors," *Appl. Surf. Sci.*, vol. 291, pp. 98–103, Feb. 2014.

[14] X. Li, J. T. Mullen, Z. Jin, K. M. Borysenko, M. Buongiorno Nardelli, and K. W. Kim, "Intrinsic electrical transport properties of monolayer silicene and MoS 2 from first principles," *Phys. Rev. B*, vol. 87, no. 11, Mar. 2013, Art. no. 115418.

[15] C. Grazianetti and A. Molle, "Engineering epitaxial silicene on functional substrates for nanotechnology," *Research*, vol. 2019, pp. 1–8, Sep. 2019.

[16] C. Grazianetti et al., "Optical conductivity of two-dimensional silicon: Evidence of dirac electrodynamics," *Nano Lett.*, vol. 18, no. 11, pp. 7124–7132, Nov. 2018.

[17] Z. I. Alferov, "Nobel lecture: The double heterostructure concept and its applications in physics, electronics, and technology," *Rev. Mod. Phys.*, vol. 73, no. 3, pp. 767–782, Oct. 2001.

[18] Y. Kim et al., "Remote epitaxy through graphene enables two-dimensional material-based layer transfer," *Nature*, vol. 544, no. 7650, pp. 340–343, Apr. 2017.

[19] E. Y. Andrei et al., "The marvels of moiré materials," *Nature Rev. Mater.*, vol. 6, no. 3, pp. 201–206, Mar. 2021.

[20] D. S. Dhungana, C. Grazianetti, C. Martella, S. Achilli, G. Fratesi, and A. Molle, "Two-dimensional silicene–stanene heterostructures by epitaxy," *Adv. Funct. Mater.*, vol. 31, May 2021, Art. no. 2102797.

[21] S. Achilli et al., "Crystal phase engineering of silicene by Sn-modified Ag(111)," *Nanoscale*, vol. 15, no. 26, pp. 11005–11012, Jul. 2023.

[22] D. S. Dhungana, C. Massetti, C. Martella, C. Grazianetti, and A. Molle, "All-around encapsulation of silicene," *Nanoscale Horiz.*, vol. 8, no. 10, pp. 1428–1434, Sep. 2023.

[23] E. Cinquanta et al., "Optical response and ultrafast carrier dynamics of the silicene-silver interface," *Phys. Rev. B*, vol. 92, no. 16, Oct. 2015, Art. no. 165427.

[24] E. Cinquanta et al., "Getting through the nature of silicene: An sp2-sp3 two-dimensional silicon nanosheet," *J. Phys. Chem. C*, vol. 117, no. 32, pp. 16719–16724, Aug. 2013.

[25] A. Molle et al., "Stability and universal encapsulation of epitaxial xenes," *Faraday Discuss.*, vol. 227, pp. 171–183, 2021.

[26] V. Ritter, J. Genser, D. Nazzari, O. Bethge, E. Bertagnolli, and A. Lugstein, "Silicene passivation by few-layer graphene," *ACS Appl. Mater. Interfaces*, vol. 11, no. 13, pp. 12745–12751, Apr. 2019.

[27] F. B. Wiggers et al., "Van der Waals integration of silicene and hexagonal boron nitride," *2D Mater.*, vol. 6, no. 3, Apr. 2019, Art. no. 035001.

[28] J. Genser et al., "Optical signatures of dirac electrodynamics for hBN-passivated silicene on Au(111)," *Nano Lett*, vol. 21, no. 12, pp. 5301–5307, Jun. 2021.

[29] D. Nazzari et al., "Epitaxial growth of crystalline CaF2on silicene," *ACS Appl. Mater. Interfaces*, vol. 14, no. 28, pp. 32675–32682, Jul. 2022.

[30] S. Suzuki et al., "Direct growth of germanene at interfaces between van der waals materials and Ag(111)," *Adv. Funct. Mater.*, vol. 31, no. 5, Jan. 2021, Art. no. 2007038.

[31] A. C. Ferrari and D. M. Basko, "Raman spectroscopy as a versatile tool for studying the properties of graphene," *Nature Nanotechnol.*, vol. 8, no. 4, pp. 235–246, Apr. 2013.

[32] L. Tao et al., "Silicene field-effect transistors operating at room temperature," *Nature Nanotechnol.*, vol. 10, no. 3, pp. 227–231, Feb. 2015.

[33] F. Schwierz, "Graphene transistors," *Nature Nanotechnol.*, vol. 5, no. 7, pp. 487–496, May 2010.

[34] S. Kim et al., "Realization of a high mobility dual-gated graphene field-effect transistor with Al2O3 dielectric," *Appl. Phys. Lett.*, vol. 94, no. 6, 2009, Art. no. 062107.

[35] E. Scalise et al., "Vibrational properties of epitaxial silicene layers on (1 1 1) Ag," *Appl. Surf. Sci.*, vol. 291, pp. 113–117, 2014.

[36] C. Grazianetti et al., "Silicon nanosheets: Crossover between multilayer silicene and diamond-like growth regime," *ACS Nano*, vol. 11, no. 3, pp. 3376–3382, Mar. 2017.

[37] P. De Padova et al., "24 h stability of thick multilayer silicene in air," *2D Mater.*, vol. 1, no. 2, Aug. 2014, Art. no. 021003.

[38] C. Martella et al., "Disassembling silicene from native substrate and transferring onto an arbitrary target substrate," *Adv. Funct. Mater.*, vol. 30, no. 42, Oct. 2020, Art. no. 2004546.

[39] C. Grazianetti and A. Molle, "Xene heterostructures," in *Xenes 2D Synthetic Materials Beyond Graphene*. Sawston, U.K.: Woodhead Publishing, 2022, pp. 377–403.

[40] J. Yuhara et al., "Large area planar stanene epitaxially grown on Ag(1 1 1)," *2D Mater.*, vol. 5, no. 2, Jan. 2018, Art. no. 025002.

[41] P. Gori, O. Pulci, F. Ronci, S. Colonna, and F. Bechstedt, "Origin of dirac-cone-like features in silicon structures on Ag(111) and Ag(110)," *J. Appl. Phys.*, vol. 114, no. 11, Sep. 2013, Art. no. 113710.

[42] E. Bonaventura et al., "Optical and thermal responses of silicene in Xene heterostructures," *Nanoscale Horiz.*, vol. 7, no. 8, pp. 924–930, Jul. 2022.

[43] C. Martella, C. Massetti, D. S. Dhungana, E. Bonera, C. Grazianetti, and A. Molle, "Bendable silicene membranes," *Adv. Mater.*, vol. 35, 2023, Art. no. 2211419.

[44] E. Pop, "Energy dissipation and transport in nanoscale devices," *Nano Res.*, vol. 3, no. 3, pp. 147–169, Mar. 2010.

[45] D. Akinwande, N. Petrone, and J. Hone, "Two-dimensional flexible nanoelectronics," *Nature Commun.*, vol. 5, Dec. 2014, Art. no. 5678.

[46] O. Çakıroğlu, J. O. Island, Y. Xie, R. Frisenda, and A. Castellanos-Gomez, "An automated system for strain engineering and straintronics of 2D materials," *Adv. Mater. Technol.*, vol. 8, no. 1, Jan. 2023, Art. no. 2201091.

[47] T. M. G. Mohiuddin et al., "Uniaxial strain in graphene by Raman spectroscopy: G peak splitting, Grüneisen parameters, and sample orientation," *Phys. Rev. B - Condens. Matter Mater. Phys.*, vol. 79, no. 20, May 2009, Art. no. 205433.

[48] Y. Luo et al., "Technology roadmap for flexible sensors," *ACS Nano*, vol. 17, no. 6, pp. 5211–5295, Mar. 2023.

[49] C. Grazianetti, G. Faraone, C. Martella, E. Bonera, and A. Molle, "Embedding epitaxial (blue) phosphorene in between device-compatible functional layers," *Nanoscale*, vol. 11, no. 39, pp. 18232–18237, Oct. 2019.

[50] H. Nakano et al., "Solution-processed silicane field-effect transistor: Operation due to stacking defects on the channel," *Adv. Funct. Mater.*, vol. 30, no. 15, Apr. 2020, Art. no. 1908746.

[51] B. N. Madhushankar et al., "Electronic properties of germanane field-effect transistors," *2D Mater.*, vol. 4, no. 2, Jun. 2017, Art. no. 021009.

[52] M. Ezawa, "Quantized conductance and field-effect topological quantum transistor in silicene nanoribbons," *Appl. Phys. Lett.*, vol. 102, no. 17, Apr. 2013, Art. no. 172103.

[53] Q. Guo, C. Bai, C. Gao, N. Chen, and L. Qu, "Two dimensional silicene nanosheets: A new choice of electrode material for high-performance supercapacitor," *ACS Appl. Mater. Interfaces*, vol. 14, no. 34, pp. 39014–39021, Aug. 2022.

[54] Q. Guo, J. Liu, C. Bai, N. Chen, and L. Qu, "2D silicene nanosheets for high-performance zinc-ion hybrid capacitor application," *ACS Nano*, vol. 15, no. 10, pp. 16533–16541, Oct. 2021.

[55] Y. Liu et al., "Silicene oxide: A potential Battery500 cathode for sealed non-aqueous lithium–oxygen batteries," *Mater. Today Energy*, vol. 18, Dec. 2020, Art. no. 100503.

[56] J. Liu et al., "Few-layer silicene nanosheets with superior lithium-storage properties," *Adv. Mater.*, vol. 30, no. 26, Jun. 2018, Art. no. 1800838.
[57] C. Wang et al., "Neuromorphic device based on silicon nanosheets," *Nature Commun.*, vol. 13, no. 1, pp. 1–10, Sep. 2022.
[58] K. Yang, S. Cahangirov, A. Cantarero, A. Rubio, and R. D'Agosta, "Thermoelectric properties of atomically thin silicene and germanene nanostructures," *Phys. Rev. B - Condens. Matter Mater. Phys.*, vol. 89, no. 12, Mar. 2014, Art. no. 125403.
[59] W. Hu, N. Xia, X. Wu, Z. Li, and J. Yang, "Silicene as a highly sensitive molecule sensor for NH3, NO and NO2," *Phys. Chem. Chem. Phys.*, vol. 16, no. 15, pp. 6957–6962, Mar. 2014.
[60] J. Wang, J. Li, S. S. Li, and Y. Liu, "Hydrogen storage by metalized silicene and silicane," *J. Appl. Phys.*, vol. 114, no. 12, Sep. 2013, Art. no. 124309.
[61] Y. You, C. Yang, X. Zhang, H. Lin, and J. Shi, "Emerging two-dimensional silicene nanosheets for biomedical applications," *Mater. Today Nano*, vol. 16, Dec. 2021, Art. no. 100132.
[62] H. Lin et al., "Silicene: Wet-chemical exfoliation synthesis and biodegradable tumor nanomedicine," *Adv. Mater.*, vol. 31, no. 37, Sep. 2019, Art. no. 1903013.
[63] R. Gonzalez-Rodriguez, R. M. Del Castillo, E. Hathaway, Y. Lin, J. L. Coffer, and J. Cui, "Silicene/silicene oxide nanosheets for broadband photodetectors," *ACS Appl. Nano Mater.*, vol. 5, no. 3, pp. 4325–4335, Mar. 2022.
[64] H. Sadeghi, S. Bailey, and C. J. Lambert, "Silicene-based DNA nucleobase sensing," *Appl. Phys. Lett.*, vol. 104, no. 10, Mar. 2014, Art. no. 103104.
[65] D. C. Elias et al., "Control of graphene's properties by reversible hydrogenation: Evidence for graphane," *Science*, vol. 323, no. 5914, pp. 610–613, Jan. 2009.
[66] A. Molle, J. Goldberger, M. Houssa, Y. Xu, S. C. Zhang, and D. Akinwande, "Buckled two-dimensional Xene sheets," *Nature Mater.*, vol. 16, no. 2, pp. 163–169, Jan. 2017.
[67] M. Liao et al., "Superconductivity in few-layer stanene," *Nature Phys.*, vol. 14, no. 4, pp. 344–348, Apr. 2018.
[68] F. Reis et al., "Bismuthene on a SiC substrate: A candidate for a high-temperature quantum spin hall material," *Science*, vol. 357, no. 6348, pp. 287–290, Jun. 2017.
[69] P. Bampoulis et al., "Quantum spin hall states and topological phase transition in germanene," *Phys. Rev. Lett.*, vol. 130, no. 19, May 2023, Art. no. 196401.
[70] W. Wu, G. Qiu, Y. Wang, R. Wang, and P. Ye, "Tellurene: Its physical properties, scalable nanomanufacturing, and device applications," *Chem. Soc. Rev.*, vol. 47, no. 19, pp. 7203–7212, Oct. 2018.
[71] P. Y. Liao, J. K. Qin, G. Qiu, Y. Wang, W. Wu, and P. D. Ye, "Selenene and tellurene," in *Xenes 2D Synthetic Materials Beyond Graphene*. Sawston, U.K.: Woodhead Publishing, 2022, pp. 197–224.
[72] S. Ghomi et al., "Tailoring the dimensionality of tellurium nanostructures via vapor transport growth," *Mater. Sci. Semicond. Process.*, vol. 168, Dec. 2023, Art. no. 107838.
[73] C. Zhao et al., "Evaporated tellurium thin films for p-type field-effect transistors and circuits," *Nature Nanotechnol.*, vol. 15, no. 1, pp. 53–58, Dec. 2019.
[74] Y. Wang et al., "Field-effect transistors made from solution-grown two-dimensional tellurene," *Nature Electron.*, vol. 1, no. 4, pp. 228–236, Apr. 2018.
[75] X. Ren, Y. Wang, Z. Xie, F. Xue, C. Leighton, and C. D. Frisbie, "Gate-tuned insulator-metal transition in electrolyte-gated transistors based on tellurene," *Nano Lett.*, vol. 19, no. 7, pp. 4738–4744, Jul. 2019.
[76] A. M. Askar et al., "Two-dimensional tellurium-based diodes for RF applications," *npj 2D Mater. Appl.*, vol. 7, no. 1, pp. 1–11, Sep. 2023.
[77] C. Shen et al., "Tellurene photodetector with high gain and wide bandwidth," *ACS Nano*, vol. 14, no. 1, pp. 303–310, Jan. 2020.
[78] J. Peng et al., "Two-dimensional tellurium nanosheets exhibiting an anomalous switchable photoresponse with thickness dependence," *Angewandte Chemie Int. Ed.*, vol. 57, no. 41, pp. 13533–13537, Oct. 2018.
[79] G. Qiu et al., "Quantum hall effect of weyl fermions in n-type semiconducting tellurene," *Nature Nanotechnol.*, vol. 15, no. 7, pp. 585–591, Jun. 2020.
[80] X. Xu et al., "Growth of 2D materials at the wafer scale," *Adv. Mater.*, vol. 34, no. 14, Apr. 2022, Art. no. 2108258.
[81] G. Meyer and K. H. Rieder, "Low temperature STM study on the growth of ultrathin Ag films on Si(111)7 × 7," *Surf. Sci.*, vol. 331–333, no. PART A, pp. 600–605, Jul. 1995.
[82] K. Zhu et al., "The development of integrated circuits based on two-dimensional materials," *Nature Electron.*, vol. 4, no. 11, pp. 775–785, Nov. 2021.
[83] M. Lanza, Q. Smets, C. Huyghebaert, and L. J. Li, "Yield, variability, reliability, and stability of two-dimensional materials based solid-state electronic devices," *Nature Commun.*, vol. 11, no. 1, pp. 1–5, Dec. 2020.
[84] Y. Sassa et al., "Kagome-like silicene: A novel exotic form of two-dimensional epitaxial silicon," *Appl. Surf. Sci.*, vol. 530, Nov. 2020, Art. no. 147195.
[85] L. Meng et al., "Buckled silicene formation on Ir(111)," *Nano Lett.*, vol. 13, pp. 685–690, 2013.
[86] J. Zhao et al., "Ultrahigh-mobility semiconducting epitaxial graphene on silicon carbide," *Nature*, vol. 625, no. 7993, pp. 60–65, Jan. 2024.

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