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Temperature behavior and logic circuit applications of InAs nanowire-based field-effect transistors

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ABSTRACT

InAs nanowire-based back-gated field-effect transistors realized starting from individual InAs nanowires are investigated at different temperatures and as building blocks of inverter circuits for logic applications. The nanodevices show n-type behavior with a carrier concentration up to 8.0×10^{17} cm^{-3} and corresponding electron mobility exceeding 1590 and 1940 cm^2 V^{-1} s^{-1} at room temperature and 200 K, respectively. The investigation over a wide temperature range indicates no Schottky barrier at source/drain electrodes, where Ohmic contacts are formed with the Cr adhesion layer. The switching characteristics of the devices improve with decreasing temperature and a subthreshold swing less than 1 V/decade is achieved at 200 K, suggesting the occurrence of a trap population with density around 4×10^8 cm^{-1} eV^{-1}. Besides, the nanodevices are exploited in single-transistor circuits with a resistive load. As an inverter, the circuit shows 30 % and 24 % of the voltage supply noise margins for the high and low states, respectively; as a low signal amplifier, it shows a gain that is weakly dependent on temperature. The present study highlights the impact of temperature on the operation of InAs nanowire-based back-gated transistors and evidences their potential applications in logic circuits including inverters and low-signal amplifiers.

1. Introduction

Nanowires exhibit unique electronic and optical properties due to their small dimensions and high aspect ratio as well as quantum confinement effects, making them suitable for multiple applications in different fields including electronics, photonics, and sensing [1–9]. III-V semiconductor compounds, such as indium arsenide (InAs), are particularly attractive for high-speed electronic devices due to their low electron effective mass and high carrier mobility [3,7]. InAs nanowires, with their direct bandgap, also exhibit strong light-matter interaction and high absorption coefficients, lending themselves to nanoscale optoelectronic applications such as photodetectors, light emitting diodes, and solar cells [10]. Moreover, most of III-V semiconductors are characterized by a strong spin-orbit coupling, which makes them useful for spintronic applications and topological quantum computing [11,12]. Unlike their bulk counterparts, InAs nanowires can be grown in both the zinc blende (ZB) and wurtzite (WZ) crystal phases, each with its own crystal lattice structure [13,14] and a direct bandgap that ranges from 0.354 eV in the ZB to 0.477 eV in the WZ structure at room temperature, making them suitable for broad band detection [15,16]. They have been successfully used in photodetectors, including mid-wave infrared (MWIR) photodetection, where their high mobility and absorption coefficient contribute to low dark current and high detectivity [17–22].

Furthermore, InAs nanowires (NWs) can serve as conductive channels in field-effect transistors (FETs), showing a low contact resistance, as the reported 1.4×10^{-7} Ω cm^{-2} by M.J.L. Sourribes [23], and high charge carrier mobility exceeding 10000 cm^2 V^{-1} s^{-1} at temperature slightly above 100 K [24,25]. The high electron mobility, which is

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strongly influenced by several factors, such as the crystal quality, the size and morphology of the NW and the temperature, is due to the very high mobility of bulk InAs around 40000 $cm^2\ V^{-1}\ s^{-1}$ at room temperature [26]. Ultrathin InAs NWs have been employed in the fabrication of high-performance FETs, demonstrating a ratio between the on and off currents around 10^6 [27]. These NWs can be implemented in different architectures, improving the gate control of the electrostatic operation of the device. W. Luo et al. [28] investigated the simulation of synaptic behaviors with a gate-all-around InAs NW-FET, exploiting the strong gate control over the device. Additionally, a droplet of ionic liquid surrounding the nanodevice was used to implement a direct gate control based on iontronics, yielding a very efficient carrier modulation [29–31]. Moreover, M. Rocci et al. [32] implemented suspended InAs NWs in device architectures for the investigation of thermal conductivity using the 3ω method.

The temperature dependence of electrical properties is an important aspect to consider in the study of semiconducting materials and as regards InAs NW-based systems it is crucial to optimize the performance of the devices. In literature, a few works deal with temperature dependent electrical properties of FETs with single InAs NWs, mainly focusing on the temperature interval below 200 K. N. Gupta et al. [33] investigated the electrical transport in the temperature range from 10 to 200 K, revealing a more evident change in parameters above 50 K. In particular, the electron mobility changes its temperature dependence at 50 K. Because of the transport across severely confined 1D subbands in NWs, InAs NW-FET transfer characteristics exhibit step-like patterns below 50 K. It is also observed that the low field magnetoconductance depends on temperature. At 8 K, a spin-orbit interaction causes a modest antilocalization effect, which is shown by a negative magnetoconductance. As the temperature rises, the antilocalization effect gradually disappears, reaching a positive magnetoconductance at 25 K [34]. InAs NWs, as well as NWs based on other III-As compounds, are used for n-type metal-oxide-semiconductor FETs (MOSFETs), while Sb-based semiconductors are the most promising materials for p-type MOSFETs with hole mobilities up to 1500 $cm^2\ V^{-1}\ s^{-1}$ for InGaSb, 1300 $cm^2\ V^{-1}\ s^{-1}$ for GaSb, and over 1200 $cm^2\ V^{-1}\ s^{-1}$ for InSb at room temperature [26]. As regards the complementary MOS technology, devices based on III-V semiconductor compounds are preferred for NMOS transistors, but the leading PMOS structures are still based on Ge. However, InAs NWs are promising to push forward the Si-based electronics because they can grow directly on Si sensors without damaging the device, displaying competitive key parameters with respect to Si-based devices [35,36].

In this work, we use single InAs NWs as the conductive channel of FETs to investigate their electronic properties at room temperature and in unexplored low temperature range. We report the fabrication of back-gated transistors based on single InAs NWs drop-casted on a p^{++}-Si/SiO_2 substrate and we present and discuss the electrical characterization of the devices in the temperature range from 200 to 290 K, which is lacking in the literature. We show that the devices are more performant at lower temperatures, as suggested by the increase of the ratio between the on and the off currents and the decrease of the subthreshold swing. The Arrhenius plot confirms the presence of Ohmic contacts. The high quality of the interface between the semiconductor NW and the oxide layer is confirmed by the low value of the trap state density, $D_{trap} = 4 \times 10^8\ cm^{-1}\ eV^{-1}$. Finally, in order to demonstrate their suitability for digital technology, the InAs NW-based devices are employed as part of an inverter circuit that can be operated in a wide range of temperatures.

2. Experimental section

Nominally undoped InAs NWs were grown on InAs (111)B substrates by Au-assisted chemical beam epitaxy (CBE), in a Riber Compact-21 reactor [37]. Gold nanoparticle catalysts were obtained by thermal dewetting, in the growth chamber, of a 0.5 nm thick Au film that had previously been thermally evaporated on the substrate. The growth process took place at a temperature of (390 ± 10) °C, using tri-methylindium (TMIn) and tertiarybutylarsine (TBAs) metalorganic precursors. The grown NWs exhibit a WZ crystal structure (see Fig. 1a) with a hexagonal cross section, have diameters of about 100 nm and are around 4.5 μm long.

After the growth, the InAs NWs were mechanically detached from the growth substrate by sonication in isopropyl alcohol and randomly deposited on a p^{++}-Si/SiO_2 substrate (0.3 mm/280 nm) by drop casting. The NWs were contacted by a single step electron beam lithography (EBL) followed by an evaporation of a metallic bilayer (Cr/Au 10/100 nm) and lift-off. A passivation step in a highly diluted ammonium polysulfide $(NH_s)_2S_x$ – H_2O solution was performed prior to metal evaporation, to remove the native oxide from the NW surface in the contact areas and promote the formation of low resistance Ohmic contacts. The fabricated InAs NW-based devices were backgated with silver paste onto the degenerate Si substrate.

The scanning electron microscopy (SEM) top view image of the fabricated device is shown in Fig. 1b. The InAs NW is contacted by metal leads of Cr and Au, where chromium is used as adhesion layer. Cr, along with Ti and Ni, is commonly used as an adhesion layer for realizing metal electrodes on WZ InAs NWs [30,38–40]. In fact, due to the favorable Fermi level pinning in the conduction band at the semiconductor surface, Cr allows to easily obtain good Ohmic contacts with these nanostructures, provided a preliminary removal of the native oxide and passivation is performed [41]. The channel of the measured transistor is the part of the NW between the inner leads, indicated as source (S) and drain (D) in Fig. 1b. The channel length is $L = 1$ μm and the radius of the NW is about $r \approx 50$ nm. The radius of the NW was estimated from the SEM image. The schematic of the back-gated device, together with the measurement setup, is reported in Fig. 1c, where only the leads used as electrodes are depicted. The source is grounded, whereas the voltage bias is applied to the drain electrode. The gate voltage is applied to the Si substrate covered by silver paste. The drain and the gate voltages, V_{ds} and V_{gs}, respectively, were swept or stepped to monitor the drain current I_d.

The electrical measurements were carried out in two-probe configuration using a Janis ST-500 cryogenic probe station, connected to a Keithley 4200 semiconductor characterization system, having current and voltage sensitivity of about 0.1 pA and 2 μV, respectively. All the electrical measurements were performed in vacuum at 2 mbar pressure to avoid any contamination of the pure material. To investigate the temperature dependence of the electrical properties of InAs NWs, the substrate temperature was monitored using a Scientific Instruments Model 9700.

3. Results and discussion

The electrical behavior of InAs NWs was first investigated at room temperature, performing current-voltage measurements in dark. Then, the same device was measured lowering the temperature down to 200 K. Additionally, the thermionic mechanism that governs the metal source/drain FET operation is studied, extracting the subthreshold swing and the trap state density. Finally, the transistor is demonstrated as part of an inverter circuit, operating at room and low temperature.

3.1. Standard electrical characterization

Fig. 2 reports the electrical characterization of one of the fabricated transistors with an InAs NW as a conductive path. Fig. 2a shows the output characteristics, displaying the drain current I_d as a function of the voltage between source and drain V_{ds} at fixed gate voltage V_{gs}, while Fig. 2b shows the transfer characteristic, i.e., the measured I_d as a function of V_{gs} at fixed $V_{ds} = 10$ mV, both in forward and reverse direction (V_{gs} from −10 V to 10 V, and back from 10 V to −10 V). The drain current is modulated by both the drain and the gate voltage, as demonstrated by the output curves collected stepping V_{gs} from −10 to 10 V. Also, the gate current was monitored during the measurements, as

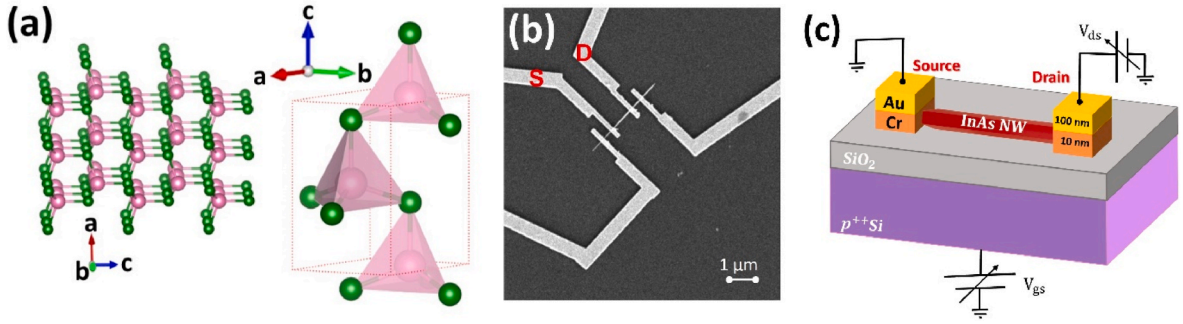

Fig. 1. (a) Schematic of InAs WZ atomic structure (the green and pink spheres represent the arsenic and indium atoms, respectively; the single unit cell is depicted with a red dotted line). (b) SEM image of the device with the NW as conductive channel and Cr/Au leads as source and drain electrodes. The channel length is 1 μm. (c) Schematic of the InAs NW-based back-gated FET with the measurement setup (only the leads used as electrodes are depicted).

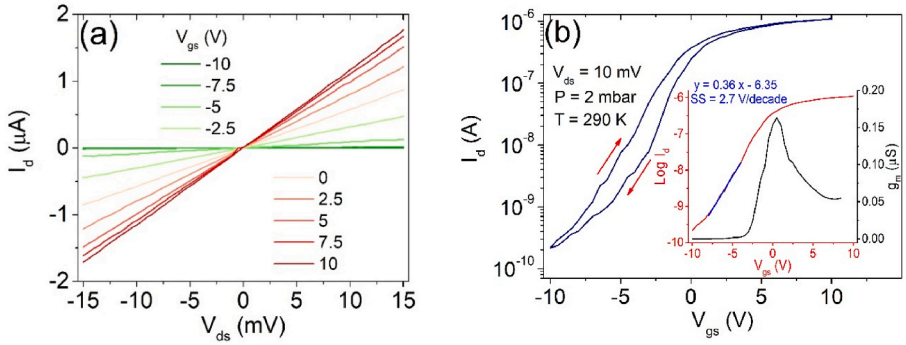

Fig. 2. Electrical measurements at room temperature of an InAs NW-based FET: (a) Output curves for V_{ds} sweep at given V_{gs}. (b) Transfer characteristic on semilog scale at $V_{ds} = 10$ mV. (In the inset: log transfer curve (red) with linear fit (blue) for the extraction of SS and transconductance curve (black).

reported in Fig. S1 in the Supporting Information. The linear behavior of the output curves indicates the presence of Ohmic contacts (InAs/Cr) over the explored V_{ds} interval, ranging from −15 to 15 mV. Since the current I_d decreases for negative V_{gs}, the device presents n-type conduction. It is worth mentioning that this behavior – despite the material being nominally undoped – is typical of Arsenic-based III-V semiconductor materials. The n-type conduction is confirmed by the transfer characteristic featuring higher current levels towards more positive gate voltage values. The estimated threshold voltage V_{th} is around −3 V, whose sign is typical of normally-on n-type FETs. The transistor under investigation operates efficiently: defining I_{ON} and I_{OFF} as the maximum and minimum recorded currents, respectively, the device shows a high I_{ON}/I_{OFF} ratio of 5×10^3 and a subthreshold swing $SS = \frac{dV_{gs}}{d\ \log_{10} I_d} \approx 2.7$ V/decade, whose extraction is displayed in the inset of Fig. 2b. The I_{OFF} of the order of 10^{-10} A contributes to lower the static power consumption, while the high channel current of the order of μA can be widely exploited for high-speed electronic devices. By sweeping the gate voltage backward and forward in the range from −10 to 10 V, a hysteretic behavior can be observed. The maximum hysteresis width, H_w, of the transfer characteristic, which is defined as the difference in voltage at the fixed current level of $I_d = 6$ nA, is less than 2 V. The origin of the hysteresis can be found in a charge redistribution under the gate electric stress, which can result in charge transfer, charge trapping or charge polarization. Indeed, a high value of H_w is typically undesirable because it makes the transistor operation affected by the gate voltage sweep range, direction, and time. To improve the stability and reliability of operation, it should be minimized or eliminated [42,43].

The transfer characteristic allows the extraction of the electron mobility from the transconductance values; the maximum field-effect mobility is calculated following the equation:

$$\mu_{FE} = g_{m,max} \frac{L}{C_{ox}\ V_{ds}}$$

The channel length is $L = 1$ μm, the drain voltage bias is $V_{ds} = 10$ mV and C_{ox} is the gate oxide capacitance. $g_{m,max} = \frac{dI_d}{dV_{gs}}$ is the maximum transconductance value; the transconductance curve in the backward direction is reported with a black line in the inset of Fig. 2b.

The fabricated device presents thermally generated SiO_2 that serves as the gate dielectric and a highly doped Si substrate that operates as the back-gate. To estimate C_{ox}, the "metallic cylinder on an infinite metal plate" approximation is used [44]. The charge density in the NW is assumed to be so high that the semiconducting NW can be treated as metallic. D. Vashaee et al. [45] showed the reliability of this approximation for GaN NWs with doping concentrations above 10^{17} cm^{-3}.

The fringing capacitance at the source and drain electrodes can be ignored because the NW length is one order of magnitude higher than the dielectric layer thickness - 1 μm vs 0.3 μm. However, this model assumes that the NW is completely embedded in the dielectric and possesses a circular cross section. It yields an analytical equation for the gate oxide capacitance per unit length $C_{ox} = \frac{C'_{ox}}{L} = \frac{2\pi\epsilon}{\cosh^{-1}\frac{(t_{ox}+r)}{r}}$, where C'_{ox} is the oxide capacitance, ε is the absolute dielectric constant and is given by the product of the constant of the embedding dielectric and the vacuum permittivity, $\varepsilon = \varepsilon_0\ \varepsilon_{SiO2}$, r is the radius of the NW, $r = 50$ nm, and t_{ox} is the oxide thickness equal to 280 nm. The estimated capacitance is $C_{ox} = 8.4 \times 10^{-11}$ F/m. The maximum mobility reached at room temperature is $\mu_{FE} = 1591$ cm^2 V^{-1} s^{-1}. By using this approximated model, the carrier mobility can be underestimated by a factor of almost 2 because the capacitance of non-embedded NWs is nearly two times lower than the value calculated as reported above. The overestimation of C_{ox} is confirmed by studies based on finite element method, implemented by O. Wunnicke [46].

The carrier concentration, which is defined as $n = \frac{C_{ox}(V_{gs}-V_{th})}{e\pi r^2}$, is equal to $n = 8.2 \times 10^{17}$ cm^{-3}, at room temperature [47]; this demonstrates the self-consistence of our method [45].

3.2. Temperature dependence of the electrical characteristics

The temperature dependence of the transistor transfer characteristics is investigated in the range (200–290) K, performing current-voltage measurements every 10 K. Fig. 3a reports some of the transfer characteristics at $V_{ds} = 10$ mV, with V_{gs} from −10 to 10 V, showing the n-type behavior. This behavior is preserved when the temperature is lowered but the current decreases and the effect is particularly evident in the subthreshold region. The inset of Fig. 3a shows the output characteristics at $V_{gs} = 0$ V and $V_{gs} = 10$ V. The linear behavior of the output curves at different temperatures emphasizes the Ohmic character of the contacts between Cr and the NW, and this is confirmed by the negligible Schottky barrier height (SBH), extracted from the Arrhenius plot, which is depicted in the inset of Fig. 3b. SBH largely affects the transport mechanism, especially when the transistor conductive path is made of a semiconductive NW. The current in the thermionic region can be fitted by the following equation:

$$I_d = SA^*T^2 \exp\left(-\frac{e\Phi_B}{k_B T}\right)\left[1 - \exp\left(-\frac{eV_{ds}}{k_B T}\right)\right]$$

where S is the cross-section area of the NW channel, A* is the Richardson constant, k_B is the Boltzmann constant, and e is the elementary electron charge [48].

The slopes of the linear fit of the Arrhenius curves correspond to the barrier height, φ_B, at different gate voltages. By plotting φ_B as a function of V_{gs}, in absence of Schottky barrier, the voltage bias at which φ_B-V_{gs} plot shows a kink is the value that distinguishes between the on and the off region, V_{th} [48–51]. In Fig. 3b the dependence of φ_B on V_{gs} is shown. At $V_{th} = -3$ V, the transition from the off to the on region can be observed. Indeed, for $V_{gs} > V_{th}$, the device is in on-state operation. For $V_{gs} < V_{th}$, thermionic emission over the channel barrier is the only allowed transport mechanism [48,52]. The thermionic emission over the barrier can be investigated from the slope of the transfer characteristics in the subthreshold region. The subthreshold swing, SS, is defined as the change in gate voltage per decade of current and it is extracted for -7 V $< V_{gs} < -4$ V. It becomes lower than 1 V/decade at 200 K. The device operation can be described through the lowering of the barrier between source and drain; the charge flow in the channel results to be proportional to the concentration of electrons that can overcome the barrier. It can be demonstrated that the current in the subthreshold region has the following dependence [53].

$$I_d \propto e^{\frac{q(V_{gs}-V_{th})}{k_B T\left[1+(C_d+C_{it}/C_{ox})\right]}}$$

in which C_d, C_{it} and C_{ox} are the depletion, the interface trap, and the gate oxide capacitance per unit length, respectively. Taking the derivative of

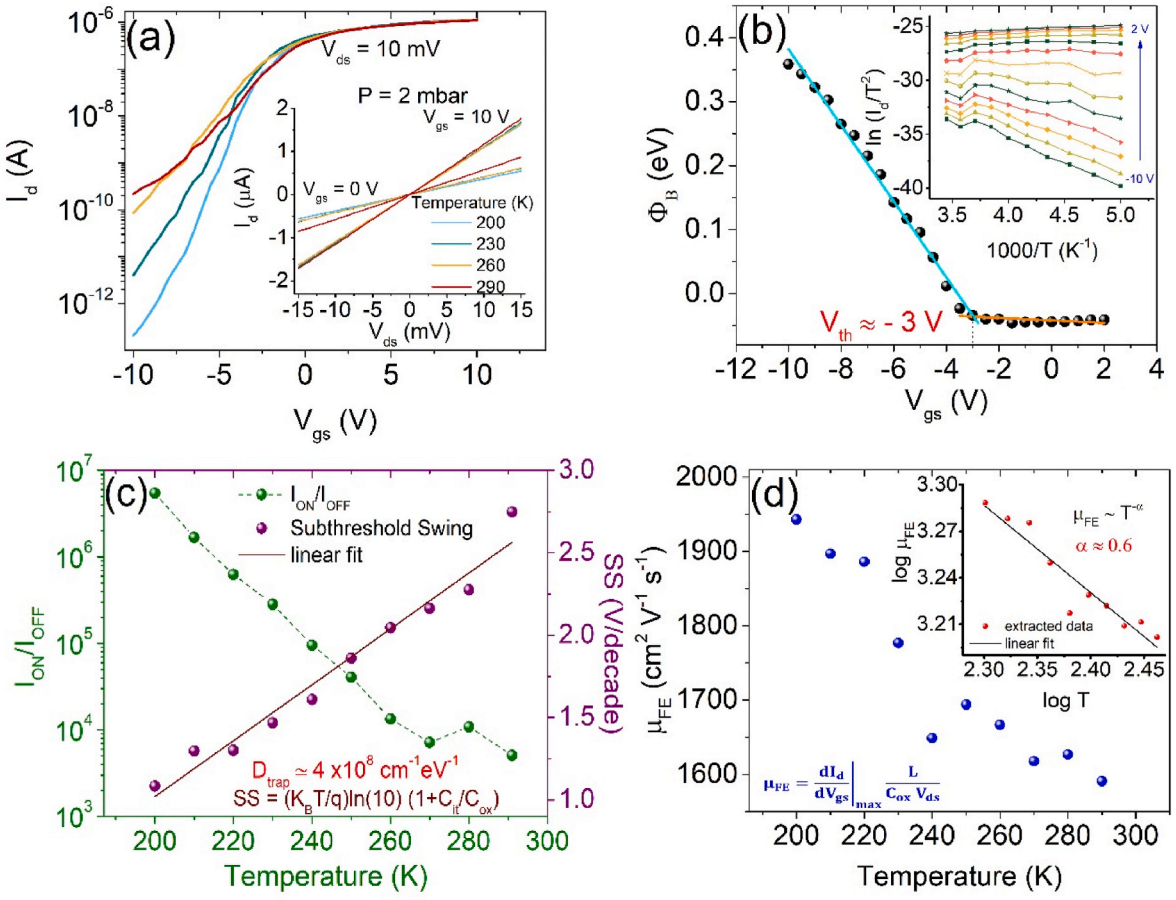

Fig. 3. (a) Electrical measurements in (200, 290) K range. Transfer characteristics on semilog scale at $V_{ds} = 10$ mV and T = 200, 230, 260, 290 K. (In the inset: Output curves at $V_{gs} = 0$ V and $V_{gs} = 10$ V at the same temperatures of the transfer curves) (b) Effective barrier height φ_B extracted from the Arrhenius plot as a function of V_{gs}. φ_{SBH} results to be negligible. (In the inset: Arrhenius plot at V_{gs} between −10 V and 2 V) (c) I_{ON}/I_{OFF} on semilog scale (green dots) and SS (purple dots) as a function of temperature. The density of trap states extracted from the linear fit of SS is $D_{trap} = 4 \times 10^8$ cm^{-1} eV^{-1}. (c) Temperature dependence of field-effect mobility in the temperature range from 200 to 290 K. (In the inset: Mobility as a function of temperature on log scale. The fit with the power law $T^{-\alpha}$ gives the estimation of the parameter, $\alpha \sim 0.6$).

the logarithm of I_d with respect to V_{gs}, the SS is given by

$$SS = \left(\frac{d \log I_d}{dV_{gs}}\right)^{-1} = \frac{k_B T}{q}\left(1 + \frac{C_d + C_{it}}{C_{ox}}\right) \ln 10$$

Because of the structure of the device presented previously, the source and drain capacitances can be negligible. In the subthreshold region, the NW is fully depleted, and C_d is negligible. The linear fit of SS as a function of temperature, which is presented in Fig. 3c, provides the estimation of the density of trap states at the Fermi energy E_F, considering that $C_{it} = q^2 D_{trap}(E_F)$ [54,55]. The extracted value is $D_{trap} = 4 \times 10^8$ cm^{-1} eV^{-1}. As a transistor metric, the SS indicates how sharply the transistor switches on and off. A related figure of merit is the I_{ON}/I_{OFF} ratio: the higher the ratio, the more the device is suitable for digital applications. Moreover, an important goal of electronics is the lowering of static power dissipation, which corresponds to low currents when the device is switched off. A strong reduction in the off current can be observed from the transfer characteristics. Fig. 3c also reports I_{ON}/I_{OFF} as a function of temperature. It increases by three orders of magnitude, reaching 5×10^6, lowering the temperature from 290 to 200 K.

Fig. 3d reports the field-effect electron mobility dependence on temperature. It was calculated using the same formula detailed in the previous paragraph. The transconductance curves at different temperatures are depicted in Fig. S2 in the Supporting Information. Two competing phenomena, which are the ionized impurity scattering and phonon scattering, generally limit the semiconductor mobility [56–58]. The first mechanism is dominant at very low temperatures and yields an increasing mobility with increasing temperature, while at higher temperatures phonon scattering becomes the main mechanism and causes a decrease in mobility with increasing temperature [59–61]. The influence of scattering mechanism from charged impurities can be observed below 50 K for InAs NWs based transistors [33]. In our InAs FETs the field-effect mobility goes from 1591 to 1943 cm^2 V^{-1} s^{-1}, lowering the temperature from 290 to 200 K. The obtained mobilities are consistent with the literature (see Table I in the Supporting Information). The change in the mobility can be described by a power law, $\mu_{FE} \sim T^{-\alpha}$. Fitting the experimental data with the power function, as reported in the inset of Fig. 3d, the α parameter results to be (0.6 ± 0.1). Indeed, the mobility dependence on temperature due to optical phonon scattering only is expected to be proportional to $T^{-0.5}$ [62]. Therefore, in the explored temperature range, the most dominant scattering mechanism should be due to optical phonons. This result is consistent with the InAs WZ phase, which is characterized by three low-lying optical and six highly placed optical branches, in addition to three acoustic branches [63].

3.3. Inverter

InAs has remarkable applications in the wide field of digital

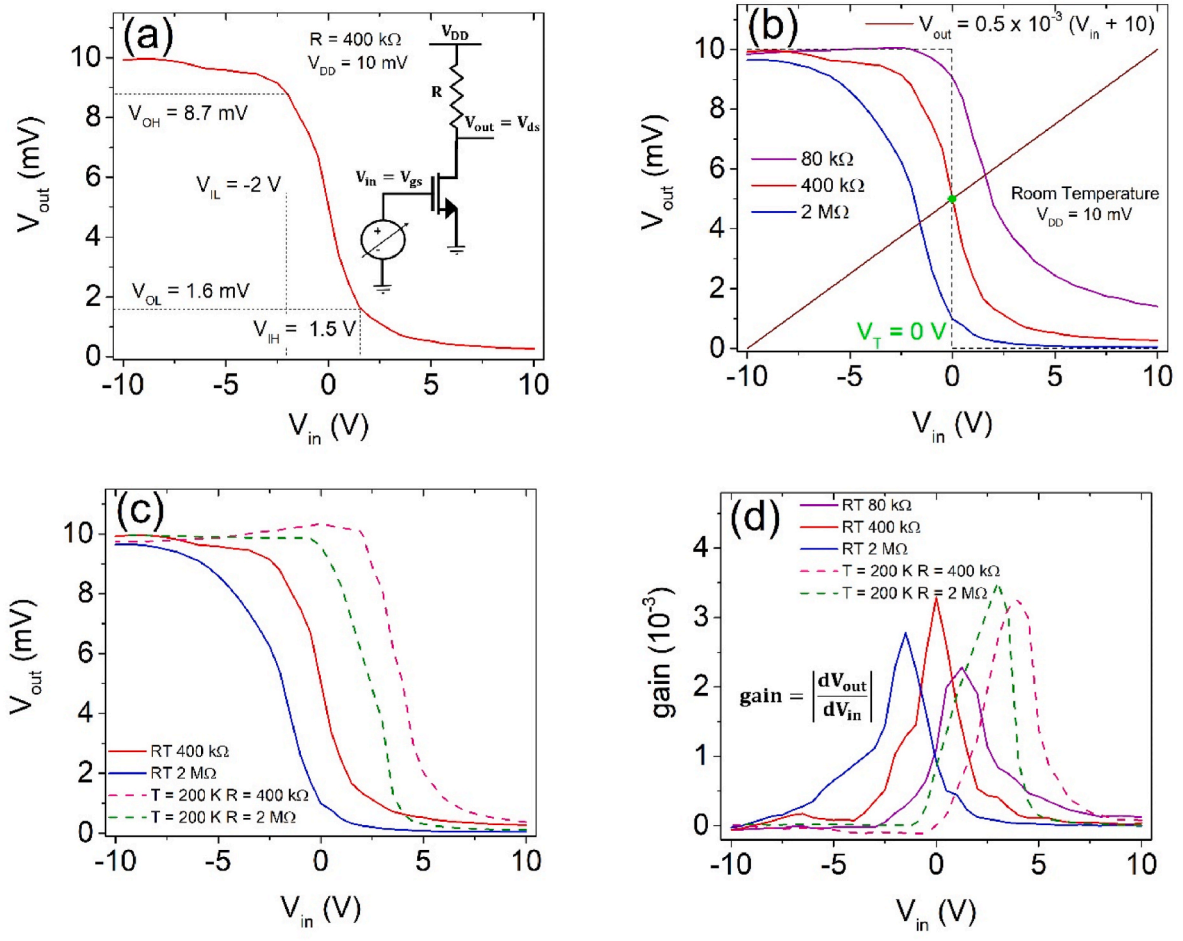

Fig. 4. Inverters measurements: (a) Voltage-transfer-characteristic (VTC) of the resistive load inverter based on the InAs NW-based transistor with a 400 kΩ resistor, obtained at $V_{DD} = 10$ mV. The evidenced points of the VTC are characterized by a slope equal to 1×10^{-3}. The extracted noise margins correspond to 30 % and 24 % of V_{DD} for the high and the low level, respectively. The schematic of the analyzed inverter is reported as inset. (b) VTCs of the resistive load InAs NW-based inverters with different resistors. The dashed curve is the ideal inverter characteristic. The reported green dot shows the threshold voltage of the inverter with a 400 kΩ resistor. (c) VTCs at room temperature (RT, solid lines) and 200 K (dashed lines) with different resistors. (d) Gain of the different inverters implemented at room temperature and 200 K with different resistors.

electronics that is based on logic operations implemented through different circuits. The core of all digital designs is the inverter, which represents the fundamental logic gate able to perform a Boolean operation with only one input variable. It provides the implementation of the logical negation [64]. The NOT operation converts the logic level from *one* into *zero*, and vice versa. The behavior of more complicated gates, such as NAND, NOR or XOR, which are the building blocks for other modules like multipliers and processors, can be explained by extending the analysis of inverters [65,66].

The InAs NW-based transistor was employed in a resistive load inverter circuit, whose schematic is shown in the inset of Fig. 4a. The driver transistor is the n-type NW-based FET investigated in the previous sections. The load consists of a resistor R, whose optimal resistance results to be about 400 kΩ. The power supply of the circuit is $V_{DD} = 10$ mV, the input voltage of the inverter is equal to the voltage applied to the gate electrode, $V_{in} = V_{gs}$, and the output voltage of the inverter is equal to the drop voltage between source and drain, $V_{out} = V_{ds}$. While applying a gate voltage sweep from −10 to 10 V, the drain voltage was monitored as the outcome of the circuit. Although the coupling between a transistor and a resistor is not the most advantageous approach for power consumption and processing speed, it results to be low cost and easy to implement. Firstly, the analysis was conducted at room temperature.

Fig. 4a shows the voltage-transfer-characteristic (VTC) of the inverter, i.e. V_{out} versus V_{in}. When the applied gate voltage is lower than the transistor threshold voltage, $V_{gs} < V_{th}$, the transistor is off, and it is expected to have $V_{out} = V_{DD}$ that is referred as a logical 1. Meanwhile, when $V_{gs} > V_{th}$, the transistor is on and a logical 0 is expected as outcome. This mostly depends on the specific transistor properties, the resistive load and the voltages applied as input. The logical states 1 and 0 are not associated to fixed voltage values, but to voltage intervals that can be defined by identifying two characteristic points of the VTC [67]. Along the transient region of the VTC, the two points at which the curve slope is equal to the ratio between V_{DD} and the maximum V_{in}, about 10^{-3}, were selected. V_{IL} and V_{IH} are defined as the maximum and minimum input voltage considerable as logical 0 and 1, respectively. The corresponding output voltages, V_{OH} and V_{OL}, are defined as the maximum and minimum output voltage considerable as logical 1 and 0. The noise margins (NMs) for both high and low logic levels were estimated. To evaluate NM_H and NM_L, which refer to the HIGH and the LOW signals, V_{IH} and V_{IL} are rescaled considering that V_{in} ranges from −10 to 10 V, while V_{out} from 0 to 10 mV. They are defined as $NM_H = V_{OH}–V_{IH,mod}$ and $NM_L = V_{IL,mod} – V_{OL}$, where $V_{IH,mod} = 0.5 \times 10^{-3}$ x $(V_{IH} + 10)$ V and $V_{IL,mod} = 0.5 \times 10^{-3}$ x $(V_{IL} + 10)$ V. The percentage of variation with reference to V_{DD}, 10 mV, is 30 % for NM_H and 24 % for NM_L. The noise margins represent the tolerance to signal fluctuations. The obtained values are well above the minimum requirement that the noise margin should be at least 10 % of V_{DD} [68]. The extracted noise margins evidence the robustness of the inverter toward noise for multistage operations. Several digital applications use multiple inverters connected in series; in these cases, the output signal from one stage serves as the input signal for the subsequent step [69,70]. Hence, NM_L and NM_H indicate the noise margins that the inverter can tolerate for multistage operations, which is crucial for the demonstration of ring oscillator and SRAM, as example [71].

The threshold voltage of the inverter, V_T, was estimated by the intersection of the VTC and the linear equation $V_{out} = 0.5 \times 10^{-3}$ $(V_{in} + 10)$, as depicted in Fig. 4b. The equation parameters were rescaled to make $V_{out} = V_{in}$, because V_{in} and V_{out} ranges are different in size and order of magnitude. The inverter with the 400 kΩ resistor has V_T around 0 V. Fig. 4b reports the VTC of different inverter circuits with resistors of 80 kΩ, 400 kΩ and 2 MΩ. The ideal characteristic curve is dashed to compare the three VTCs to it. It is evident that the curve of the inverter with 400 kΩ resistor has a more similar behavior to the ideal characteristic with respect to the other VTCs [67,72,73]. Moreover, the red VTC is symmetric in the V_{in} range. The curve with the lowest resistance presents the worst performance, as demonstrated by its slope, the right shift of V_T and the higher zero logical state that can reach.

The performance of the inverter was also tested at T = 200 K, both with the 0.4 and 2 MΩ resistors. The measured VTCs are reported in Fig. 4c. The threshold voltage V_T shifts to higher voltage values, making the curve lose the symmetric behavior highlighted at room temperature with 0.4 MΩ. However, the inverter is still working at low temperature, showing comparable small transient regions [74].

An important challenge in the realization of this type of inverters consists of the reduction of the transient region whose width is related to the slope of the curve connecting the high and low logical levels. Indeed, an effective figure-of-merit of inverter operation is the slope of the transition region, which provides a measure of the inverter gain, defined as $|dV_{out}/dV_{in}|$. It must be higher than the ratio between the output and input ranges to guarantee the regeneration of the logical states, i.e. greater than 5×10^{-4} (10 mV/20 V = 5×10^{-4}) [75–77]. In Fig. 4d the gain curves for all the investigated InAs NW-based inverters are reported. It is quite constant around 3×10^{-3}, which is one order of magnitude higher than the minimum expected value. The lowest gain is exhibited by the inverter with the resistor of 80 kΩ, and this is consistent with the previous comments.

4. Conclusion

We have fabricated and electrically characterized back-gated field-effect transistors with a single InAs NW as conductive channel and Cr/Au metal electrodes as the source and the drain, at different temperatures and in different circuit configurations. The devices show n-type conduction with a charge carrier mobility up to 1943 $cm^2 V^{-1} s^{-1}$ at 200 K; the mobility was estimated by using the "metallic cylinder on an infinite metal plate" approximation to calculate the gate capacitance. The transfer characteristic presents a low-hysteretic behavior, which evidences the crystallinity of the NW and the good quality of the interface with SiO_2. We have investigated the temperature dependence in the 200–290 K range. The Ohmic contacts between Cr and InAs NW are confirmed by the absence of a Schottky barrier. The thermionic emission over the channel barrier has been investigated and the subthreshold swing has been used to evaluate the density of trap states as $D_{trap} = 4 \times 10^8$ $cm^{-1} eV^{-1}$. Also, the field-effect mobility has shown an increase with the lowering of temperature, which is a typical behavior observed in semiconductors in the temperature regime where the main scattering mechanism is due to phonons and the mobility follows the power law $T^{-\alpha}$, with α around 0.6. Finally, we have reported the characterization of a resistive load inverter circuit using the InAs NW-based transistor. We have demonstrated the good performance of the inverter also at 200 K, showing a quite constant gain in at both room and low temperatures. Our results are promising for the integration of InAs NWs into digital devices.

CRediT authorship contribution statement

Loredana Viscardi: Writing – original draft, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Enver Faella:** Methodology, Investigation, Data curation. **Kimberly Intonti:** Methodology, Investigation, Data curation. **Filippo Giubileo:** Methodology, Investigation, Data curation. **Valeria Demontis:** Resources, Methodology, Formal analysis. **Domenic Prete:** Software, Resources, Formal analysis. **Valentina Zannier:** Visualization, Validation, Resources, Funding acquisition. **Lucia Sorba:** Writing – review & editing, Validation, Supervision, Resources. **Francesco Rossella:** Writing – review & editing, Validation, Supervision, Resources. **Antonio Di Bartolomeo:** Writing – original draft, Formal Analysis, Conceptualization, Resources, Supervision, Validation, Project administration.

Declaration of competing interest

The authors declare that they have no known competing financial

interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.mssp.2024.108167.

References

[1] W. Lu, C.M. Lieber, Semiconductor nanowires, J. Phys. D Appl. Phys. 39 (21) (2006) R387, https://doi.org/10.1088/0022-3727/39/21/R01.
[2] H.J. Joyce, J.L. Boland, C.L. Davies, S.A. Baig, M.B. Johnston, A review of the electrical properties of semiconductor nanowires: insights gained from terahertz conductivity spectroscopy, Semicond. Sci. Technol. 31 (10) (2016) 103003, https://doi.org/10.1088/0268-1242/31/10/103003.
[3] A. Agarwal, G. Misra, K. Agarwal, Semiconductor III–V nanowires: synthesis, fabrication and characterization of nanodevices, J. Inst. Eng. India Ser. B 103 (2) (2022) 699–709, https://doi.org/10.1007/s40031-021-00671-w.
[4] I. Leontis, A. Othonos, A.G. Nassiopoulou, Structure, morphology, and photoluminescence of porous Si nanowires: effect of different chemical treatments, Nanoscale Res. Lett. 8 (1) (2013) 383, https://doi.org/10.1186/1556-276X-8-383.
[5] C. Jia, Z. Lin, Y. Huang, X. Duan, Nanowire electronics: from nanoscale to macroscale, Chem. Rev. 119 (15) (2019) 9074–9135, https://doi.org/10.1021/acs.chemrev.9b00164.
[6] V. Demontis, V. Zannier, L. Sorba, F. Rossella, Surface nano-patterning for the bottom-up growth of III-V semiconductor nanowire ordered arrays, Nanomaterials 11 (8) (2021) 2079, https://doi.org/10.3390/nano11082079.
[7] E. Barrigón, M. Heurlin, Z. Bi, B. Monemar, L. Samuelson, Synthesis and applications of III–V nanowires, Chem. Rev. 119 (15) (2019) 9170–9220, https://doi.org/10.1021/acs.chemrev.9b00075.
[8] F. Giubileo, A.D. Bartolomeo, Y. Zhong, S. Zhao, M. Passacantando, Field emission from AlGaN nanowires with low turn-on field, Nanotechnology 31 (47) (2020) 475702, https://doi.org/10.1088/1361-6528/abaf22.
[9] F. Giubileo, M. Passacantando, F. Urban, A. Grillo, L. Iemmo, A. Pelella, C. Goosney, R. LaPierre, A. Di Bartolomeo, Field emission characteristics of InSb patterned nanowires, Advanced Electronic Materials 6 (10) (2020) 2000402, https://doi.org/10.1002/aelm.202000402.
[10] R.R. LaPierre, M. Robson, K.M. Azizur-Rahman, P. Kuyanov, A review of III–V nanowire infrared photodetectors and sensors, J. Phys. D Appl. Phys. 50 (12) (2017) 123001, https://doi.org/10.1088/1361-6463/aa5ab3.
[11] C. Fasth, A. Fuhrer, M.T. Björk, L. Samuelson, Tunable double quantum dots in InAs nanowires defined by local gate electrodes, Nano Lett. 5 (7) (2005) 1487–1490, https://doi.org/10.1021/nl050850i.
[12] C. Fasth, A. Fuhrer, L. Samuelson, V.N. Golovach, D. Loss, Direct measurement of the spin-orbit interaction in a two-electron InAs nanowire quantum dot, Phys. Rev. Lett. 98 (26) (2007) 266801, https://doi.org/10.1103/PhysRevLett.98.266801.
[13] A.R. Ullah, H.J. Joyce, A.M. Burke, J. Wong-Leung, H.H. Tan, C. Jagadish, A. P. Micolich, Electronic comparison of InAs wurtzite and zincblende phases using nanowire transistors: electronic comparison of InAs wurtzite and zincblende phases using nanowire transistors, Phys. Status Solidi RRL 7 (10) (2013) 911–914, https://doi.org/10.1002/pssr.201308014.
[14] S.A. Dayeh, D. Susac, K.L. Kavanagh, E.T. Yu, D. Wang, Structural and room-temperature transport properties of zinc blende and wurtzite InAs nanowires, Adv. Funct. Mater. 19 (13) (2009) 2102–2108, https://doi.org/10.1002/adfm.200801307.
[15] M.B. Rota, A.S. Ameruddin, H.A. Fonseka, Q. Gao, F. Mura, A. Polimeni, A. Miriametro, H.H. Tan, C. Jagadish, M. Capizzi, Bandgap energy of wurtzite InAs nanowires, Nano Lett. 16 (8) (2016) 5197–5203, https://doi.org/10.1021/acs.nanolett.6b02205.
[16] T. Xu, H. Wang, X. Chen, M. Luo, L. Zhang, Y. Wang, F. Chen, C. Shan, C. Yu, Recent progress on infrared photodetectors based on InAs and InAsSb nanowires, Nanotechnology 31 (29) (2020) 294004, https://doi.org/10.1088/1361-6528/ab8591.
[17] H. Fang, W. Hu, P. Wang, N. Guo, W. Luo, D. Zheng, F. Gong, M. Luo, H. Tian, X. Zhang, C. Luo, X. Wu, P. Chen, L. Liao, A. Pan, X. Chen, W. Lu, Visible light-assisted high-performance mid-infrared photodetectors based on single InAs nanowire, Nano Lett. 16 (10) (2016) 6416–6424, https://doi.org/10.1021/acs.nanolett.6b02860.
[18] E.A. Anyebe, I. Sandall, Z.M. Jin, A.M. Sanchez, M.K. Rajpalke, T.D. Veal, Y.C. Cao, H.D. Li, R. Harvey, Q.D. Zhuang, Optimization of self-catalyzed InAs nanowires on flexible graphite for photovoltaic infrared photodetectors, Sci. Rep. 7 (1) (2017) 46110, https://doi.org/10.1038/srep46110.
[19] D. Ren, X. Meng, Z. Rong, M. Cao, A.C. Farrell, S. Somasundaram, K.M. Azizur-Rahman, B.S. Williams, D.L. Huffaker, Uncooled photodetector at short-wavelength infrared using InAs nanowire photoabsorbers on InP with $p - n$ heterojunctions, Nano Lett. 18 (12) (2018) 7901–7908, https://doi.org/10.1021/acs.nanolett.8b03775.
[20] J. Svensson, N. Anttu, N. Vainorius, B.M. Borg, L.-E. Wernersson, Diameter-dependent photocurrent in InAsSb nanowire infrared photodetectors, Nano Lett. 13 (4) (2013) 1380–1385, https://doi.org/10.1021/nl303751d.
[21] W.-J. Lee, P. Senanayake, A.C. Farrell, A. Lin, C.-H. Hung, D.L. Huffaker, High quantum efficiency nanopillar photodiodes overcoming the diffraction limit of light, Nano Lett. 16 (1) (2016) 199–204, https://doi.org/10.1021/acs.nanolett.5b03485.
[22] D. Ren, K.M. Azizur-Rahman, Z. Rong, B.-C. Juang, S. Somasundaram, M. Shahili, A.C. Farrell, B.S. Williams, D.L. Huffaker, Room-temperature midwavelength infrared InAsSb nanowire photodetector arrays with Al2O3 passivation, Nano Lett. 19 (5) (2019) 2793–2802, https://doi.org/10.1021/acs.nanolett.8b04420.
[23] M.J.L. Sourribes, I. Isakov, M. Panfilova, P.A. Warburton, Minimization of the contact resistance between InAs nanowires and metallic contacts, Nanotechnology 24 (4) (2013) 045703, https://doi.org/10.1088/0957-4484/24/4/045703.
[24] A.C. Ford, J.C. Ho, Y.-L. Chueh, Y.-C. Tseng, Z. Fan, J. Guo, J. Bokor, A. Javey, Diameter-dependent electron mobility of InAs nanowires, Nano Lett. 9 (1) (2009) 360–365, https://doi.org/10.1021/nl803154m.
[25] S. Roddaro, D. Ercolani, M.A. Safeen, S. Suomalainen, F. Rossella, F. Giazotto, L. Sorba, F. Beltram, Giant thermovoltage in single InAs nanowire field-effect transistors, Nano Lett. 13 (8) (2013) 3638–3642, https://doi.org/10.1021/nl401482p.
[26] J.A. del Alamo, Nanometre-scale electronics with III–V compound semiconductors, Nature 479 (7373) (2011) 317–323, https://doi.org/10.1038/nature10677.
[27] D. Pan, M. Fu, X. Yu, X. Wang, L. Zhu, S. Nie, S. Wang, Q. Chen, P. Xiong, S. von Molnár, J. Zhao, Controlled synthesis of phase-pure InAs nanowires on Si(111) by diminishing the diameter to 10 nm, Nano Lett. 14 (3) (2014) 1214–1220, https://doi.org/10.1021/nl4040847.
[28] W. Luo, C. Zha, X. Zhang, X. Yan, X. Ren, Synaptic devices based on gate-all-around InAs nanowire field effect transistor, J. Phys.: Conf. Ser. 2370 (1) (2022) 012015, https://doi.org/10.1088/1742-6596/2370/1/012015.
[29] J. Lieb, V. Demontis, D. Prete, D. Ercolani, V. Zannier, L. Sorba, S. Ono, F. Beltram, B. Sacépé, F. Rossella, Ionic-liquid gating of InAs nanowire-based field-effect transistors, Adv. Funct. Mater. 29 (3) (2019) 1804378, https://doi.org/10.1002/adfm.201804378.
[30] D. Prete, E. Dimaggio, V. Demontis, V. Zannier, M.J. Rodriguez-Douton, L. Guazzelli, F. Beltram, L. Sorba, G. Pennelli, F. Rossella, Electrostatic control of the thermoelectric figure of merit in ion-gated nanotransistors, Adv. Funct. Mater. 31 (37) (2021) 2104175, https://doi.org/10.1002/adfm.202104175.
[31] D. Prete, V. Demontis, V. Zannier, M.J. Rodriguez-Douton, L. Guazzelli, F. Beltram, L. Sorba, F. Rossella, Impact of electrostatic doping on carrier concentration and mobility in InAs nanowires, Nanotechnology 32 (14) (2021) 145204, https://doi.org/10.1088/1361-6528/abd659.
[32] M. Rocci, V. Demontis, D. Prete, D. Ercolani, L. Sorba, F. Beltram, G. Pennelli, S. Roddaro, F. Rossella, Suspended InAs nanowire-based devices for thermal conductivity measurement using the 3ω method, J. Mater. Eng. Perform. 27 (12) (2018) 6299–6305, https://doi.org/10.1007/s11665-018-3715-x.
[33] N. Gupta, Y. Song, G.W. Holloway, U. Sinha, C.M. Haapamaki, R.R. LaPierre, J. Baugh, Temperature-dependent electron mobility in InAs nanowires, Nanotechnology 24 (22) (2013) 225202, https://doi.org/10.1088/0957-4484/24/22/225202.
[34] L.B. Wang, J.K. Guo, N. Kang, D. Pan, S. Li, D. Fan, J. Zhao, H.Q. Xu, Phase-coherent transport and spin relaxation in InAs nanowires grown by molecule beam epitaxy, Appl. Phys. Lett. 106 (17) (2015) 173105, https://doi.org/10.1063/1.4919390.
[35] Y. Cui, X. Duan, J. Hu, C.M. Lieber, Doping and electrical transport in silicon nanowires, J. Phys. Chem. B 104 (22) (2000) 5213–5216, https://doi.org/10.1021/jp0009305.
[36] J. Nah, H. Fang, C. Wang, K. Takei, M.H. Lee, E. Plis, S. Krishna, A. Javey III–V, Complementary metal–oxide–semiconductor electronics on silicon substrates, Nano Lett. 12 (7) (2012) 3592–3595, https://doi.org/10.1021/nl301254z.

[37] U.P. Gomes, D. Ercolani, V. Zannier, F. Beltram, L. Sorba, Controlling the diameter distribution and density of InAs nanowires grown by Au-assisted methods, Semicond. Sci. Technol. 30 (11) (2015) 115012, https://doi.org/10.1088/0268-1242/30/11/115012.
[38] L. Viscardi, K. Intonti, A. Kumar, E. Faella, A. Pelella, F. Giubileo, S. Sleziona, O. Kharsah, M. Schleberger, A. Di Bartolomeo, Black phosphorus nanosheets in field effect transistors with Ni and NiCr contacts, Phys. Status Solidi (2023) 2200537, https://doi.org/10.1002/pssb.202200537.
[39] W. Zhang, W.-H. Han, X.-S. Zhao, Q.-F. Lv, X.-H. Ji, T. Yang, F.-H. Yang, Horizontal InAs nanowire transistors grown on patterned silicon-on-insulator substrate, Chin. Phys. B 26 (8) (2017) 088101, https://doi.org/10.1088/1674-1056/26/8/088101.
[40] M. Fu, D. Pan, Y. Yang, T. Shi, Z. Zhang, J. Zhao, H.Q. Xu, Q. Chen, Electrical characteristics of field-effect transistors based on indium arsenide nanowire thinner than 10 nm, Appl. Phys. Lett. 105 (14) (2014) 143101, https://doi.org/10.1063/1.4897496.
[41] D.B. Suyatin, C. Thelander, M.T. Björk, I. Maximov, L. Samuelson, Sulfur passivation for ohmic contact formation to InAs nanowires, Nanotechnology 18 (10) (2007) 105307, https://doi.org/10.1088/0957-4484/18/10/105307.
[42] A. Di Bartolomeo, L. Genovese, F. Giubileo, L. Iemmo, G. Luongo, T. Foller, M. Schleberger, Hysteresis in the transfer characteristics of MoS_2 transistors, 2D Mater. 5 (1) (2017) 015014, https://doi.org/10.1088/2053-1583/aa91a7.
[43] F. Urban, F. Giubileo, A. Grillo, L. Iemmo, G. Luongo, M. Passacantando, T. Foller, L. Madauß, E. Pollmann, M.P. Geller, D. Oing, M. Schleberger, A. Di Bartolomeo, Gas dependent hysteresis in MoS_2 field effect transistors, 2D Mater. 6 (4) (2019) 045049, https://doi.org/10.1088/2053-1583/ab4020.
[44] D.R. Khanal, J. Wu, Gate coupling and charge distribution in nanowire field effect transistors, Nano Lett. 7 (9) (2007) 2778–2783, https://doi.org/10.1021/nl071330l.
[45] D. Vashaee, A. Shakouri, J. Goldberger, T. Kuykendall, P. Pauzauskie, P. Yang, Electrostatics of nanowire transistors with triangular cross sections, J. Appl. Phys. 99 (5) (2006) 054310, https://doi.org/10.1063/1.2168229.
[46] O. Wunnicke, Gate capacitance of back-gated nanowire field-effect transistors, Appl. Phys. Lett. 89 (8) (2006) 083102, https://doi.org/10.1063/1.2337853.
[47] S. Heedt, I. Otto, K. Sladek, H. Hardtdegen, J. Schubert, N. Demarina, H. Lüth, D. Grützmacher, T. Schäpers, Resolving ambiguities in nanowire field-effect transistor characterization, Nanoscale 7 (43) (2015) 18188–18197, https://doi.org/10.1039/C5NR03608A.
[48] D. Fan, N. Kang, S.G. Ghalamestani, K.A. Dick, H.Q. Xu, Schottky barrier and contact resistance of InSb nanowire field-effect transistors, Nanotechnology 27 (27) (2016) 275204, https://doi.org/10.1088/0957-4484/27/27/275204.
[49] Y. Wang, S. Liu, Q. Li, R. Quhe, C. Yang, Y. Guo, X. Zhang, Y. Pan, J. Li, H. Zhang, L. Xu, B. Shi, H. Tang, Y. Li, J. Yang, Z. Zhang, L. Xiao, F. Pan, J. Lu, Schottky barrier heights in two-dimensional field-effect transistors: from theory to experiment, Rep. Prog. Phys. 84 (5) (2021) 056501, https://doi.org/10.1088/1361-6633/abf1d4.
[50] H. Oh, J.-J. Kim, J.-O. Lee, S. Kim, Temperature dependent intrinsic carrier mobility and carrier concentration in individual ZnO nanowire with metal contacts, J. Kor. Phys. Soc. 58 (2) (2011) 291–296, https://doi.org/10.3938/jkps.58.291.
[51] D.B. Suyatin, V. Jain, V.A. Nebol'sin, J. Trägårdh, M.E. Messing, J.B. Wagner, O. Persson, R. Timm, A. Mikkelsen, I. Maximov, L. Samuelson, H. Pettersson, Strong Schottky barrier reduction at Au-Catalyst/GaAs-Nanowire interfaces by electric dipole formation and fermi-level unpinning, Nat. Commun. 5 (1) (2014) 3221, https://doi.org/10.1038/ncomms4221.
[52] A. Razavieh, P.K. Mohseni, K. Jung, S. Mehrotra, S. Das, S. Suslov, X. Li, G. Klimeck, D.B. Janes, J. Appenzeller, Effect of diameter variation on electrical characteristics of Schottky barrier indium arsenide nanowire field-effect transistors, ACS Nano 8 (6) (2014) 6281–6287, https://doi.org/10.1021/nn5017567.
[53] Byung-Gook Park; Sung Woo Hwang; Young June Park. Nanoelectronic Devices..
[54] F. Giubileo, L. Iemmo, M. Passacantando, F. Urban, G. Luongo, L. Sun, G. Amato, E. Enrico, A. Di Bartolomeo, Effect of electron irradiation on the transport and field emission properties of few-layer MoS_2 field-effect transistors, J. Phys. Chem. C 123 (2) (2019) 1454–1461, https://doi.org/10.1021/acs.jpcc.8b09089.
[55] S. Kim, J. Kim, D. Jang, R. Ritzenthaler, B. Parvais, J. Mitard, H. Mertens, T. Chiarella, N. Horiguchi, J.W. Lee, Comparison of temperature dependent carrier transport in FinFET and gate-all-around nanowire FET, Appl. Sci. 10 (8) (2020) 2979, https://doi.org/10.3390/app10082979.
[56] A. Grillo, E. Faella, A. Pelella, F. Giubileo, L. Ansari, F. Gity, P.K. Hurley, N. McEvoy, A. Di Bartolomeo, Coexistence of negative and positive photoconductivity in few-layer $PtSe_2$ field-effect transistors, Adv. Funct. Mater. 31 (43) (2021) 2105722, https://doi.org/10.1002/adfm.202105722.
[57] S.A. Dayeh, Electron transport in indium arsenide nanowires, Semicond. Sci. Technol. 25 (2) (2010) 024004, https://doi.org/10.1088/0268-1242/25/2/024004.
[58] J. Sun, M. Passacantando, M. Palummo, M. Nardone, K. Kaasbjerg, A. Grillo, A. Di Bartolomeo, J.M. Caridad, L. Camilli, Impact of impurities on the electrical conduction of anisotropic two-dimensional materials, Phys. Rev. Appl. 13 (4) (2020) 044063, https://doi.org/10.1103/PhysRevApplied.13.044063.
[59] Y. He, Z. Huang, M. Zhang, M. Wu, M. Mi, C. Wang, L. Yang, C. Zhang, L. Guo, X. Ma, Y. Hao, Temperature-dependent characteristics of AlGaN/GaN nanowire channel high electron mobility transistors, Phys. Status Solidi 216 (16) (2019) 1900396, https://doi.org/10.1002/pssa.201900396.
[60] A. Kumar, L. Viscardi, E. Faella, F. Giubileo, K. Intonti, A. Pelella, S. Sleziona, O. Kharsah, M. Schleberger, A. Di Bartolomeo, Temperature dependent black phosphorus transistor and memory, Nano Ex 4 (1) (2023) 014001, https://doi.org/10.1088/2632-959X/acbe11.
[61] K.E. Moselund, M. Najmzadeh, P. Dobrosz, S.H. Olsen, D. Bouvet, L. De Michielis, V. Pott, A.M. Ionescu, The high-mobility bended n-channel silicon nanowire transistor, IEEE Trans. Electron. Dev. 57 (4) (2010) 866–876, https://doi.org/10.1109/TED.2010.2040939.
[62] B. Van Zeghbroeck. Principles of Semiconductor Devices.
[63] F. Zhou, A.L. Moore, J. Bolinsson, A. Persson, L. Fröberg, M.T. Pettes, H. Kong, L. Rabenberg, P. Caroff, D.A. Stewart, N. Mingo, K.A. Dick, L. Samuelson, H. Linke, L. Shi, Thermal conductivity of indium arsenide nanowires with wurtzite and zinc blende phases, Phys. Rev. B 83 (20) (2011) 205416, https://doi.org/10.1103/PhysRevB.83.205416.
[64] W. Bae, CMOS inverter as analog circuit: an overview, JLPEA 9 (3) (2019) 26, https://doi.org/10.3390/jlpea9030026.
[65] Yuan Taur; Tak H. Ning. Fundamentals of Modern VLSI Devices.
[66] Behzad Razavi. Fundamentals of Microelectronics.
[67] Angelo Geraci. Principles of Electronics of Digital Systems.
[68] A.W. Dey, J. Svensson, B.M. Borg, M. Ek, L.-E. Wernersson, Single InAs/GaSb nanowire low-power CMOS inverter, Nano Lett. 12 (11) (2012) 5593–5597, https://doi.org/10.1021/nl302658y.
[69] J. Wang, X. Guo, Z. Yu, Z. Ma, Y. Liu, Z. Lin, M. Chan, Y. Zhu, X. Wang, Y. Chai, Low-power complementary inverter with negative capacitance 2D semiconductor transistors, Adv. Funct. Mater. 30 (46) (2020) 2003859, https://doi.org/10.1002/adfm.202003859.
[70] H. Wang, L. Yu, Y.-H. Lee, Y. Shi, A. Hsu, M.L. Chin, L.-J. Li, M. Dubey, J. Kong, T. Palacios, Integrated circuits based on bilayer MoS_2 transistors, Nano Lett. 12 (9) (2012) 4674–4680, https://doi.org/10.1021/nl302015v.
[71] M. Sil, A. Mallik, On the logic performance of bulk junctionless FinFETs, Analog Integr. Circuits Signal Process. 106 (2) (2021) 467–472, https://doi.org/10.1007/s10470-020-01782-y.
[72] J. Huang, S. Somu, A. Busnaina, A molybdenum disulfide/carbon nanotube heterogeneous complementary inverter, Nanotechnology 23 (33) (2012) 335203, https://doi.org/10.1088/0957-4484/23/33/335203.
[73] Y. Hashim, O. Sidek, Optimization of nanowire-resistance load logic inverter, J. Nanosci. Nanotechnol. 15 (9) (2015) 6840–6842, https://doi.org/10.1166/jnn.2015.10342.
[74] Y. Su, C.U. Kshirsagar, M.C. Robbins, N. Haratipour, S.J. Koester, Symmetric complementary logic inverter using integrated black phosphorus and MoS_2 transistors, 2D Mater. 3 (1) (2016) 011006, https://doi.org/10.1088/2053-1583/3/1/011006.
[75] Y. Liu, K.-W. Ang, Monolithically integrated flexible black phosphorus complementary inverter circuits, ACS Nano 11 (7) (2017) 7416–7423, https://doi.org/10.1021/acsnano.7b03703.
[76] B. Radisavljevic, M.B. Whitwick, A. Kis, Integrated circuits and logic operations based on single-layer MoS_2, ACS Nano 5 (12) (2011) 9934–9938, https://doi.org/10.1021/nn203715c.
[77] E. Liu, Y. Fu, Y. Wang, Y. Feng, H. Liu, X. Wan, W. Zhou, B. Wang, L. Shao, C.-H. Ho, Y.-S. Huang, Z. Cao, L. Wang, A. Li, J. Zeng, F. Song, X. Wang, Y. Shi, H. Yuan, H.Y. Hwang, Y. Cui, F. Miao, D. Xing, Integrated digital inverters based on two-dimensional anisotropic ReS2 field-effect transistors, Nat. Commun. 6 (1) (2015) 6991, https://doi.org/10.1038/ncomms7991.