Analysis of CNTFETs Operating in SubThreshold Region for Low Power Digital Applications

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The aim of this paper is to characterize and to model the behaviour of Carbon NanoTube Field Effect Transistors (CNTFETs) operating in sub-threshold region for low power applications. In particular we refer to Schottky Barrier (SB) CNTFETs, because these devices have a better performance when they operate in sub-threshold region. In this way it is possible to evaluate the noise margin and output voltage swing, necessary to digital circuits design.

Introduction

Carbon Nanotube Field Effect Transistors (CNTFETs) are novel devices that are expected to sustain the transistor scalability while increasing its performance. One of the major differences between CNTFETs and MOSFETs is that the channel of the devices is formed by Carbon NanoTubes (CNTs) instead of **semiconductor**, which enables a higher drive current density, due to the larger current carrier mobility in CNTs compared to bulk silicon (1). In particular, with CNTs we obtain good operation even at very high frequencies (2-7) **of about THz**.

The portable electronics industry, expanded intensely in the recent years, requires voltage supply scaling, so that the supply voltage is lower than the threshold voltage of a transistor **(0.4–0.6 V)**. For these low power applications, such as hearing aids, trade performance for power savings, the transistor must operate in subthreshold regime.

An important metric in subthreshold design is the ratio of on-to off-current (*Ion/Ioff*). This ratio characterizes the difference in current between a closed and open switch.

The on-current in MOSFETs decreases exponentially as the supply voltage is lowered. The same happens in carbon nanotube transistors **(2)**. However, compared to MOSFETs, the off-current in CNTFETs continues to decrease as the voltage across the FET from drain to source decreases **(1-5)**.

Carbon nanotubes have a varying *Ion/Ioff* ratio, depending on the nanotube structure and properties (1-3). These very high current values in CNTs are due to their ballistic transport and their limited electron and hole scattering. Therefore, CNTs have the ability to increase performance while adhering to lower power requirements in subthreshold circuits.

There are two main types of carbon nanotube FETs differing by their current injection methods: Schottky barrier FETs (8-10), and doped CNTFETs (11).

In this paper we refer to Schottky Barrier carbon nanotube FETs (SB-CNTFETs), because these devices **have better performance when they operate in sub-threshold regime (8-10).**

The presentation of the paper is organized as follows. At first we examine the operation of SB-CNTFETs. A description of CAD tool to reproduce the I-V characteristics of the device, operating in sub-threshold region, is presented and the study of a digital NOT gate with **complementary technology given**, together with the discussion of relative results, conclusions and future developments.

CNTFETs: Schottky Barrier carbon nanotube FETs

A straightforward application of the semiconducting property of CNTs is to form a field-effect transistor (FET) analogous to the MOSFET (1).
There are two main types of carbon nanotube FETs differing by their current injection methods: Schottky barrier FETs (8-10), and doped CNTFETs (11).
In this paper we refer to Schottky Barrier carbon nanotube FETs (SB-CNTFETs), because these devices, as we have already written, seem to have better performance when they operate in subthreshold regime **(8-10)**.
To understand the operation of a Schottky Barrier CNTFET (SB-CNTFET), it is necessary to examine the energy band diagram for the structure. At the intersection between the metal contacts and the semiconducting carbon nanotube, Schottky barriers are created (1).
The current in CNTFETs is from the tunneling of carriers through the Schottky barriers. The type of metal for the contacts is chosen so that its work function forces the metal Fermi level to lie between the valance and conduction band of the CNT (1). For short channels, the CNT channel can become ballistic and hence, the metal contact resistance and the Schottky barriers at the source and drain ends limit the current drive through the nanotube. Thus, a low contact resistance, such as that of Titanium, is desirable. Presently, the control of the metal contacts to carbon nanotubes is not consistent and the tunneling current levels between transistors can vary greatly **(1) (8-10)**.
When a negative voltage is applied between the drain and source, the band structure, of the CNT, is modulated to account for the drain to source voltage (Vds).
When a small negative gate to source voltage is applied **(-0.4 -0.05 V)**, CNTFET is in the subthreshold condition.
With a negative gate voltage applied, the Schottky barrier width at the source is modulated, allowing for holes or electrons to tunnel through the valence band and pass to the drain. The thickness of the source Schottky barrier at the metal Fermi level decreases exponentially with an increasing gate to source voltage. Thus, the tunnel current through the Schottky barrier increases exponentially, inversely to the barrier thickness.
Moreover Id-Vgs characteristic does not differ greatly changing Vds because the drain voltage does not significantly control the source Schottky barrier.
It is easy to see in (8) that the subthreshold characteristics do not vary largely with Vds and the subthreshold slope remains relatively constant **with changing temperature**.
The transistor threshold voltage, where the device acts similarly to an *on* MOSFET, is reached when the metal source Fermi level is approximately even with the valence or conduction band of the CNT, in a p-channel or n-channel respectively. **In the simulations proposed in this paper we have considered both p-channel and n-channel devices**.
If the gate voltage continues to increase above this threshold, the Schottky barrier thickness at the source will remain constant and the current will not continue to increase exponentially. Above the threshold voltage, the current will only increase linearly with Vds.

Above the CNTFET threshold voltage, the I-V characteristics are very similar to a MOSFET ones: the current increases linearly with Vds; and, when the barrier at the drain is completely eliminated, the FET current saturates.
The Id-Vds characteristics for a saturated SB-CNTFETs have a very little slope, unlike short channel MOSFETs.

Characteristics modeling of subthreshold CNTFETs

The total current in a CNTFET, as described previously, depends on the tunnelling current both of the holes and of the electrons through the source and drain Schottky barriers: the current in a SB-CNTFET exponentially increases, reducing the thickness of the Schottky barrier at source, with also an increase of the subthreshold current.
In comparison with MOSFETs, in CNTFETs we have not the minimum current for Vgs = 0 V, but to Vgs = Vds/2. This is true for all SB-CNTFETs having the same metal used for the gate, drain and source **(3) (8-10)**. This minimum condition (Vgs = Vds/2) is independent on metal work function **(8-10)**.
In order to model the Id-Vgs characteristics, we have implemented a Matlab code, characterized by a minimum current at Vds/2, threshold voltage and exponential subthreshold current.
In particular the following equations, proposed in (16), allow to value the current for a n-channel transistor (for a p-channel transistor we have the same expressions with negative voltages values):

$$V_{th} = c * \left(\frac{D_t}{2} \right) + d \qquad [1]$$

$$V_{min} = \frac{Vds}{2} \qquad [2]$$

$$I_{Dm0} = 6.96 * 10^{-20} * e^{(9.17 \cdot D_t)} \qquad [3]$$

$$I_{D\,min} = I_{Dm0} * e^{(h_n |Vds|)} \qquad [4]$$

$$I_{Dnchannel} = I_{D\,min} * e^{(a_n |Vgs - V_{min}|)} \qquad [5]$$

where c is equal to - $0.125 \cdot 10^{-9}$ V/m, d is equal to 0.6625 V and h_n is a constant depending on the process variations. Moreover a_n is a fitting parameter, dependent on gate oxide thickness (t_{ox}) and on CNT diameter (D_t). **We used for previous parameters the same values of (16), in order to have comparable results with those reported in (16).**
In the proposed model we have assumed $E_{Fermi} = E_{CNTmidband_gap}$. **In this way the p-channel current characteristics are equal to the n-channel I-V data.**
The obtained Id-Vgs characteristics, for a n-channel and a p-channel CNTFETs, are shown in **Fig. 1** (where D_t = 1.3 nm and h_n =16.1 $V^{-1}s$) and in **Fig. 2** (D_t = 2.5 nm and h_n = 14.1 $V^{-1}s$) respectively.

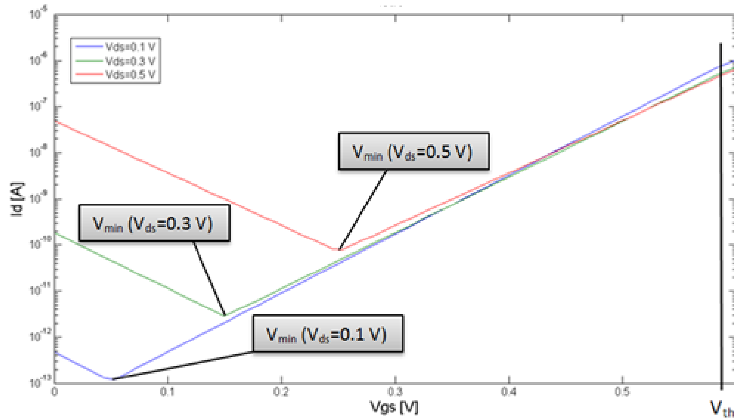

Figure 1. Simulated Id-Vgs characteristics of a n-channel SB-CNTFET.

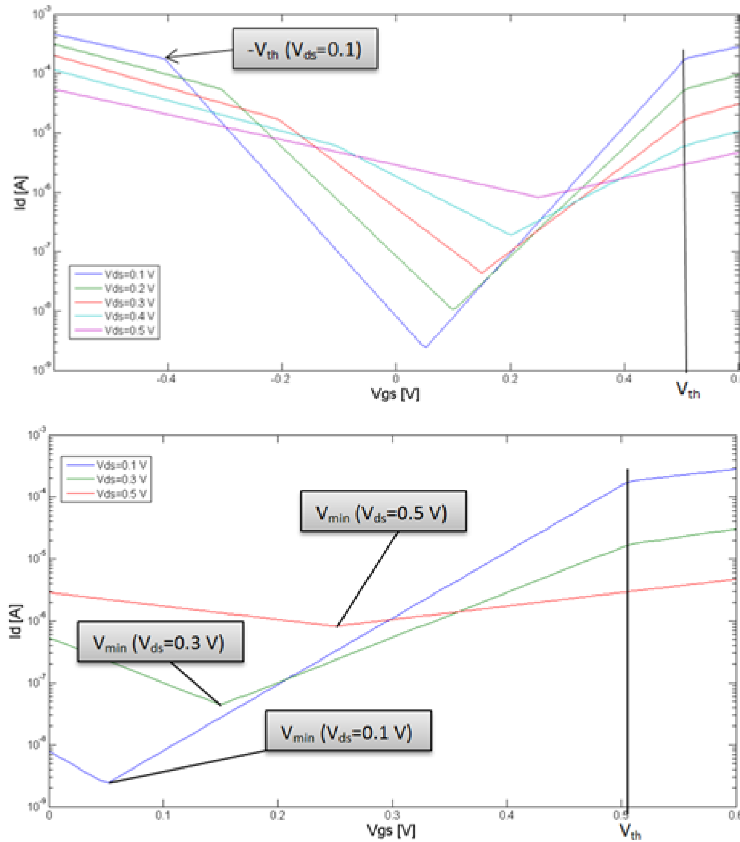

Figure 2. Simulated Id-Vgs characteristics of a p-channel SB-CNTFET.

From these figures we can evaluate the numerical values of V_{min}, I_{Dmin} and V_{th}. In fact the CNTFET subthreshold regime is verified between the two threshold voltage (V_{th}) points. These points have the same distance from the minimum voltage.
The distance from the minimum to the threshold is ΔV_{SUB} (Vds) = V_{th} - V_{min}.
In order to compare the experimental results with our simulated ones, in Table I we have reported the numerical values of V_{min}, I_{Dmin} and V_{th}, obtained in (8), and those obtained

by us, for a SB-CNTFETs, denoted as Device A, which has a diameter equal to 1.3 nm, having assumed a value of h_n equal to 16.1 V^{-1}.

TABLE I. Numerical values of V_{min}, I_{Dmin} and V_{th}, obtained in (8) (bold) and those obtained by us, for device A.

V_{ds}(V)	V_{min}(V)	I_{Dmin}(pA)	V_{th} (V)
0.1	**0.05**	**0.119**	**0.58**
	0.05	0.111	0.60
0.3	**0.15**	**2.83**	**0.58**
	0.15	3.73	0.60
0.5	**0.25**	**77.10**	**0.58**
	0.25	72.20	0.60

Similarly, in Table II we have reported the numerical values of V_{min}, I_{Dmin} and V_{th}, obtained in (8), and those obtained by us, for a SB-CNTFETs, denoted as Device B, which has a diameter equal to 2.5 nm, having assumed a value of h_n equal to 14.6 V^{-1}.

Table II. Numerical values of V_{min}, I_{Dmin} and V_{th}, obtained in [8] (bold) and those obtained by us, for device B.

V_{ds}(V)	V_{min}(V)	I_{Dmin}(pA)	V_{th} (V)
0.1	**0.05**	**2.34**	**0.50**
	0.05	2.03	0.45
0.3	**0.15**	**43.80**	**0.50**
	0.15	64.20	0.45
0.5	**0.25**	**819.0**	**0.50**
	0.25	702.0	0.55

The analysis of the previous Tables allows us to say that there is a good agreement between the experimental and simulated Id-Vgs characteristics, with a negligible relative error, and this supports the validity of our approach. Moreover, the computation is instantly, or with processing times too short to be evaluated**.** To perform all the simulations we have used a common Windows-based PC, equipped with a Pentium IV CPU and main memory of 1 Gbyte.

A design example: SB-CNTFETs inverter

We have considered a typical NOT gates, shown in **Fig. 3**, employing the same architectures used in standard CMOS technology. **Fig. 4** shows the voltage-transfer characteristic (VTC) of a NOT gate, in which we have highlighted three separate regions: low input, region of transition and high input.

In low power digital applications it is necessary to evaluate the differences (V_{OH_MIN} - V_{IL_MIN}) and ($V_{IL_MAX} – V_{OL\ MAX}$), as shown in **Fig. 4**, which are respectively the noise margin to the logical level 1 (NM_H) and the noise margin to the logical level 0 (NM_L). The noise margin NM is defined as the least among the two values of NM_H and of NM_L.

In order to maximize NM, it would be desirable $V_{IL_Max} = V_{IH_MIN}$. Moreover to maximize contemporary both the noise margins, we need to assume them equal to half of the maximum supply voltage **(1) (16)**.

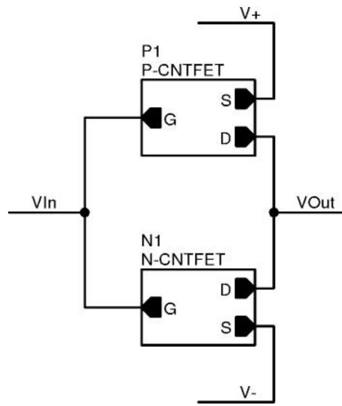

Figure 3. NOT gate with complementary CNTFET technology.

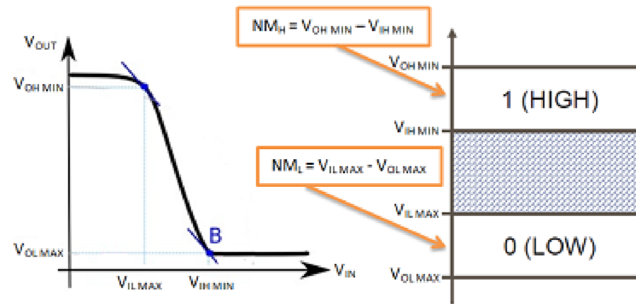

Figure 4. Transfer function of NOT gate.

Moreover VTC depends on CNT diameter. In fact, the *Ioff* current of a n-FET, with diameter ≥ 2 nm, is greater than the *Ion* of a p-FET, and therefore, increasing the diameter, the Vout voltage value, for which the gate assumes logical value 1, will slightly decrease **(1)** **(8-10)**.
For smaller diameters we have an opposite effect. Nevertheless the *Ion/Ioff* ratio is enough high and the increase of *Ioff* does not substantially change the VTC.
We have calculated the maximum Voltage Swing for which the logical values are 1 (high) and 0 (low), for supply voltage $V_+ = V_{DD}$ equal to 0.4 V versus the CNT diameter. The results obtained allow us to affirm that, for diameters greater than 2 nm and supply voltage equal to 0.6 V, the voltage swing decreases.
Intersecting the previous simulated d Id-Vds characteristics of the p-FET with those of the n-FET for a same value of Vin, we may easily obtain the VTC.
In Table III we have reported the calculated NM values of CNTFET inverter, for a supply voltage V_{DD} equal to 0.4 V and for different CNT diameters. In bold we have indicated the values of noise margins obtained in (8-9).

Table III. Noise margin of CNTFET inverter.

D_t (nm)	NM_h	NM_l	NM
1.3	**0.17** 0.17	**0.18** 0.17	**0.17** 0.17
1.9	**0.17** 0.14	**0.18** 0.14	**0.17** 0.14
2.5	**0.16** 0.09	**0.17** 0.09	**0.17** 0.09

We have repeated the same calculations for a supply voltage V_{DD} equal to 0.6 V, obtaining also in this case that, with regards to noise margin, the optimal condition is obtained for a CNT having a diameter equal to 1.3 nm.
Instead, for CNT diameters of 1.9 nm and 2.5 nm, the noise margin reduces because the I-V characteristics are not monotonous. In this case it is convenient to take the points where the voltage V_{OUT} worsens, that to say where $V_{IN} = 0$ or $V_{IN} = V_{DD}$.

Conclusions and future developments

In this paper we have proposed a procedure to model the current in SB-CNTFETs, operating in the low voltage subthreshold condition, in order to determine the functionality of future sub-threshold CNTFETs in digital design. In this way, through a design example of a SB-CNTFET inverter, it has been possible to evaluate the noise margin and output voltage swing to determine the optimal working condition and the optimal CNTFET technological characteristics.
Actually we are working to compare our results with those obtained in (17), using the Stanford-Source Virtual Carbon Nanotube Field-Effect Transistor model (VS-CNFET) of Stanford University (18-19).

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