

**Temperature and time dependent electron trapping in Al<sub>2</sub>O<sub>3</sub> thin films onto AlGaN/GaN heterostructures**

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**Abstract**

In this article, the charge trapping phenomena in Al<sub>2</sub>O<sub>3</sub> thin films grown by atomic layer deposition (ALD) on AlGaN/GaN heterostructures have been studied by time-dependent capacitance-voltage (C-V) measurements as a function of temperature. In particular, monitoring the transient of the capacitance enabled us to estimate the maximum depth of the insulating layer interested by the negative charge trapping effect under our bias stress conditions and to determine a charge traps density in the bulk Al<sub>2</sub>O<sub>3</sub> in the order of  $3 \times 10^{19} \text{ cm}^{-3}$ . A temperature dependent C-V analysis up to 150°C demonstrated the presence of two competitive mechanisms that rule the electron capture and emission in the Al<sub>2</sub>O<sub>3</sub> film, characterized by activations energies of 22 and 88 meV respectively. Photoluminescence analyses revealed the presence of oxygen-related point defects in the insulator with a concentration in the order of  $\sim 10^{20} \text{ cm}^{-3}$  envisaging that only a fraction of them is electrically active. The results are useful to establish the thermal stability of the trapping phenomena, and the possible application in real devices.

**Keywords:** Al<sub>2</sub>O<sub>3</sub>, Gallium Nitride, Plasma Enhanced Atomic Layer Deposition, charge trapping, capacitance transient measurements

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## INTRODUCTION

Aluminum oxide ( $\text{Al}_2\text{O}_3$ ) is theoretically one of the most attracting insulating materials for a variety of applications in electronic devices [1]. In particular, thin  $\text{Al}_2\text{O}_3$  layers can be used as gate insulator to reduce the leakage current in gallium nitride (GaN) high electron mobility transistors (HEMTs), and/or as passivation layer to reduce the current collapse phenomena [2,3]. The great interest towards  $\text{Al}_2\text{O}_3$  thin films in GaN technology arises from its relevant electronic properties, e.g. the high relative dielectric permittivity  $\kappa$  ( $\sim 9$ ), the high critical electric field (10 MV/cm), the large band gap ( $\sim 8.9$ ) and the favorable band alignment with GaN [4].

Atomic Layer Deposition (ALD), either in thermal or plasma-enhanced mode, is certainly the most widely used technique to deposit  $\text{Al}_2\text{O}_3$  thin films on GaN-based heterostructures [5]. In fact, ALD allows an accurate control of the deposition parameters inducing a self-limited growth mechanism, the control of film thickness and interface abruptness, and an uniform coverage at low deposition temperature, i.e. compatible with GaN thermal stability range and typical device processing temperatures [4]. However, the amorphous films grown by ALD are often characterized by the occurrence of negative charge trapping effects, especially when subjected to current or bias stress [6,7]. In particular, it is continuously debated that  $\text{Al}_2\text{O}_3$  layers suffer by the presence of native defects [8,9,10] that influence the electrical behavior (i.e. leakage current) by introducing electronic levels in the band gap [11,12].

While the majority of the literature on GaN-based devices has been focused on the electrical properties of thermal ALD  $\text{Al}_2\text{O}_3$  films [2,3,4,13,14,15], plasma-enhanced atomic layer deposition (PE-ALD) has been less explored in spite of its potential benefits with respect to the standard thermal ALD approach, e.g. the possibility to achieve a high growth rate and an improved film density at low deposition temperature [16,17]. However, independently of the deposition method, the mechanisms ruling the charge trapping in the bulk ALD  $\text{Al}_2\text{O}_3$  films grown on GaN-based heterostructures have not been yet clarified [18,19]. In this context, some works have been devoted

to the theoretical comprehension of the impact of distributed bulk traps in ALD Al<sub>2</sub>O<sub>3</sub> films on semiconductor compounds such as InGaAs [20], GaN [21] and AlGaN [22,23] on the threshold voltage stability of transistors. However, an experimental method to determine the amount of these traps in the insulator layer volume is missing. Furthermore, the knowledge of the charge/discharge phenomena occurring in bulk traps in ALD Al<sub>2</sub>O<sub>3</sub> films is required to ultimately understand the possible impact on the power electronics device fabrication.

In the present paper, electron trapping/detrapping phenomena in bulk Al<sub>2</sub>O<sub>3</sub> thin films deposited by PE-ALD on AlGaN/GaN heterostructures have been investigated by means of transient capacitance measurements and cyclic gate bias stress acquired at different temperatures. In particular, the temperature dependent cyclic gate bias stress allowed to determine the residual amount of charged bulk traps, while transient capacitance measurements allowed to estimate the maximum distance from the Al<sub>2</sub>O<sub>3</sub>/AlGaN interface of the bulk traps stimulated under our bias stress conditions. Insights on the optical emission properties of these bulk traps have been investigated also by means of photoluminescence measurements. Moreover, the stability of the enhancement mode operation in AlGaN/GaN MISHEMTs has been discussed in terms of the thermal emission of the bulk traps in Al<sub>2</sub>O<sub>3</sub>.

## EXPERIMENTAL

The AlGaN/GaN heterostructures used in this study were grown on Si (111) substrates. The thickness of the AlGaN barrier layer was 16 nm, while the Aluminum concentration was 26% [19].

Al<sub>2</sub>O<sub>3</sub>/AlGaN/GaN circular MIS-capacitor and MISHEMTs were fabricated to monitor the electrical quality of the bulk oxide and of the interface, using the following procedure. First, the AlGaN surface has been cleaned using piranha (H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>SO<sub>4</sub> =1:5) and diluted hydrofluoric acid (H<sub>2</sub>O:HF=10:1) solutions, for 10 and 5 minutes, respectively [24,25]. Then the Ohmic contacts have been formed by a Ti/Al/Ni/Au multilayer annealed at 850°C [26]. Afterward, a 30nm thick

$\text{Al}_2\text{O}_3$  film has been deposited at  $250^\circ\text{C}$  using a PE-ALD LL reactor from SENTECH Instruments GmbH. Trimethyl-aluminum (TMA) and  $\text{O}_2$ -plasma were used as aluminum and oxygen sources, respectively. For the plasma-enhanced ALD mode, a 100 sccm  $\text{O}_2$  flow was released to plasma source, while nitrogen ( $\text{N}_2$ ), with a flow rate of 40 sccm, has been used as carrier gas for TMA precursor. The pressure was 20 Pa during deposition. Finally, a gate contact consisting of a Ni/Au bilayer was defined by photolithography and lift-off [27]. The MISHEMT dimensions are gate-width of  $200\ \mu\text{m}$  and gate-length of  $14\ \mu\text{m}$ .

Time resolved photoluminescence (PL) spectra were excited by 5.85 eV-laser radiation generated in a pulsed tunable laser system (VIBRANT OPOTEK), pulse width  $\approx 5\ \text{ns}$ , repetition rate 10 Hz. The sample was excited by a laser beam, spot size of 3 mm, in  $45^\circ$  front-scattering geometry; the fluence/pulse, monitored with a pyroelectric detector, was fixed at  $1\ \text{mJ}/\text{cm}^2$ . The emitted light was spectrally resolved by a monochromator equipped with a 150 grooves/mm grating blazed at 300 nm, and then acquired by an intensified charge coupled device camera (PIMAX Princeton Instruments), setting the acquisition time window,  $T_W$ , and the delay,  $T_D$ , with respect to the arrival of excitation laser pulses. All the emission spectra were detected with a bandwidth of 3 nm and corrected for the instrumental response.

The test devices characterized by low frequency (1 kHz) capacitance-voltage (C-V) and current-voltage (I-V) measurements under different bias stress conditions. The C-V and I-V measurements on capacitors and transistors were carried out using a Microtech Cascade probe station equipped with a Keysight B1505 parameter analyzer varying the temperature between 25 and  $150\ ^\circ\text{C}$ . Atomic force microscopy (AFM) was carried out to investigate the surface morphology of the samples during the fabrication steps, using a Veeco Dimension 3100 AFM with a NanoScope V controller. Transmission electron microscopy (HR-TEM) on cross-section samples enabled us to monitor the structural quality of the  $\text{Al}_2\text{O}_3/\text{AlGaIn}$  interface.

## RESULTS AND DISCUSSION

### *Morphological, structural and chemical properties*

The investigation started from the morphological, structural and chemical points of view. Figs. 1a and 1b show the AFM morphology collected on the AlGaN/GaN and Al<sub>2</sub>O<sub>3</sub>/AlGaN/GaN surfaces, respectively. The heights distribution collected on the scanned area can be visualized as shown in Fig. 1c. Fig. 1c shows also the comparison between the heights distribution collected both on the Al<sub>2</sub>O<sub>3</sub> and on the AlGaN/GaN substrate bare surfaces. As can be seen, very smooth surface of the deposited Al<sub>2</sub>O<sub>3</sub> film is achieved. Furthermore, Figs. 1d and 1e report the cross-sectional TEM micrographs showing the abrupt Al<sub>2</sub>O<sub>3</sub>/AlGaN interface between the amorphous insulator and the crystalline semiconductor substrate.

Often, the Al<sub>2</sub>O<sub>3</sub>/AlGaN/GaN system is used to fabricate MISHEMTs with a tunable threshold voltage ( $V_{th}$ ). In fact, MISHEMTs having a  $V_{th} < 0$  V due to the active presence of a 2DEG in the gate region – namely called “normally- on” transistors – can become “normally-off” after the suppression of the 2DEG in the gate region by an appropriate positive gate bias stress procedure [7]. In particular, electrons trapped in the gate region produce an electrostatic repulsion on the 2DEG inhibiting the conduction between source and drain.

*Johnson et al.* [28] and *Hou et al.* [29] observed an analogous trapping effect in HfO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> AlGaN/GaN MISHEMTs and attributed it to the presence of a GaON interfacial layer formed during the thermal ALD process. However, our TEM analyses did not reveal the presence of such interfacial layer.

On the other hand, a chemical analysis based on electron energy-loss spectroscopy performed on amorphous Al<sub>2</sub>O<sub>3</sub> films grown under the same conditions showed the presence of low coordinated Al cations in the layers, which is an indication of oxygen vacancies [7]. However, a

clear identification of the electrically active defects in the amorphous  $\text{Al}_2\text{O}_3$  film is not yet provided.

Figs. 2a and 2b report the PL spectra in the 2.0-4.0 eV range of the AlGaN/GaN and  $\text{Al}_2\text{O}_3/\text{AlGaN}/\text{GaN}$  samples, respectively, acquired under excitation at 5.85 eV with  $T_w=10$  ns and  $T_D=6$  ns. While in the UV region both samples emit a peak centered around 3.4 eV, well associated with the GaN band gap transition [30], different features are observed in the visible. Indeed, the  $\text{Al}_2\text{O}_3/\text{AlGaN}/\text{GaN}$  exhibits a band peaked at 2.9 eV with full width half maximum (FWHM)  $\approx 0.5$  eV (Fig. 2b), that decays in few ns. This emission certainly originates from point defects in the  $\text{Al}_2\text{O}_3$  layer, their concentration can be roughly estimate of the order of  $\sim 10^{20} \text{ cm}^{-3}$  by comparing the PL amplitude with that measured in a reference sample containing a known concentration of luminescent defects, nonbridging oxygen hole centers in irradiated silica [31], normalizing appropriately for the excited volume. It is worth noting that in earlier works [9], Perevalov et al. recorded a PL band at 2.9 eV in amorphous  $\text{Al}_2\text{O}_3$  films,  $\sim 20$  nm thick, with excitation and decay characteristics similar to those observed in the present work. Those authors associated this emission with oxygen vacancies and measured a concentration of  $N \approx 7 \times 10^{20} \text{ cm}^{-3}$ .

### *Electrical properties*

The electrical characterization is carried out in order to fully investigate the effects of temperature and time on the charge trapping effects in  $\text{Al}_2\text{O}_3/\text{AlGaN}/\text{GaN}$  system. In particular, the electrical characterization of the  $\text{Al}_2\text{O}_3/\text{AlGaN}$  system started with a method to separate the trapping phenomena both at the interface and inside the insulating layer.

Firstly, the trapping phenomena have been investigated on  $\text{Al}_2\text{O}_3/\text{AlGaN}/\text{GaN}$  MIS capacitors, by the C-V measurements, reported in Fig. 3 at different temperatures (25 °C (a,b,c, and d); 75 °C (3); 125 °C (f)). In particular, C–V curves have been collected by increasing the final positive gate bias stress from 0 V up to + 14 V with + 2 V steps.

To avoid an underestimation of the trapping phenomena, as may occur in AlGaIn/GaN MISHEMTs probed by high-frequency C-V measurements [32,33], our C-V measurements have been carried out at 1kHz

In the C-V characterization reported in the following part, the gate bias was swept from negative toward positive values (from depletion to accumulation) and backward from positive toward negative biases (from accumulation to depletion). The cyclic C-V curves have been sequentially collected by increasing the final gate bias value by + 2 V from 0V to +14V on “fresh” (i.e. non-stressed) MIS capacitors. The hysteresis between the forward and backward C-V curves in two different specific regions has been recorded for different gate bias stress conditions. This procedure allowed to discriminate among the different trapping contributions at the Al<sub>2</sub>O<sub>3</sub>/AlGaIn interface and inside the insulator.

The first C-V measurement (Fig. 3a), collected from  $V_G = -10V$  to 0V and backward, shows no hysteresis. This means that the depletion of the two dimensional electron gas (2DEG) at the AlGaIn/GaN interface occurs at the expected “pinch-off” bias value  $V_{PO} = -7.5 V$  [34].

Further cyclic C-V curves acquired by increasing the final positive gate bias stress value by steps of +2 V up to the final value of +14V have been collected (Figs. 3b, 3c, and 3d). During this progressive cyclic gate bias stress procedure, it is possible to monitor both the pinch-off bias  $V_{PO}$  (Fig. 3 a) and the “flat band voltage”  $V_{FB}$  (Fig. 3b), this latter defined as the point of the intersection of the second derivative of the C-V curve with the positive gate bias axis region [35]. In fact, for positive gate bias values, the C-V curves starts exhibiting a second step due to accumulation of electrons in the AlGaIn layer at the Al<sub>2</sub>O<sub>3</sub> interface that can be monitored by the  $V_{FB}$  shifts.

These hystereses can be attributed to different charge trapping phenomena occurring in the MIS system. In particular, the flat band voltage shift  $\Delta V_{FB}$  is associated with the charging of the Al<sub>2</sub>O<sub>3</sub>/AlGaIn interface states. On the other hand, the pinch-off bias shift  $\Delta V_{PO}$  is due to the charge trapping in the bulk Al<sub>2</sub>O<sub>3</sub> film [36]. Similarly, Figs. 3e and 3f show the hysteresis between the forward and backward C-V curves collected at 75 °C and 125 °C, respectively. As discusses later

in the paper, a more detailed analysis of these cyclic C-V curves collected at different temperatures enabled to get determine the temperature-dependent charge trapping behaviour.

An additional analysis of the cyclic C-V curves allowed us to determine the charge traps density and their location inside the insulator.

According to the planar capacitor approximation, the total amount of charge trapped at the Al<sub>2</sub>O<sub>3</sub>/AlGaN interface ( $N_{it}$ ) can be obtained by:

$$N_{it} = \frac{\Delta V_{FB} C_{Al_2O_3}}{q} \quad (1)$$

where  $C_{Al_2O_3}$  is the insulator layer capacitance in accumulation and  $q$  is the electron charge.

In a similar way, the capacitance plateaux  $C_{PO}$  observed close to  $V_G = 0$  V is the series of the insulator ( $C_{Al_2O_3}$ ) and AlGaN layer ( $C_{AlGaN}$ ) capacitances and can be used to extract the total amount of charge trapped at the Al<sub>2</sub>O<sub>3</sub> bulk interface ( $N_{OT}$ ):

$$N_{OT} = \frac{\Delta V_{PO} \left( \frac{t_{Al_2O_3}}{\kappa_{Al_2O_3} \epsilon_0} + \frac{t_{AlGaN}}{\kappa_{AlGaN} \epsilon_0} \right)^{-1}}{q} \quad (2)$$

where  $t_{Al_2O_3}$  and  $t_{AlGaN}$  are the Al<sub>2</sub>O<sub>3</sub> and AlGaN layer thicknesses, while  $\kappa_{Al_2O_3}$  and  $\kappa_{AlGaN}$  are the Al<sub>2</sub>O<sub>3</sub> and AlGaN relative dielectric permittivities.

Fig. 4 reports the  $\Delta V_{FB}$  (a) and  $\Delta V_{PO}$  (b) shifts that are due to the total amount of the trapped charges at the Al<sub>2</sub>O<sub>3</sub>/AlGaN interface ( $N_{it}$ ) and in the bulk Al<sub>2</sub>O<sub>3</sub> ( $N_{OT}$ ), respectively. The values are collected as a function of the positive value of the final gate bias stress, at the different measurement temperatures from 25°C to 150 °C.

The values of the trapped charges have been extracted from the C-V curves from the shifts  $\Delta V_{FB}$  and  $\Delta V_{PO}$ , using Eq. (1) and Eq. (2), respectively. As it can be seen, at all the measurement temperatures the values of  $\Delta V_{FB}$  (red curves in Fig. 5a) after an increase below 6V tend to saturate at high stress bias to a value of interface trapped charge  $N_{it} = 7 \times 10^{12} \text{ cm}^{-2}$  (see Fig. 5a). On the



other hand, the positive  $\Delta V_{PO}$  shift does not show a saturation with increasing the bias stress or a monotonic trend with increasing the temperature (Fig. 4b).

It must be pointed out that an analogous trapping behavior has been observed in  $Al_2O_3$  films deposited on 4H-SiC under similar conditions [37]. This latter allows us to rule out an effect of the GaN buffer, as observed by other authors under reverse bias [38,39].

In order to get further insights on the trapping phenomena and on the stability of the enhancement mode MISHEMT behavior, a temperature dependence of the transfer characteristics after bias stress has been carried out.

Fig. 5a reports a series of sequential transfer characteristics ( $I_D$ - $V_G$ ) of the  $Al_2O_3/AlGaN/GaN$  MISHEMT after a +14 V positive gate bias stress, collected sweeping the gate bias from a large negative bias (i.e.  $V_G = -20$  V) up to a moderate positive gate bias (i.e.  $V_G = +5$  V) at 100 °C following the green arrow direction (Fig. 5a) and at 150°C (Fig. 4b).

The  $V_D = 0.1$  V value has been chosen not only to minimize the self heating effect but also to get information on the turn-on process of the HEMT keeping a low perturbation of the  $Al_2O_3$  traps.

As can be noticed, after the positive gate bias the MISHEMT shows an enhancement-mode behavior, with a positive pinch-off bias  $V_{PO}=+1.5$  V.

Fig. 5c reports the device pinch-off bias  $V_{PO}$  measured during the sequence of several transfer characteristics of the device collected at 100°C between  $V_G = -20$ V to +5V depicted in Fig. 5a. Evidently, the device shows only a small variation of the  $V_{PO}$ , i.e. the enhancement mode operation is preserved. On the other hand, the same sequence at 150°C (Fig. 5b) leads to a more significant variation of the  $V_{PO}$ , which reach the zero ( $V_{PO}=0$ V) after 6 sweeps. An additional increase of the negative bias stress, by means of an increased number of the gate ramps, induced a further shift of  $V_{PO}$  toward negative values, which indicates that the enhanced-mode operation is not anymore stable at 150 °C.

Noteworthy, the  $V_{PO}$  stability depends on the temperature and the reverse biasing that promotes the electron emission from the  $Al_2O_3$  traps. Hence, our results are a “proof of concept” of the possibility to control the electron trapping in a specific region of the device.

In order to estimate the amount of bulk traps per volume unit in the insulator, it is needed the estimation of the insulator volume fraction involved in the mentioned trapping phenomenon under our experimental conditions of bias stress. Hence, it is mandatory to determine the depth of the charged bulk traps from the  $Al_2O_3/AlGaN$  interface. It is believed that the trapping phenomena have a time-dependent behaviour depending on several parameters.

According to *Fujino and Kita* [40], the trapping/detrapping of the near-interface-oxide-traps (NIOTs) in MOS capacitors produces a transient capacitance  $C(t)$  variation. This transient capacitance can be described by the so called “*extended-Debye relaxation model*” [41] instead of a conventional relaxation model with a single time constant using the equation:

$$\Delta C \equiv [C(t) - C_{eq}] \cong |\Delta C_0| \exp \left\{ - \left( \frac{t}{\tau_{eff}} \right)^\beta \right\} \quad (3)$$

where  $C(t)$  is the capacitance at each time,  $C_{eq}$  is the capacitance at the equilibrium (i.e, after 1000s in our case),  $\tau_{eff}$  is the characteristic tunneling time needed for the carrier transport back and forth from the NIOTs,  $\Delta C_0$  is the total change of capacitance caused by the detrapping of NIOTs and the semiconductor and  $0 < \beta < 1$  is a fitting parameter [42]. Indeed, the characteristic tunneling time  $\tau_{eff}$  is related to the spatial location of the NIOTs with respect to the insulator/semiconductor interface.

The charge penetration distance from the semiconductor into the insulator depends on the applied electric field and stress duration time [43]. In fact, it can be assumed that for a single trap energy and uniform spatial distribution of traps in the insulator the tunneling injection from the semiconductor into the insulator is always sharply peaked spatially. Furthermore, this peak moves at a linear-with-log-time rate of about  $2 \text{ \AA}$  per decade of time into the insulator, giving rise to the notion of a tunneling front [43]. Hence, the variation of the gate bias stress condition in the

capacitance transient measurement may help to understand which is the deepest trap reached inside the insulator during the charge injection. In fact, the deepest trap reached inside the insulator during the charge injection is the slowest trap to be stimulated.

The experimental relaxation time can be used to estimate the maximum distance ( $x$ ) from the insulator/semiconductor interface that is interested, in our experimental stress conditions, by the trapping/detrapping phenomenon.

*Paulsen et al.* [44] described the relaxation time  $\tau(x)$  of a  $\delta$ -shaped distribution of traps located at a distance  $x$  from the semiconductor interface using the following equations:

$$\tau(x) = \frac{m_1^* x \left(1 + \frac{1}{2\eta_1 x}\right)}{2\pi\eta_2 \hbar^3 D_{it}} \exp(2\eta_1 x) \quad (4)$$

where

$$\eta_1^2 = \frac{2m_1^*(\phi_B + E_C - E_f)}{\hbar^2} \quad (5)$$

and

$$\eta_2^2 = \frac{2m_2^*(E_C - E_f)}{\hbar^2} \quad (6)$$

where  $\phi_B$  is the energy discontinuity between the semiconductor and the oxide,  $m_1^*$  and  $m_2^*$  are the effective masses for electrons in the oxide and semiconductor respectively, and  $E_f$  is the position of the Fermi level in the semiconductor. Furthermore,  $D_{it}$  is the interface state density close to the AlGaIn conduction band edge,  $\hbar$  is the reduced Plank constant. Considering that the transient characterization is carried out in strong accumulation, the  $E_f$  position can be considered as the energy position of the trap level inside the insulator. The transient is collected in strong accumulation,  $E_f$  position coincides with the AlGaIn conduction band edge and it gives information on the energetic location of the  $\text{Al}_2\text{O}_3$  traps within its band gap.

Fig. 6a shows the experimental transient capacitance  $\Delta C/\Delta C_0$  collected at room temperature used to be fitted using Eq. 3 to extract the effective relaxation time  $\tau_{\text{eff}} \approx 28$  s. Furthermore, Fig. 6a shows that increasing the gate bias stress condition (i.e. from  $V_G = + 7.5$  V up to  $V_G = + 10$  V) the

effective relaxation time is not varied demonstrating that the injected charge cannot reach any physical position inside the insulating layer. The inset of Fig. 6a shows the exponential decay of the capacitance in good agreement to Eq. 3

Eq. 4 is solved considering the literature values of  $m_1^*$  and  $m_2^*$  [45,46] as a function of the distance  $x$  between the deepest bulk trap and the  $\text{Al}_2\text{O}_3/\text{AlGaIn}$  interface, as shown in Fig. 6b. To solve Eq. 4 realistic  $D_{it}$  values are used ranging between  $10^{12}$  up to  $10^{14}$   $\text{cm}^2\text{eV}^{-1}$ . However, this produces an extrapolation error of a less than one Ångström around the mean value of 1.5 nm (see Fig. 6b). The depth of 1.5 nm can be considered as the location of the deepest trap in the insulator determining the transient capacitance behavior observed under our stress conditions. While *Matys et al.* [22] reported about a simulated spatial extension of traps into the dielectric bulk about 4 nm from the insulator/semiconductor interface in ALD  $\text{Al}_2\text{O}_3/\text{AlGaIn}$  system to fit their results, in our case the electron penetration is limited within a narrow region of the insulator close to the semiconductor interface.

The spatial extension of the detected bulk traps from the  $\text{Al}_2\text{O}_3/\text{AlGaIn}$  interface is an information needed to convert the amount of traps in the volume fraction from the surface density determined from the  $\Delta V_{\text{PO}}$  shifts. From Fig. 4b and Fig. 6b it is possible to determine the amount of traps in the volume fraction (about 1.5 nm from the semiconductor interface) of the insulator interested by the trapping/detrapping phenomena of  $N_{\text{bulk}} \approx 3 \times 10^{19} \text{ cm}^{-3}$ . This is one order of magnitude lower trap concentration compared to the believed and detected by PL oxygen vacancies concentration [9]. Hence, it is possible to argue that only a part of the oxygen-related defects is actually active as an electron trap or on another hand, the total amount of the F-centers is lower than argued from the PL analysis.

As can be seen in Fig. 4b, the increasing rate of the  $\Delta V_{\text{PO}}$  measured with increasing the positive gate bias stress (i.e.  $V_G = +14$  V) has different behaviors at different temperatures. This means that the larger the positive gate bias stress is the deeper bulk trap can be reached. In particular, it can be noticed that increasing the temperature the gate bias stress curves show a different growing

behavior with a concavity change above 100 °C. This result can be analyzed and interpreted looking at the  $\Delta V_{PO}$  measured at  $V_G = +14$  V at different temperatures, which is reported in an Arrhenius-like plot in Fig. 7.

As can be noticed in Fig. 7, the amount of the detected charged bulk traps first increases with increasing the gate bias stress temperature up to 100 °C, and then decreases upon a further increase of the temperature up to 150 °C. Hence, the presence of two competitive trap-assisted mechanisms is envisaged. In particular, it can be argued that one mechanism is favorable to the bulk trap filling – with an activation energy of  $E_A \sim 22$  meV (with the assumption of  $N_{OT} \propto \pm E_A/kT$ ) – dominating at low temperature, while a second mechanism promotes the electron emission from the traps states – with an activation energy of  $E_A \sim 88$  meV – once the temperature is raised.

Fig. 8 schematically illustrates the trapping/detrapping effect occurring near the  $Al_2O_3/AlGaN$  interface.

As mentioned before, by increasing the gate bias stress no charge deeper than 1.5 nm from the semiconductor interface is stimulated. However, by increasing the gate biasing one can enhance the emission of the trapped charge in the insulator conduction band moving toward the metal gate.

## CONCLUSION

The electron trapping occurring in the bulk of  $Al_2O_3$  films grown by plasma enhanced atomic layer deposition on  $AlGaN/GaN$  heterostructures has been studied by means of time-dependent C-V characterizations at different temperatures. These characterizations allowed to determine the maximum depth of the insulating layer interested by a negative charge trapping effect and to determine the amount of volume charge traps in the bulk  $Al_2O_3$  in the order of  $3 \times 10^{19} \text{ cm}^{-3}$ . These electron bulk traps can be associated with a fraction of the oxygen vacancies revealed by PL measurements. Hence, only a fraction optically detected point defects is electrically active.

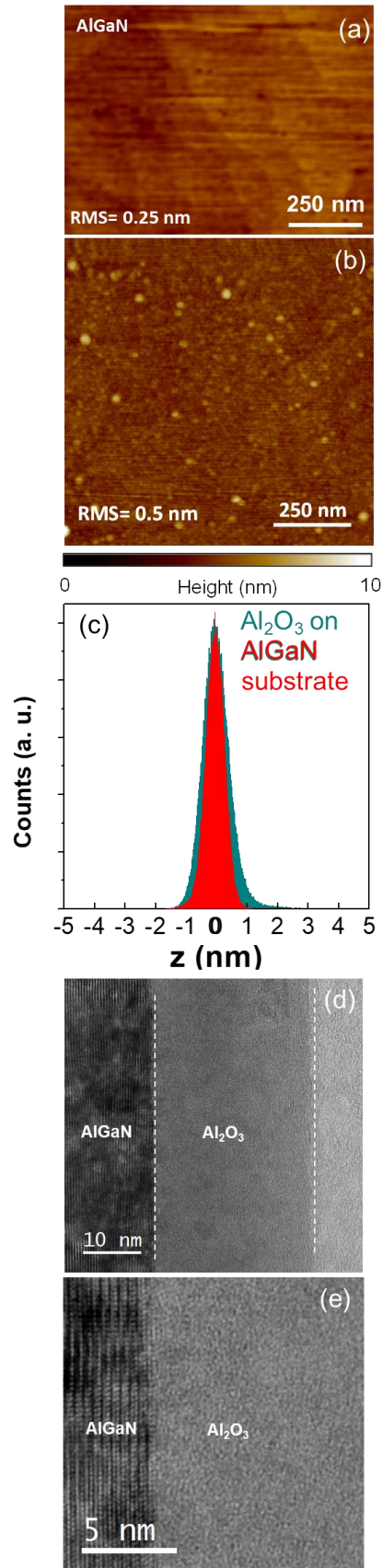
A temperature dependent C-V analysis demonstrated the presence of two competitive trap-assisted mechanisms that promote the electron capture and the emission in the Al<sub>2</sub>O<sub>3</sub> film. These charge trapping effects are stable up to 100°C under reverse bias stress operation.

These results can be particularly useful for device manufacturers and open new routes for controlling the enhancement-mode operation in AlGaN/GaN MISHEMTs.

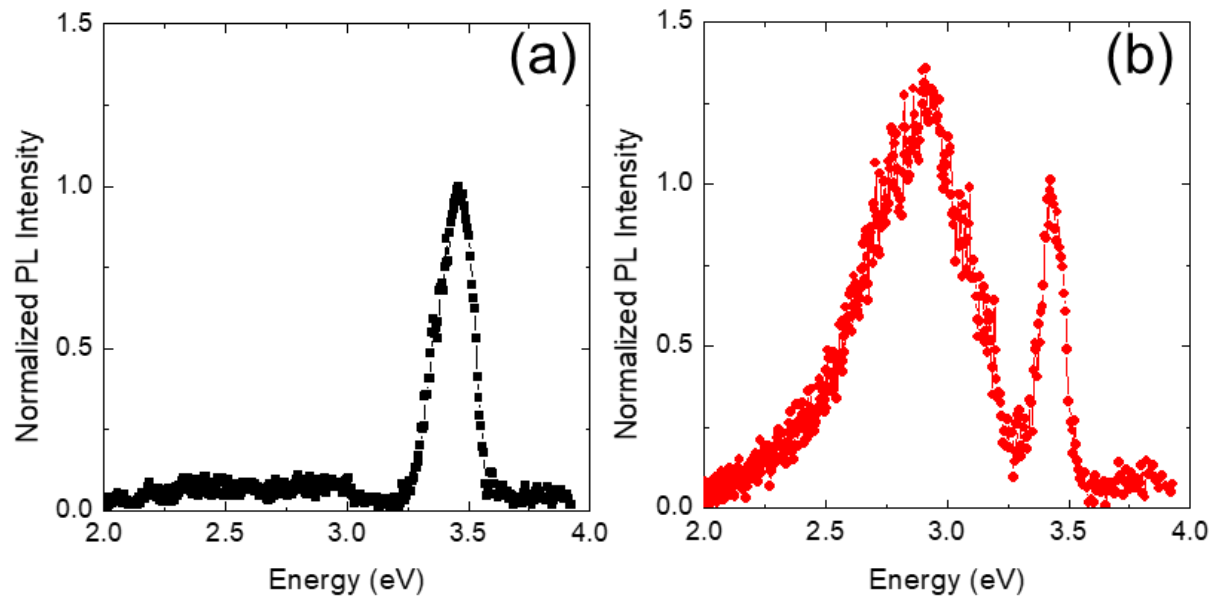
## ACKNOWLEDGMENTS

The authors would like to thank S. Di Franco and C. Bongiorno for technical assistance during device fabrication and TEM analyses, respectively. This work has been funded by the Italian Ministry for University and Research (MUR) in the framework of the National Project PON EleGaNTe (Electronics on GaN-based Technologies), ARS01\_01007.

The data that support the findings of this study are available from the corresponding author upon reasonable request.

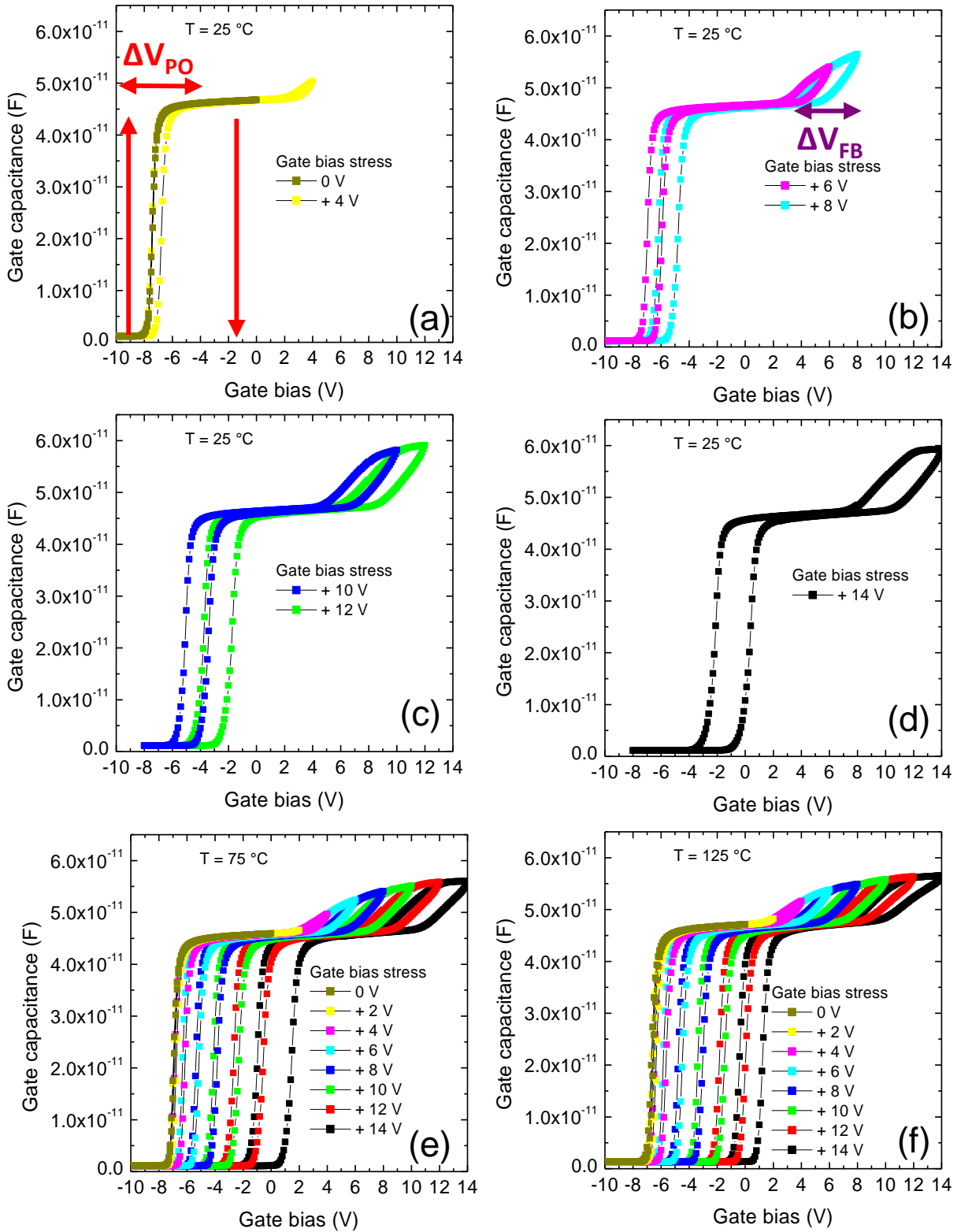


**Fig. 1:** (a) Morphological AFM image on the AlGaN/GaN and (b) Al<sub>2</sub>O<sub>3</sub>/AlGaN/GaN bare surfaces respectively. The heights distributions collected on the substrate and on the Al<sub>2</sub>O<sub>3</sub> (c). Low and high resolution cross-sectional TEM image of the Al<sub>2</sub>O<sub>3</sub>/AlGaN interface (d) and (e) respectively.

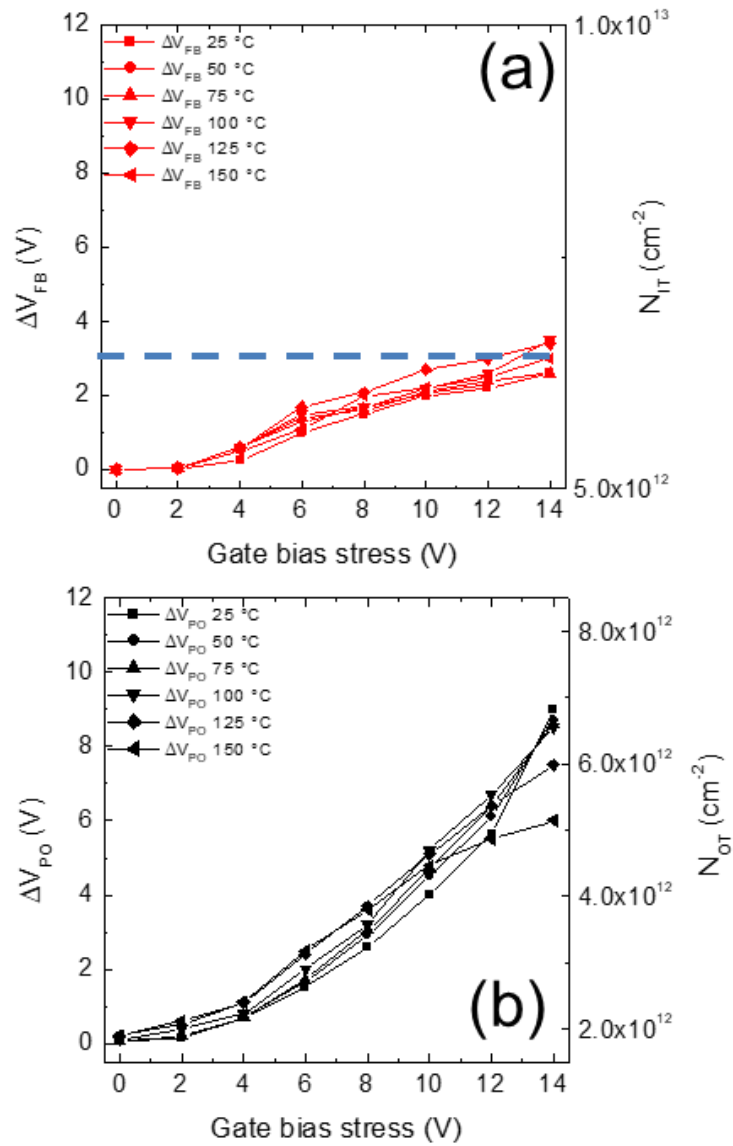


**Fig. 2:** PL-spectrum measured under laser excitation at 5.85 eV for (a) the AlGaIn/GaN and (b) Al<sub>2</sub>O<sub>3</sub>/AlGaIn/GaN sample.

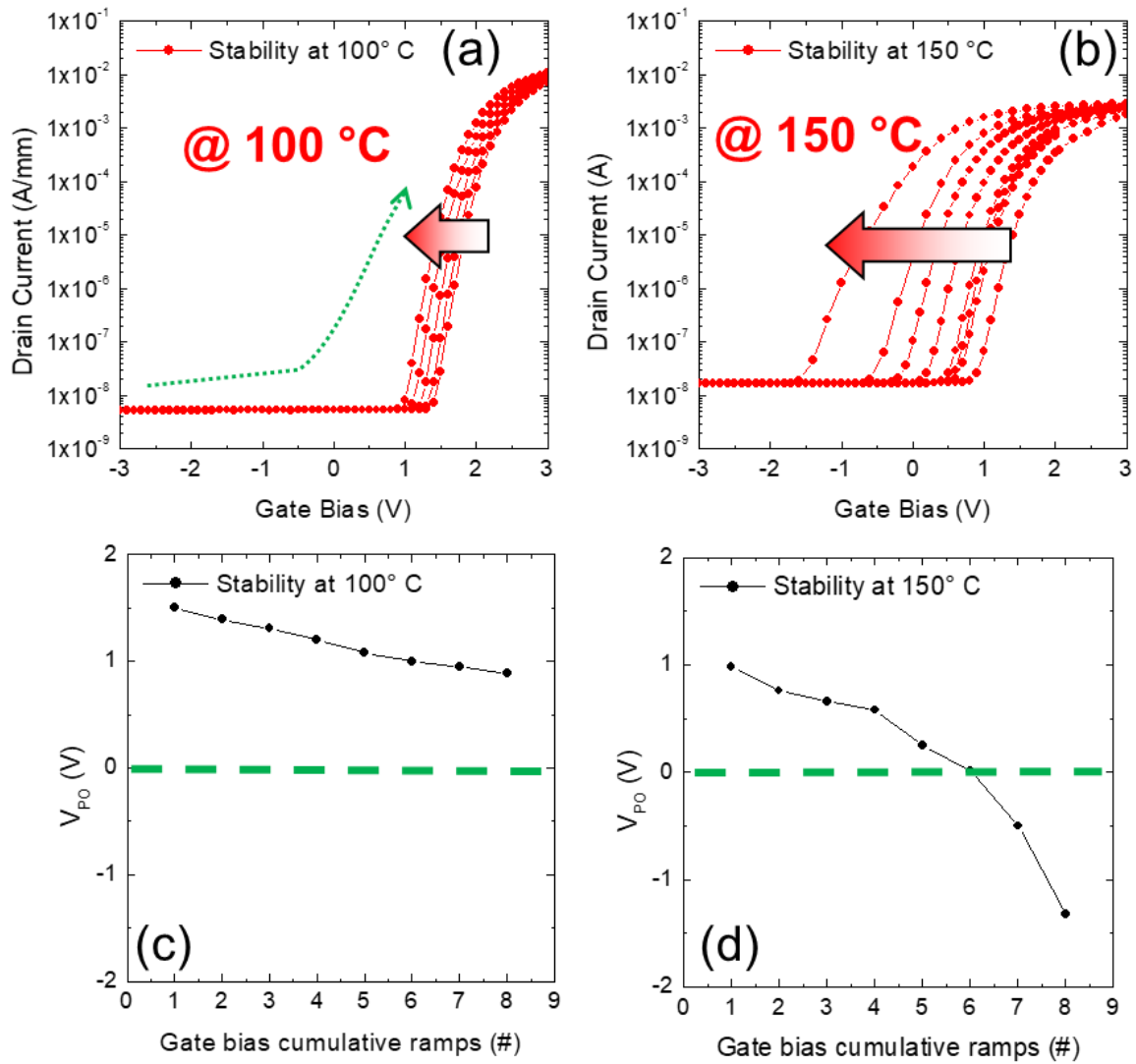




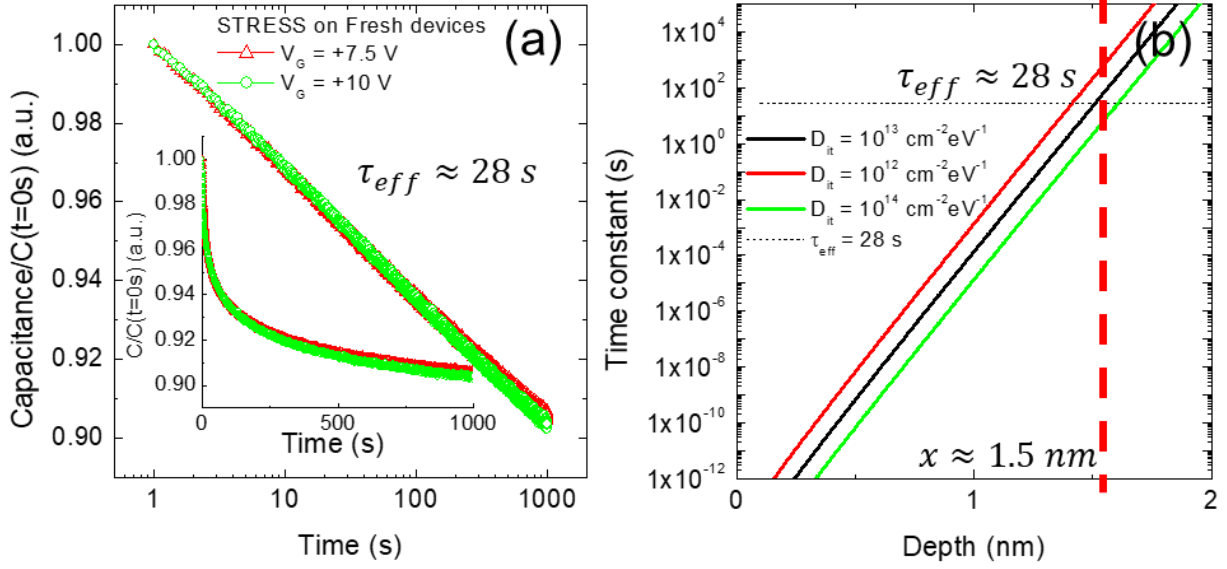
**Fig. 3:** C-V curves collected on an  $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$  MIS capacitor sweeping the gate bias from depletion-to-accumulation and backward, by increasing the final the gate bias value at different temperatures:  $25^\circ\text{C}$  (a),  $75^\circ\text{C}$  (b); and  $125^\circ\text{C}$  (c).



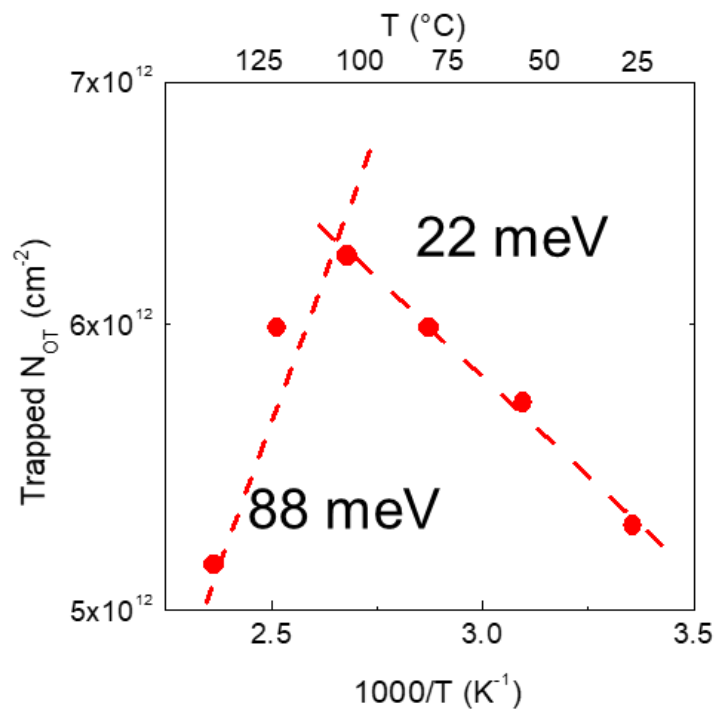
**Fig. 4:** Flat band voltage shift  $\Delta V_{FB}$  (a) and pinch-off bias shift  $\Delta V_{PO}$  (b) extracted from the cyclic C-V curves collected at temperatures from 25 up to 150 °C.



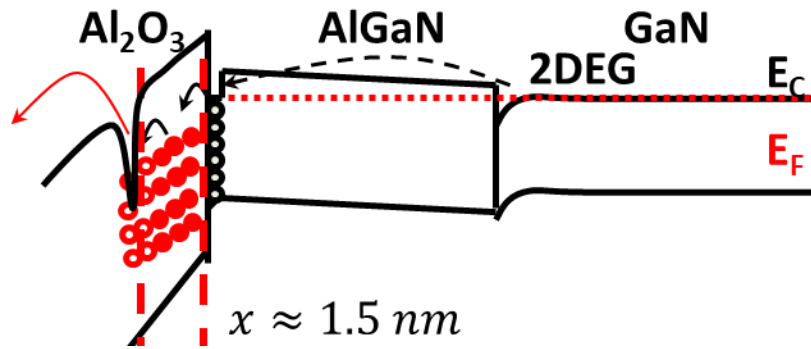
**Fig. 5:** (a) Series of 8  $I_D$ - $V_G$  characteristics collected at  $V_{DS}=0.1V$  for the  $Al_2O_3/AlGaIn/GaN$  MISHEMT after gate bias stress at 14V collected at 100 °C (a) and at 150°C (b). Shift of the pinch-off  $\Delta V_{PO}$  observed on the  $I_D$ - $V_G$  characteristics after each ramp of stress, at 100 °C (c) and 150 °C (d).



**Fig. 6:** (a) Experimental  $\Delta C/\Delta C_0$  vs time acquired on  $\text{Al}_2\text{O}_3/\text{AlGaN}$  MIS capacitors subjected to two different gate bias stress of 7.5V and 10V. In the inset, the capacitance exponential decay is shown in linear time scale. (b) Time constant as a function of the depth between the bulk traps and the  $\text{Al}_2\text{O}_3/\text{AlGaN}$  interface, calculated using Eq. 4. The experimental value  $\tau_{eff}=28$ s correspond to a depth  $x=1.5$  nm.



**Fig. 7:** Arrhenius plot of the trapped charge density determined from the  $\Delta V_{PO}$  measured in Fig.2 at  $V_G = +14$  V.



**Fig. 8:** Schematic energy band diagram of the Al<sub>2</sub>O<sub>3</sub>/AlGaN/GaN system at  $V_G \gg 0 \text{ V}$ . The electron spill-over from the 2DEG is filling the bulk oxide traps at a distance of 1.5 nm from the semiconductor interface.

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