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Topical Review

Silicon spin qubits from laboratory to industry

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Abstract

Quantum computation (QC) is one of the most challenging quantum technologies that promise to revolutionize data computation in the long-term by outperforming the classical supercomputers in specific applications. Errors will hamper this quantum revolution if not sufficiently limited and corrected by quantum error correction codes thus avoiding quantum algorithm failures. In particular millions of highly-coherent qubits arranged in a two-dimensional array are required to implement the surface code, one of the most promising codes for quantum error correction. One of the most attractive technologies to fabricate such large number of almost identical high-quality devices is the well known metal-oxide-semiconductor technology. Silicon quantum processor manufacturing can leverage the technological developments achieved in the last 50 years in the semiconductor industry. Here, we review modeling, fabrication aspects and experimental figures of merit of qubits defined in the spin degree of freedom of charge carriers confined in quantum dots and donors in silicon devices along with classical electronics innovations for qubit control and readout. Furthermore, we discuss potential applications of the technology and finally we review the role of start-ups and companies in the silicon-based QC era.

Keywords: silicon qubits, CMOS technology, semiconductor qubit readout schemes, Cryo-CMOS electronics

(Some figures may appear in colour only in the online journal)

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1. Introduction

Quantum computation (QC) is one of the most challenging quantum technologies that promise to outperform classical computation for a list of specific problems, such as search algorithm, device/system simulations and prime factorization.

Information has to be represented in a suitable physical system to perform a QC and silicon spin qubits are part of a wider semiconductor spin qubits platform that fulfills the requirements for QC: the well-known DiVincenzo criteria [1]. These are:

(1). Identification of well-defined quantum bits (qubits), where a qubit is a quantum two-level system with distinguishable basis states $|0\rangle$ and $|1\rangle$, to generate a scalable quantum register.
(2). A reliable state preparation to perform qubit initialization.
(3). Low decoherence is needed to assure several basic logical operations during the qubit coherence time.
(4). A universal set of quantum gate operations to manipulate the qubit state.
(5). A viable quantum measurement for the qubit readout.

The definition of a qubit in spin states of charge carriers in semiconductors is a natural choice and this is particularly true in silicon, where the exploitation of the complementary metal-oxide-semiconductor (CMOS) fabrication technology developed in the last 50 years and the availability of isotopic purification techniques are two fundamental qubit technology boosters.

Then scale is another motivation to use silicon spin qubits: sub 100 nm scale for qubit (quantum dot (QD) or donor based) along with the at least 1 million qubit required for the implementation of quantum error correction (QEC) surface code [2] can lead to dense QC system produced by the semiconductor electronics industry.

The scope of this review is limited to silicon spin qubits in gate-defined QDs and donors fabricated by industries or with a foundry-compatible approach.

This review article is organized as follows: section 2 includes a collection of published and recent pre-printed reviews where silicon qubits are considered. The different qubit types, categorized by the qubit holder and then subcategorized by the number of spins are studied in section 3. Section 4 focuses on the qubit readout schemes and the fabrication of silicon qubits is reviewed in section 5. Section 6 is focused on classical electronics for qubit control and readout whereas the scalability and application issues are reviewed in section 7. We conclude by commenting on future ways of Si QC development in section 8.

2. Reviews on semiconductor qubits

Since 2017 an increasing number of reviews on QC in (not only) semiconducting materials has been published but only a few are found with a specific focus on quantum computation based on Si metal-oxide-semiconductor (MOS) devices.

In particular, in 2017 Vandersypen *et al* reviewed the spin qubits in semiconductors with a specific focus on their scaling up [3]. In the same year, the review from Russ *et al* dealt with the theory of spin qubits based on configurations of three electrons confined in QDs [4].

In 2019 Zhang *et al* provided a comprehensive study of semiconducting qubits, reviewing their modeling and characterization aspects [5] whereas in 2020 Morello *et al* proposed a review on donor spins in silicon for quantum technologies [6].

In 2021 the number of reviews on qubits in semiconductors has increased notably: De Leon *et al* focused their study on the material side, comparing performances among different platforms even based on not only semiconducting materials [7], McCallum *et al* reviewed donor-based qubits in silicon [8], Saraiva *et al* addressed the material issues on QD-based qubits in silicon [9], Gonzalez-Zalba *et al* dealt with the scaling of QD-based qubits in MOS technology [10] and Chatterjee *et al* reviewed QDs and donors spin qubits in semiconductors with a particular focus on applications in quantum sensing, communication and computation [11]. In the same year, Burkard *et al* pre-printed a very extensive review covering theory, characterization and fabrication of spin qubits in semiconductors [12].

In 2022, Stano and Loss presented a review on the performance metrics of spin qubits in gated semiconducting nanostructures with a broad comparison among the performances of all the different known qubit kinds in Si, GaAs and Ge [13].

None of the cited reviews focuses predominantly on industrial fabricated silicon qubits and on the aspects leading to the transition from laboratory to industrial fabrication thus this topical review aims to close this gap.

3. Qubit types

In this section the qubits are sorted by qubit holder type leading to three different sections: QD-based, donor-based and QD-donor based qubits. For each qubit holder, we describe qubit types differing on the number of exploited spins. In literature, spin qubits are referred to as physical qubits, while composed qubits made of more than one physical unit are called virtual qubits [14]. They should not be confused with logical qubits which arise after some QEC method is applied. The set of qubit types collected in this review is reported in table 1 and for each qubit its scheme flanked by the corresponding energy level diagram is shown in figure 1. Some simulation studies comparing performances among different types of physical spin qubits based on QD(s) and donors have already been published [15, 16].

3.1. QD-based qubits

3.1.1. 1 spin: Loss-DiVincenzo. In the Loss-DiVincenzo qubit [17], realized confining the spin of a single electron in a QD, the logical qubit basis is defined by the two spin eigenstates $|0\rangle \equiv |\uparrow\rangle$ and $|1\rangle \equiv |\downarrow\rangle$, i.e. the angular momentum states with $S = \frac{1}{2}$, $S_z = \frac{1}{2}$ and $S = \frac{1}{2}$, $S_z = -\frac{1}{2}$ respectively. It is modeled through the time-dependent Hamiltonian

Table 1. Qubit types grouped by the number of spin-1/2 per qubit, kind of qubit (physical or virtual) and the type of confining element: QD, donor or QD-donor.

Number of spins	Qubit type	QD-based	Donor-based	QD-donor -based
1	Physical	Loss-DiVincenzo [17]	donor bounded e^- [18]	
2	Virtual	singlet-triplet [19, 20]		$e^-/^{31}P^+$ flip-flop [21, 22] Carroll [23–25]
3	Virtual	hybrid [26, 27] exchange only [1]		

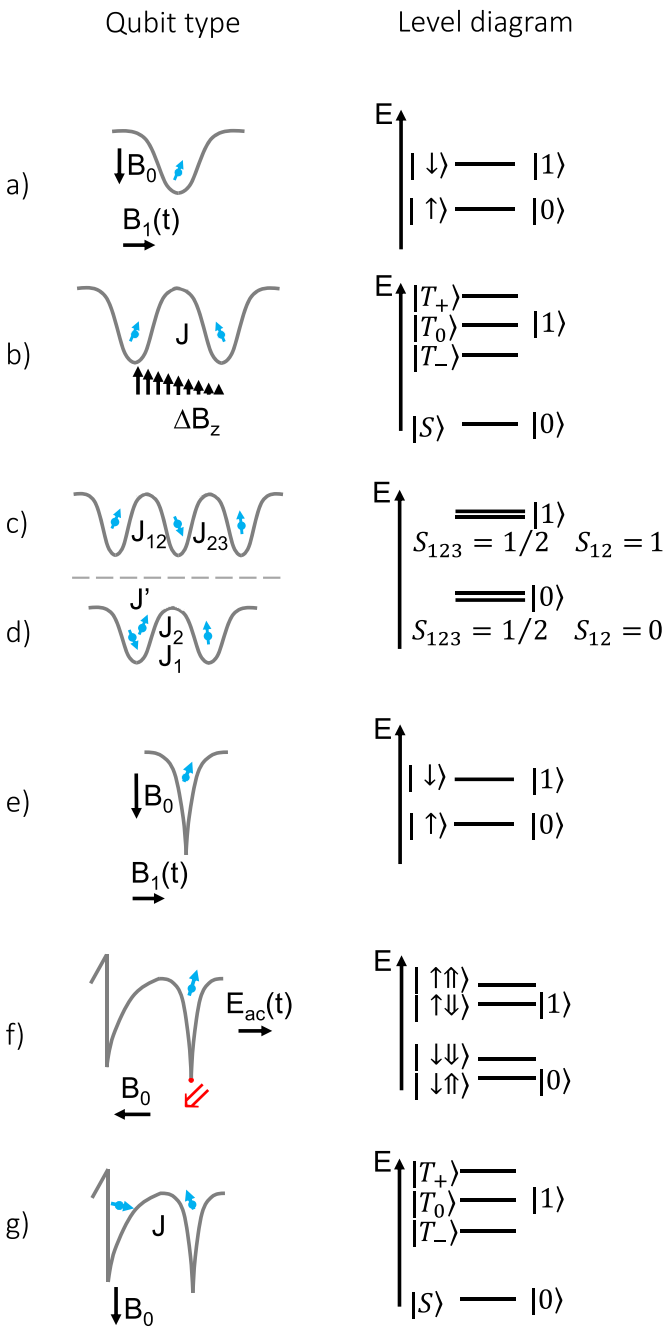

Figure 1. Qubit confining profiles and their corresponding energy level diagram (a) Loss-DiVincenzo qubit. (b) Singlet-triplet qubit. (c) Exchange Only qubit and (d) Hybrid qubit having the same computational basis states. (e) Donor-bounded e^- qubit. (f) $e^-/^{31}P^+$ flip-flop qubit. (g) Carroll qubit.

$$H = \frac{\hbar}{2}\omega_z\sigma_z + \hbar\Omega_x\cos(\omega t)\sigma_x \quad (1)$$

that prevents itself from an analytical solution. In equation (1) $\sigma_{z(x)}$ is the Pauli operator, $\hbar\omega_z = g_e\mu_B B_0$ is the Zeeman energy associated to the constant magnetic field in the z direction B_0 with g_e the electron g-factor and μ_B the Bohr magneton and $\hbar\Omega_x = g_e\mu_B B_1/2$ where B_1 is the oscillating magnetic field amplitude and ω is its angular frequency.

The time-independent Hamiltonian is obtained into a rotating frame, which rotates at the angular frequency ω, under the rotating wave approximation achieving the following form

$$H = H_z + H_x = \frac{\hbar}{2}(\omega_z - \omega)\sigma_z + \frac{\hbar}{2}\Omega_x\sigma_x, \quad (2)$$

where the Larmor angular frequency ω_z and the amplitude Ω_x of the AC local magnetic field are adopted as input controls.

The approaches implemented to control the qubit are various: (1) electron spin resonance (ESR) using local AC magnetic fields [28], (2) application of global magnetic fields for local manipulation, (3) all-electrical manipulation via AC electric fields in a magnetic field gradient [29]. For the qubit initialization a single-shot measurement, where it is tested if the spin orientation is parallel or anti-parallel to the external magnetic field, is exploited [30]. The read-out, in which the state of the qubit is determined after implementing the algorithm, can rely on spin-to-charge conversion, where the tunneling of a single electron towards a reservoir can be measured through an integrated charge sensor or can exploit RF reflectometric techniques, using gate electrodes coupled to off-chip lumped-element resonators [31]. A detailed explanation of the qubit readout mechanisms is provided in section 4.

Furthermore, spin qubits could in principle be coherently moved across an odd array of QDs by control gate operations based on coherent tunneling by adiabatic passage sequences [32–34]. For all the qubit types reported, we indicate the coherence time T_2^* that by definition is extracted from a Ramsey experiment and is different from the dephasing time T_2 obtained though spin echo. From an experimental point of view, the state-of-the-art performances of Loss-DiVincenzo qubits are obtained with electrons in natural Si and isotopically purified silicon (^{28}Si): starting from the coherence time, a $T_2^* = 120\ \mu s$ is reached for electrons in QDs in a $^{28}Si/SiO_2$ system [35]. Gate times down to $T_{\text{gate}} = 42\ ns$ are obtained in QDs in Si/SiO_2 device [36], initialization times down to $T_{\text{init}} = 50\ \mu s$ in Si/SiGe QDs [37] and measurement times down to $T_{\text{meas}} = 24\ \mu s$ in Si/SiGe QDs [38]. Regarding the operation fidelities obtained by Randomized Benchmarking, one-qubit gate fidelities up to $F_{1Q} = 99.957\%$ in a $^{28}Si/SiO_2$ system are achievable [39] as well as two-qubit gate fidelity up to $F_{2Q} = 99.81\%$ in ^{28}Si/SiGe QDs [40]. Also high values are obtained for the initialization fidelity $F_{\text{init}} = 99\%$ in Si/SiGe QDs [37] and measurement fidelity $F_{\text{meas}} = 99\%$ in ^{28}Si/SiGe device [40]. The system with the largest number of Loss-DiVincenzo qubits demonstrated by now is a 6 qubit ensemble displaced in a linear array [41].

Moving from the electron to the hole carrier type, the reduced susceptibility to nuclear noise, the lack of valley degeneracy, the low in-plane effective mass, and the possibility to achieve a fully-electric fast control provided via a strong Spin-Orbit Interaction (SOI) make holes confined in silicon QDs a very attractive platform for scalable spin qubits. In general, SOI, also known as Spin Orbit Coupling, arises from the relativistic coupling of a particle's spin to electric fields thus a spin moving in a potential experiences an effective magnetic field that is momentum-dependent [42]. Moreover, additional SOI effects emerge in quantum wells and QDs due to quantum confinement and lowered symmetries. Thus, SOC can be important either as a decoherence mechanism or more interestingly as a tool to drive spins as holes in Si and Ge. SOI and g-factor engineering has been already exploited to address spin in Si MOS devices [43–46].

From the theoretical point of view, a three-dimensional qubit description of the single hole confined in a QD can be simplified to a two-level model with the following Hamiltonian H describing the qubit of spin 1/2,

$$H = \sum_{i,j=x,y,z} \mu_B B_i \hat{g}_{ij} \tau_j \quad (3)$$

where μ_B is the Bohr's magneton and B is the space vector of the magnetic field, τ is a vector of Pauli matrices defined with up and down spin one-half states corresponding to perturbed states (mixed HH and LH spin states), and $\hat{g}$ is the (second-rank) g-tensor. This model provides orbital effects through the g-tensor dependence on confining electric fields that provide control [47]. In other words, driving AC electric fields can modify the confining potential and thus the wave function, which can be interpreted as an effective time-modulation of the g-tensor which can produce spin rotations [48]. The readout of a single hole qubit can be performed in a similar way as for a (electron based) Loss-DiVincenzo qubit.

The state-of-the-art performances of single spin hole qubits in silicon are the following: a coherence time $T_2^* = 0.44\ \mu s$ is reached with operations of gate time $T_{gate} = 3.4\ ns$ and single qubit gate fidelity up to $F_{1Q} = 98.9\%$ in a Si/SiO_2 QD [49].

3.1.2. 2 spins: singlet-triplet. Two electrons, ideally spatially separated, in two QDs are the elements to create the singlet-triplet qubit. Therefore the logical states are defined by a superposition of two-particle spin singlet and triplet states, that are $|0\rangle \equiv |S\rangle$ and $|1\rangle \equiv |T_0\rangle$, where each QD is occupied with one electron. An external magnetic field removes the $|T_-\rangle$ and $|T_+\rangle$ branches.

The Hamiltonian model

$$H = \frac{\hbar}{2}\Delta\omega_z(\sigma_1^z - \sigma_2^z) + \frac{1}{4}J\boldsymbol{\sigma}_1\cdot\boldsymbol{\sigma}_2 \quad (4)$$

is composed by the exchange interaction between the two electrons, described by the Pauli matrices $\boldsymbol{\sigma}_1$ and $\boldsymbol{\sigma}_2$, through the coupling constant J and the Zeeman term corresponding to a magnetic field gradient between the QDs adopted for the single qubit control, that is $\Delta\omega_z = (\omega_1^z - \omega_2^z)$. The analytical form of the exchange coupling J is derived from a generalized

Hubbard model adopting a standard procedure based on the Schrieffer–Wolff transformation [50] and it is

$$J = \frac{4(t - J_t)^2}{U - U' - |\Delta\varepsilon|} - 2J_e, \tag{5}$$

where t is the single-electron tunneling across the double QD (DQD), J_t is the single-electron tunneling in the presence of a second electron, U (U') is the intradot (interdot) Coulomb repulsion, $\Delta\varepsilon$ is the interdot bias, i.e. the single electron ground-orbital energy difference between the two dots and J_e is the direct exchange interaction of the two electrons across the DQD.

Qubit state rotations are performed through the exchange coupling J between the two electrons acting on the energy detuning. Moreover a local magnetic field gradient is necessary to achieve arbitrary qubit rotations.

To initialize the singlet-triplet qubit in a singlet spin state it is necessary to load an electron in the single occupied QD, from $(1,0)$ to $(2,0)$ charge configuration. The readout is instead achieved using the Pauli spin blockade [51]. Singlet-triplet qubit allows fast readout and fast manipulation, however experimentally the big challenge is represented by the creation of the local magnetic gradient [19, 20, 31, 52, 53]. A valid strategy to achieve such task is represented by the use of a micromagnet in close proximity [20, 52, 53].

The state-of-the-art performances of working singlet-triplet qubits are: $T_2^* = 12\ \mu s$ in a $^{28}Si/SiO_2$ DQD system [54]. Gate times down to $T_{\text{gate}} = 2.5\ ns$ are obtained in $^{28}Si/SiO_2$ device [55], initialization times down to $T_{\text{init}} = 20\ ms$ in Si/SiO_2 QDs [56] and measurement times down to $T_{\text{meas}} = 50\ ns$ in Si/SiO_2 systems [57]. Regarding the operation fidelities, one-qubit gate fidelity up to $F_{1Q} = 99.76\%$ in a $^{28}Si/SiO_2$ systems are achievable [54]. Experimental values for the measurement fidelity $F_{\text{meas}} = 75\%$ in Si/SiO_2 device are obtained [58].

3.1.3. 3 spins: hybrid. The hybrid qubit is a three spins qubit and owes its name to the fact that is an *hybrid* of spin and charge qubit [26, 59]. It is realized in a DQD in which three electrons have been confined with all-electrical control via gate electrodes [60–69]. The logical states have been defined by adopting combined singlet and triplet states of a pair of electrons occupying one dot with the states of the single electron occupying the other and they are $|0\rangle \equiv |S\rangle|\uparrow\rangle$ and $|1\rangle \equiv \sqrt{\frac{1}{3}}|T_0\rangle|\uparrow\rangle - \sqrt{\frac{2}{3}}|T_+\rangle|\downarrow\rangle$ where $|S\rangle$, $|T_0\rangle$ and $|T_\pm\rangle$ are the singlet and triplet states of two electrons. The value of the total angular momentum operator S specifies whether the decoherence free subsystem qubit has leaked; S = 1/2 is unleaked while S = 3/2 is leaked. The effective Hamiltonian model involving only exchange interaction terms among couples of electrons for a single and two qubits was derived in [70] and in [71], respectively and is equal to

$$H = \frac{\hbar}{2}\omega_z(\sigma_1^z + \sigma_2^z + \sigma_3^z) + \frac{1}{4}J'\boldsymbol{\sigma}_1\cdot\boldsymbol{\sigma}_2 + \frac{1}{4}J_1\boldsymbol{\sigma}_1\cdot\boldsymbol{\sigma}_3 + \frac{1}{4}J_2\boldsymbol{\sigma}_2\cdot\boldsymbol{\sigma}_3, \tag{6}$$

where the effective coupling constants are given in [70].

To initialize the qubit in the state corresponding to the $|0\rangle$ logical state, all the variables are regulated through appropriate external electric and magnetic fields. After that, it is possible to lead the desired logical gates through operations that are generally described by unitary matrices. In order to inject electrons in the QDs a reservoir as source of electrons near the double QD is required. The height of the energy barrier between the reservoir itself and the double QD is controlled through an electrostatic gate. A charge sensor enables the readout of the spin state of electrons confined in the doubly occupied QD. A single-electron transistor (SET) can be used to electrostatically sense the spin state of the electrons. When readout of the qubit starts, tunneling is allowed from the doubly occupied QD to some reservoir by a reduction in the interposed electrostatic barrier. When the electron pair is in a singlet state the corresponding wavefunction is more confined and the tunneling rate to the reservoir is lower than that of the triplet state, which has a broader wavefunction. When the electron tunnels, the electrostatic potential landscape changes and so does the current passing through the electrostatically coupled SET. The measurement of the time interval between the read out signal and the current variation in the SET is supposed to reveal the spin state of the electron pair.

In this qubit the manipulation is all electrical and very fast. The state-of-the-art coherence time of an hybrid qubit is $T_2^* = 177$ ns [72] with gate times down to $T_{\text{gate}} = 45$ ps [59] and highest achieved one-qubit gate fidelity of $F_{1Q} = 94.5\%$ in a Si/SiGe DQD [73].

3.1.4. 3 spins: exchange only. A full all-electrical qubit through the exchange interaction is the exchange only qubit, a three-qubit decoherence free subsystem, in which three spins are confined in a triple QD. It can be controlled by electrostatic control of the gates underneath and in between the QDs. Focusing on the eight-dimensional subspace with a symmetric (1, 1, 1) charge configuration, a Schrieffer–Wolff transformation yields an effective Heisenberg Hamiltonian with three effective exchange coupling parameters

$$H = \frac{1}{4}J_{12}\boldsymbol{\sigma}_1\cdot\boldsymbol{\sigma}_2 + \frac{1}{4}J_{23}\boldsymbol{\sigma}_2\cdot\boldsymbol{\sigma}_3 + \frac{1}{4}J_{13}\boldsymbol{\sigma}_1\cdot\boldsymbol{\sigma}_3, \tag{7}$$

note that when a linear arrangement is considered, $J_{13} = 0$. The logical states are defined in the doublets in correspondence to $S = \frac{1}{2}$ with projection $S_z = \pm\frac{1}{2}$. When $S_z = \frac{1}{2}$ an appropriate basis is given by: $|0\rangle \equiv |S\rangle_{13}|\uparrow\rangle_2$ and $|1\rangle \equiv -\sqrt{\frac{1}{3}}|T_0\rangle_{13}|\uparrow\rangle_2 + \sqrt{\frac{2}{3}}|T_+\rangle_{13}|\downarrow\rangle_2$ where $|S\rangle$, $|T_0\rangle$ and $|T_\pm\rangle$ are the singlet and triplet states of a pair of electrons and the subscript specify the pair involved. Analogously it is possible to define the logical states in the subspace with projection $S_z = -\frac{1}{2}$ in which all spins are flipped.

The state-of-the-art performances of working exchange only qubits are the following: coherence times $T_2^* = 2\ \mu s$, gate times down to $T_{\text{gate}} = 10\ ns$ and measurement times of $T_{\text{meas}} = 0.98\ \mu s$ in QDs in $^{28}Si/SiGe$ stack [74]. Regarding the operation fidelities, one-qubit gate fidelity up to $F_{1Q} = 99.88\%$ in a Si/SiGe system is achievable [75] and measure fidelity up to $F_{\text{meas}} = 99.975\%$ in $^{28}Si/SiGe$ QDs has been obtained [76].

3.2. Donor-based qubits

3.2.1. 1 spin: donor bounded e^-. This qubit is implemented on the spin of an electron bound to a donor and the qubit basis is given by the single electron spin $|0\rangle \equiv |\uparrow\rangle$ and $|1\rangle \equiv |\downarrow\rangle$ logical states. The spin Hamiltonian common for group V donors in silicon is given by [18, 77–80]

$$H = \gamma_e B_0 S_z - \gamma_n B_0 I_z + \Omega_x \cos(\omega t) S_x + A\boldsymbol{S}\cdot\boldsymbol{I}. \tag{8}$$

The first two terms are respectively the electronic $\boldsymbol{S}$ and nuclear $\boldsymbol{I}$ spin Zeeman interactions with an external field B_0, where $\gamma_e = \mu_B g_e$ and $\gamma_n = \mu_n g_n$ with μ_B (μ_n) the Bohr (nuclear) magneton and g_e (g_n) the electron (nuclear) g-factor. The third term represents the microwave control. The last term corresponds to the hyperfine coupling where $A = \frac{8}{3}\pi\mu_B g_n \mu_n |\psi(0)|^2$ is the contact hyperfine interaction energy with $|\psi(0)|^2$ the probability density of the electron wavefunction evaluated at the nucleus [77]. The electron and nuclear gyromagnetic ratios as well as the hyperfine constant A are measurable by estimating the magnetic field dependencies of the spin transition frequencies.

When $I = 1/2$, that is the case of ^{31}P, and in the high field limit, i.e. $\gamma_e B_0 \gg A$, the diagonal terms of the hyperfine interaction become negligible and the ESR allowed transition are confined in two distinct subspaces, one in which the nuclear spin has down projection $|\Downarrow\rangle$ and the complementary in which the nuclear spin has up projection $|\Uparrow\rangle$. The Hamiltonian models that describe the qubit in the two subspaces are

$$H_{\{\uparrow,\downarrow\}\otimes\Downarrow} = \frac{\hbar}{2}(\omega_{12} - \omega)\sigma_z + \frac{\hbar}{2}\Omega_x\sigma_x \tag{9}$$

and

$$H_{\{\uparrow,\downarrow\}\otimes\Uparrow} = \frac{\hbar}{2}(\omega_{34} - \omega)\sigma_z + \frac{\hbar}{2}\Omega_x\sigma_x, \tag{10}$$

where $\omega_{12} = \Delta_- + \sqrt{\Delta_+^2 + 4a^2} - 2a$, $\omega_{34} = \Delta_- + \sqrt{\Delta_+^2 + 4a^2} + 2a$ with $\Delta\pm = \frac{1}{2}(\gamma_e \pm \gamma_n)B_0$ and $a = \frac{A}{4}$.

Rabi oscillations are driven through ESR. Coherence times are longer in comparison with the previous architectures and can reach values ranging in hundreds of microseconds [81, 82] and this is due to the weak spin–orbit coupling. The control and manipulation of the single spin take place using local AC magnetic fields with sub microsecond gate times and fidelities up to $F_{1Q} = 99.4\%$ [83]. The spin read out uses the detection of tunnelling to a nearby reservoir, the so called energy filtering or Elzerman readout as explained in section 4.1.1. Deep donors have also been considered to serve as physical substrate for spin qubits in silicon [84, 85].

3.3. QD-Donor qubit

3.3.1. 2 spin: $e^-/^{31}P^+$ flip-flop. The flip-flop qubit is realized embedding a phosphorous ^{31}P donor atom in a ^{28}Si substrate at a depth d from the interface with a SiO_2 layer. A vertical electric field E_z applied by a metal gate on top, controls the position of the electronic wavefunction [21, 22, 86]. The electronic spin (S = 1/2) is described in the basis $\{|\downarrow\rangle, |\uparrow\rangle\}$ and has a gyromagnetic ratio $\gamma_e = 27.97$ GHzT^{-1}, while for the nuclear spin (I = 1/2) the basis is denoted by $\{|\Downarrow\rangle, |\Uparrow\rangle\}$ and the gyromagnetic ratio is $\gamma_n = 17.23$ MHzT^{-1}, they interact through the hyperfine coupling A. Applying a large static magnetic field B_0, (i.e. $(\gamma_e + \gamma_n)B_0 \gg A$), the eigenstates of the system are the four qubit states: $\{|\downarrow\Uparrow\rangle, |\downarrow\Downarrow\rangle, |\uparrow\Downarrow\rangle, |\uparrow\Uparrow\rangle\}$. Electrically modulating the hyperfine interaction A by E_z causes an Electron Dipole Spin Resonance (EDSR) transition between the states with antiparallel spins $\{|\downarrow\Uparrow\rangle, |\uparrow\Downarrow\rangle\}$, that are in turn chosen to encode the qubit.

The flip-flop qubit Hamiltonian model is given by the sum of three contributions [21, 87]

$$H = H_{orb} + H_{B_0} + H_A. \tag{11}$$

The orbital Hamiltonian that reads (in units of Hz):

$$H_{orb} = -\frac{\varepsilon_0}{2}\sigma_z - \frac{deE_{ac}(t)}{2h}\left(\frac{de\Delta E_z}{h\varepsilon_0}\sigma_z + \frac{V_t}{\varepsilon_0}\sigma_x\right), \tag{12}$$

where V_t is the tunnel coupling between the donor and the interface potential wells; $\Delta E_z = E_z - E_z^0$ where E_z^0 is the vertical electric field at the ionization point, i.e. the point in which the electron is shared halfway between the donor and the interface; $\varepsilon_0 = \sqrt{V_t^2 + (de\Delta E_z/h)^2}$ is the energy difference between the orbital eigenstates, where h is the Planck's constant, d is the distance from the interface and e is the elementary charge. $E_{ac}(t) = E_{ac}\cos(\omega_E t + \phi)$ is the AC electric field applied in resonance with the flip-flop qubit, i.e. $\omega_E = 2\pi\epsilon_{ff}$, where ϵ_{ff} is the flip-flop qubit transition frequency, and ϕ is an additional phase. Finally the Pauli matrices are expressed in the basis of the orbital eigenstates: $\sigma_z = |g\rangle\langle g| - |e\rangle\langle e|$ and $\sigma_x = |g\rangle\langle e| + |e\rangle\langle g|$, where $|g\rangle(|e\rangle)$ is the ground (excited) state of the orbital part of the Hamiltonian.

The second term in equation (11) is the Zeeman interaction related to the static magnetic field B_0 oriented along the $\hat{z}$ axis that includes also the dependence of the electron Zeeman splitting on its orbital position through the quantity Δ_γ and is equal to

$$H_{B_0} = \gamma_e B_0\left[\mathbf{1} + \left(\frac{\mathbf{1}}{2} + \frac{de\Delta E_z}{2h\varepsilon_0}\sigma_z + \frac{V_t}{2\varepsilon_0}\sigma_x\right)\Delta_\gamma\right]S_z - \gamma_n B_0 I_z, \tag{13}$$

where $\mathbf{1}$ is the identity operator on the orbital subspace, the electron (nuclear) spin operators are $\mathbf{S}$ ($\mathbf{I}$), with $\hat{z}$ component S_z (I_z), and $B_0 = 0.4$ T.

Finally, the third term in equation (11) is given by

$$H_A = A\left(\frac{\mathbf{1}}{2} - \frac{de\Delta E_z}{2h\varepsilon_0}\sigma_z - \frac{V_t}{2\varepsilon_0}\sigma_x\right)\mathbf{S}\cdot\mathbf{I}, \tag{14}$$

where A is the hyperfine coupling that is a function of the applied electric field ΔE_z. Simulations of parallel gate fidelity in a linear array of flip-flop qubits have been studied [88].

A first experiment on a flip-flop qubit provided a coherence time $T_2^* = 4.09$ μs with gate times of $T_{gate} = 4.16$ μs and randomized benchmarking one-qubit gate fidelity of $F_{1Q} = 98.4\%$ [89].

3.3.2. 2 spin: Carroll. The effective Hamiltonian model of the QD-donor qubit, that is the analogous of the singlet-triplet qubit, is easily written in terms of all the angular momentum operators involved [24, 25]

$$H = \gamma_e B_0 (S^z_{\text{donor}} + S^z_{\text{dot}}) - \gamma_n B_0 I_z + A\boldsymbol{S}_{\text{donor}} \cdot \boldsymbol{I} + J\boldsymbol{S}_{\text{donor}} \cdot \boldsymbol{S}_{\text{dot}}. \quad (15)$$

$\boldsymbol{S}_{\text{donor}}$ ($\boldsymbol{S}_{\text{dot}}$) represents the electron spin operator of the donor (QD) while $\boldsymbol{I}$ is the donor nuclear spin. B_0 is the applied DC magnetic field and A is the hyperfine coupling between the electron spin and the nuclear spin of the donor. J is the exchange coupling between the electron spins of the donor and of the dot. Such qubit type assures fast readout and fast manipulation via GHz one-axis electrical control [90]. From the fabrication point of view, one issue to be solved is represented by the incorporation of the donor array into the Si layer beneath the barrier layer.

The logical states depend on the transition energies selected and in this qubit type are various. Qubit operations can be indeed performed on the donor electron spin and on the dot electron spin with a pulsed microwave field, which can be delivered locally or globally by placing devices into microwave cavities. For example in [24], the qubit is defined by the singlet-triplet states between the electronic spin in the QD and the electronic spin in the donor. For the readout the SET, that is explained in section 4.2, would be integrated with the bottom gate.

The measured decoherence time of a working Carroll qubit is $T_2^* = 1.3\ \mu s$ in a ^{28}Si:P—QD system [23].

4. Qubit readout

Direct measurement of the spin degree of freedom is generally very challenging at the few-spin level, due to the small magnetic dipole moment of a single electron. This magnetic dipole moment is given by the Bohr magneton, $\mu_B \approx 57.9\ \mu\text{eV} \cdot \text{T}^{-1}$, and accordingly the spin transition frequencies are in the microwave regime of order 1 to 10 GHz, at realistic magnetic fields. On the other hand, the electric dipole moment associated with a charge transition, classically given by the product of the charge with the distance of the transfer, usually dominates light-matter interactions where the wavelength is much greater than the distances involved. Comparing the wavelength of microwave photons to the separation of charge centres in semiconductor quantum devices, it is clear the dominant interaction mechanism is the charge dipole. This is reflected in the state of the art sensitivity metrics, which are $\sim$10 spins $\cdot$ $\text{Hz}^{-\frac{1}{2}}$ for spin [91, 92] and $\sim 10^{-6}$ electrons $\cdot$ $\text{Hz}^{-\frac{1}{2}}$ for charge sensing [93–96], where these values represent the precision of a measurement integrating over a period of one second. Achieving high fidelity for the readout of qubits in general requires that the measurement is performed in a time significantly shorter than the relaxation time of the qubits, so that the state does not decay during the measurement. For QEC protocols, the measurement should be performed in timescales much faster than the decoherence time of the qubits.

Charge sensing in conjunction with the so-called spin-to-charge conversion techniques has proven a very successful approach to achieving high fidelity readout of single spins [56, 82, 97–99]. The spin information is projected into the charge degree of freedom generally by tuning the energy levels (via gate voltages) so that tunneling occurs conditionally on the spin state. We will first explain the two core mechanisms of spin-to-charge conversion, then introduce the distinct types of charge sensors and, for each case, review the progress with foundry-compatible devices towards high-fidelity readout.

4.1. Spin-to-charge conversion

4.1.1. Qubit spin with reservoir: energy filtering (Elzerman). A spin confined to a QD or donor can be read out by detecting the tunnelling to a nearby reservoir, a technique known as energy filtering or Elzerman readout [30]. As shown in figure 2(a), this protocol is performed by adjusting the gate voltage so that the reservoir Fermi energy is aligned between the spin $|\downarrow\rangle$ and $|\uparrow\rangle$ energy levels. In this configuration, if the spin occupies the low-energy $|\uparrow\rangle$ state (panel a.i), no tunneling in or out occurs due to Coulomb blockade. In the $|\downarrow\rangle$ state (panel a.ii), however, the system will seek to minimise its energy through tunnelling from the dot to the reservoir, followed by refilling the dot with a $|\uparrow\rangle$ electron. The charge sensor must be sensitive to the electron occupancy of the dot or donor, and the detection of a short-lived signal (illustrated in the panel a.ii) corresponding to the emptying of the dot will confirm the readout of a $|\downarrow\rangle$ state. The time delay and the length of the signal are both random with an exponential distribution characterised by the tunnelling-out and tunnelling-in rates, $\Gamma_{1\to0}$ and $\Gamma_{0\to1}$ respectively. Variations on this technique exploit the dependence of the tunnel rates on the energy difference between the dot energy and reservoir, distinguishing the two states by thresholding the tunneling signature in panel a.ii in the time domain [100, 101].

The main limitation of this technique comes from the finite Fermi width, which is broadened according to the Fermi–Dirac distribution [102], meaning that there is a finite probability for the $|\uparrow\rangle$ electron to tunnel to the reservoir resulting in readout errors. Typically the reservoir temperature is higher than the refrigerator base temperature due to electron-phonon decoupling at milliKelvin temperatures. This mechanism is typically the dominant contribution to readout error when the Zeeman splitting is not much larger than the thermal broadening $\sim k_B T$ [103], which means high magnetic fields of the order 1 Tesla (with corresponding transition frequencies $>$10 GHz) are required to minimise errors. High fidelity readout is prohibitively hard to achieve at temperatures $\sim$1 K [54, 101, 104].

4.1.2. Qubit spin with ancilla spin: Pauli Spin Blockade (PSB). The second main spin-to-charge conversion technique used to perform spin readout uses an ancilla QD adjacent to the qubit, rather than a reservoir, as illustrated in figure 2(b). The ancilla dot is initialised with a single spin in the low-energy $|\uparrow\rangle$ state. Then assuming a non-zero exchange interaction between the

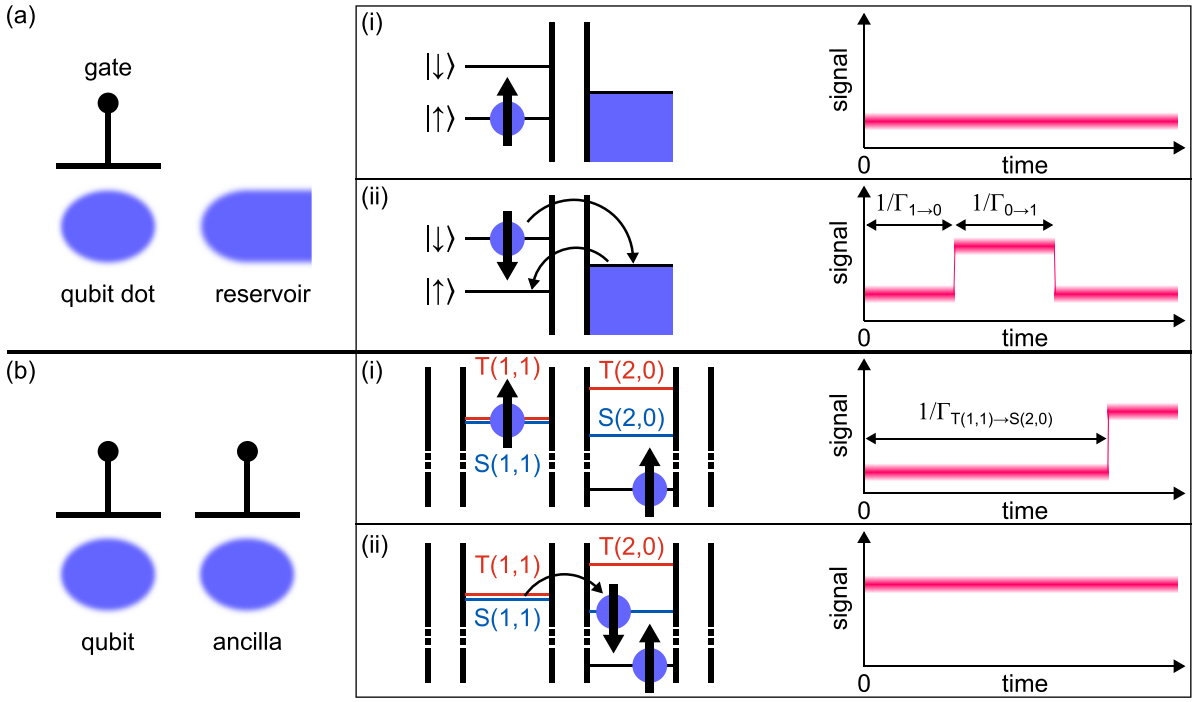

Figure 2. Spin-to-charge conversion protocols. (a) Energy filtering involves a reservoir situated close to the QD to be read. Panels (i) and (ii) illustrate energy diagrams and the expected readout signal for the spin $|\uparrow\rangle$ and $|\downarrow\rangle$ states respectively, showing that, for the $|\uparrow\rangle$ state, the system is blockaded and no change in the sensor signal is detected, whereas in the $|\downarrow\rangle$ state, the energy of the system is minimised by sequential emptying and re-filling of the dot with a $|\uparrow\rangle$ spin from the reservoir. The signal expected for this second case is a 'blip' with random duration related to the tunneling-in rate of the dot ($\Gamma_{0\to1}$), and a random delay time related to the tunneling-out rate ($\Gamma_{1\to0}$). (b) Pauli spin blockade requires a second 'ancilla' dot (with it is own gate) close enough to the qubit dot that there is a measurable exchange coupling between them. Together the pair of spins shared by the dots can form either a singlet or triplet state, denoted S and T respectively, and we specify the charge state of the double-dot system using the following numbers in brackets (here assuming a total of two electrons are contained in the system, though the technique can also be used in the multi-electron regime). The energy diagrams in panels (i) and (ii) illustrate that the triplet state is not energetically favourable in the (2,0) charge configuration, and thus no change in the signal is expected for the triplet state [panel (i)], until spin relaxation occurs. For the singlet state [panel (ii)], however, the system can immediately transfer to the (2,0) charge configuration, producing a change in the charge sensor signal (the signal illustrated here is expected when the inter-dot tunneling occurs faster than the sensor integration time).

two spins, the DQD system exists in one of four possible spin states: the singlet or one of three triplet states. In the singlet state (b.ii), the qubit spin can be moved adiabatically across into the ancilla QD by tuning the gate voltages to cause tunneling, however in a triplet state (b.i), the charge transition is blocked due to Pauli exclusion, until relaxation occurs or the excited triplet state becomes energetically accessible. This mechanism is known as Pauli spin blockade [105]. The typical signal traces illustrated on the right show the signal where tunneling in the singlet case occurs in a timescale much shorter than the resolution of the measurement. The ability to operate in this regime enables shorter measurement times than for energy filtering due to the large asymmetry in the singlet and triplet tunnel rates [106].

Pauli spin blockade avoids the temperature-related limitation of energy filtering: the reservoir temperature does not directly cause erroneous tunneling, and accordingly can been used at lower magnetic fields and higher temperatures [49]. Care must be taken, however, in placing the sensor to ensure that it is asymmetrically coupled to the qubit and ancilla dots, to prevent a net cancellation of the induced charge on the sensor.

4.2. The SET

The SET is illustrated in figure 3(a). A charged island, exhibiting Coulomb blockade, is connected to reservoirs either side by tunnel barriers, and is capacitively-coupled to a gate electrode for controlling the sensor dot potential [107]. The 'qubit dot' whose charge state is sensed by the current through the SET, is illustrated by the dot to the right of the SET labelled with a spin symbol, and is capacitively coupled to the SET. The black arrows indicate that current flows sequentially between reservoir-island-reservoir in one direction determined by the sign of V_{ds}. The readout signal is the current measured through the device, the source-drain current. In figure 3(a), the coaxial cable represents the connection to the external measurement equipment. Current flows through the SET when the sensor electrochemical potential is aligned between the reservoir Fermi levels, which is achieved by tuning the gate voltage, V_{gs}. Charge transitions in the qubit dot affect the potential of the sensor dot via their mutual capacitance, which translates into a measurable change in the current. To maximise the readout sensitivity, V_{gs} should be fine-tuned to a point of maximum transconductance, dI_{ds}/dV_{gs}, in the case of small

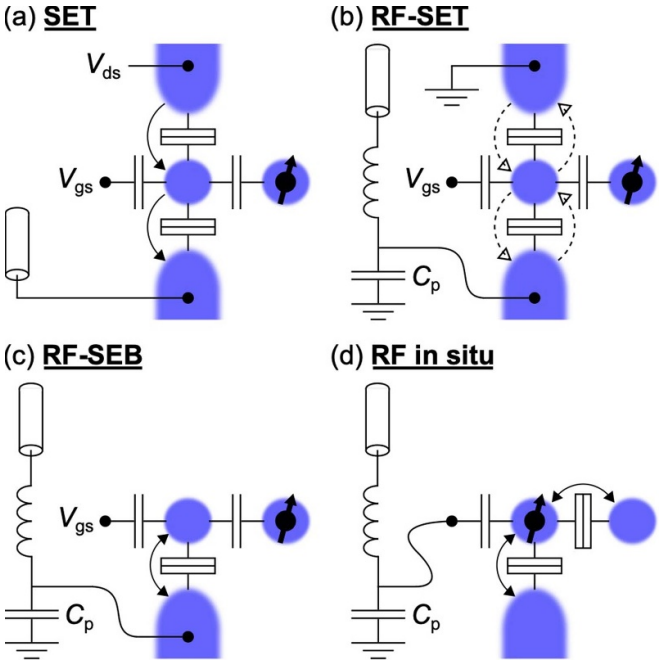

Figure 3. Summary of different charge sensors. (a) The SET, formed by a gated island of charge between two reservoirs. The gate voltage, V_{gs} must be tuned to a region where Coulomb blockade is lifted, and bias voltage V_{ds} is applied causing charges to tunnel sequentially between reservoirs via the island, as indicated by the black arrows. The tunneling current is measured using external equipment (not shown) through the illustrated coaxial line. The QD containing the qubit to be read, labelled with a black spin symbol, must be close enough to the SET island such that changes in the charge of the qubit dot modulate the potential of the island via their mutual capacitance, thereby modulating the sensor current. (b) The radio-frequency SET (RF-SET), created by attaching an impedance-matching network (resonator) to a reservoir of the SET. One must also take into account the parasitic capacitance, C_p, of the setup. A RF probe tone is applied through the coaxial line, causing the current between the reservoirs to change sign periodically, as indicated by the black dashed arrows. The sensor is measured by analysis of the phase and magnitude of the reflected RF signal, which depend on the resistance between reservoirs. This resistance is modulated by changes in the qubit dot, similarly to the SET. (c) The radio-frequency single-electron box (RF-SEB) has a similar form to the RF-SET, but only requires one reservoir. This is because changes in the capacitance of the sensor, rather than resistance, generate the signal. The capacitance associated with a single charge transition between island and reservoir is probed cyclically, as indicated by the double-ended arrow. (d) RF *In Situ* sensing—this technique probes changes in the device capacitance associated with charge transitions of the qubit dot itself, by connecting the resonator to the corresponding gate. Such transitions may be transfer of charge with a reservoir or another dot, as indicated by the black arrows.

induced voltage shifts. If the induced voltage shift is larger than a linewidth, the sensor should be biased to the current maximum of the Coulomb oscillation.

Single-gate transistors with lateral dimensions between 10–100 nm, produced in commercial foundries, can form charged islands when cooled, and exhibit the periodic conductance peaks characteristic of SETs [108, 109]. However, integrating SETs in close proximity to qubits to perform charge sensing, similarly to the experiments on university-cleanroom devices (for example [110, 111]), is a significant challenge under foundry constraints. Recently, experiments with industry-compatible devices have succeeded in demonstrating integration of an SET with multi-QD devices. Two examples, the silicon-on-insulator (SOI) nanowire FET [112] and the other based on FinFET technology [113], approach this challenge similarly, by fabricating two parallel channels where one is used to form the qubit dots and the other an SET sensor. The spacing between the channels was minimised within the constraints of lithography to 120 nm, to maximise the mutual capacitance between qubit and sensor dots, while the nanowire FET device used floating gates to further enhance this capacitance [112]. Another approach demonstrated with the nanowire FET technology is to implement a SET in the same channel as the qubit dots, which is enabled by splitting the gates along the length of the channel so that the potentials of the SET and qubit dots can be varied independently [114]. A single split-gate device was used to perform single-shot spin readout with the energy-filtering technique in 1 ms with a 92% fidelity [115]. Relatively wide (90–110 nm) channels were used in order to minimise tunneling between the DQD and the SET. Creating a split-gate with a gap of 40 nm [114] can only be achieved today by incorporating an electron-beam lithography step in the fabrication process. The third approach, pioneered by imec, improved the fabrication flexibility by developing a 300 mm electron-beam lithography process [116], yielding highly tunable SET sensors with low charge noise $<1\ \mu\text{eV}/\sqrt{\text{Hz}}$ at 1 Hz [117].

The main limitation of the SET sensor to date has been a relatively small measurement bandwidth, in comparison with spin dephasing rates in silicon, which can be up to 1 MHz [35, 37, 118–120]. The bandwidth of the SET is limited by the RC constant of the low-pass filter formed by the resistance of the tunnel barriers—being at least the resistance quantum (25.6 kΩ) — and the parasitic capacitance at the output. The broadband coaxial cable that carries the current from the SET to the measurement equipment at room temperature (RT) has a typical capacitance to ground ∼0.1 nF per metre, which shunts the parasitic capacitance of the SET and therefore reduces the bandwidth to tens of kilohertz [121]. A cryogenic transimpedance amplifier (TIA) could be used to avoid the issue by converting the current signal into voltage [122], however the TIA would need to be situated within millimetres of the SET, operating at mK temperatures [123, 124] in order to reach MHz bandwidths. The challenge with this approach is designing an amplifier compatible with the limited cooling power available below 100 mK, typically on the order of 100 μW [125]. The development of amplifiers with minimised power dissipation per unit gain, and investigations into the effects of placing them close to quantum hardware is an ongoing effort [126–129], with one demonstration of charge state readout achieving 99.9% fidelity in an integration time of 6 μs [130]. The state of the art for spin readout with the SET is 99.56% in 670 μs (Elzerman spin-to-charge conversion), using two separate HEMT amplifiers at the 1 K and 4 K stages of the refrigerator [131].

The SET has been used for PSB spin readout at elevated temperatures $\sim$1 K, though the readout fidelity drops significantly compared to mK temperatures [132], with one example falling from 99.9% fidelity at 40 mK to 80% at 1.5 K [54]. This is due to thermal broadening of the reservoirs reducing the maximum transconductance of the current peak, thereby reducing the signal contrast between the different charge states of the qubit dot. The issue has recently been addressed, however, by the demonstration of a double-island SET which adds an additional island between the two reservoirs [133]. Then the current can only flow through the sensor by passing sequentially between the two dots, permissible only when the potentials of the two dots (which are not subjected to the same broadening as the reservoirs) are aligned.

4.3. The radio-frequency SET

The radio-frequency SET (rf-SET) was developed to overcome the bandwidth limitations of the SET, by switching from a measurement of the source-drain current to measurement of the dissipated power at radio-frequencies [134]. As shown in figure 3(b), the rf-SET is implemented by connecting an inductor to one of the reservoirs of the SET, forming, in combination with the parasitic capacitance, a L-shape matching network. The objective of the matching network is to transform the high impedance of the SET down to 50 Ω, the more common impedance of high frequency transmission lines and by doing so, removing the impact of the cabling parasitic capacitance. Furthermore, the rf-SET can be used in conjunction with high-frequency low-noise cryogenic amplifiers to reduce the noise of the measurement down to a few Kelvin.

Impedance matching of the resonator to the 50 Ω input line is important to ensure maximal power transfer to the device [135, 136]. The second factor to consider in terms of circuit design is that the sensitivity is proportional to the fractional change in resistance, that is, the change in resistance divided by the total series resistance in the sensor. Therefore, the response to a charge transition is maximised if the total series resistance in the sensor is minimised. For a more in-depth review of sensing with the rf-SET, and the other rf sensors below, see [137].

Demonstration of remote sensing of QDs with an rf-SET has not yet been reported in industry-compatible devices. This is likely due to the combination of challenges including fabrication complexity discussed in the previous section, with achieving low contact resistance and developing the high-frequency circuitry. Dispersive readout techniques, discussed in the next section, have been used extensively by comparison to measure arrays of quantum dots, by tackling the last two challenges. Given the recent progress in integration of SETs with QDs covered in the previous section, remote sensing using rf-SETs may be demonstrated soon. In the wider field of silicon quantum electronics, the rf-SET is a well-proven approach to performing high-fidelity readout, with a state of the art spin readout fidelity above 99% in 1.8 μs, achieved with the PSB technique in SiGe heterostructure devices [138, 139].

4.4. Dispersive Readout

4.4.1. Sensing changes in capacitance. Dispersive readout also uses a radio-frequency resonator connected to the nanoscale device, however is distinct from the rf-SET in that the resonator responds primarily to changes in capacitance associated with charge transitions, rather than resistance. Where changes in resistance modify the damping of the resonator, changes in capacitance produce a shift in the resonant frequency. Such changes in capacitance have been described in [140, 141], that are separated into the quantum capacitance and tunneling capacitance. Quantum capacitance is produced by a charge transition when the resonant frequency is smaller than the characteristic tunnel coupling for that transition, i.e. the transition occurs adiabatically and the electron transfer happens elastically with the oscillating electric field in the resonator. Tunneling capacitance is associated with inelastic tunneling, which occurs when the system relaxes after non-adiabatic evolution caused by driving the transition at frequencies comparable to or above the tunnel coupling [142, 143]. Non-adiabatic driving can add noise to the measurement [31, 144]. Ideally, adiabatic driving (quantum capacitance) should be the main source of the readout signal, and the resonator frequency sets a lower limit for the tunnel rate that can be sensed with dispersive readout. Two distinct approaches have so far been used to exploit quantum capacitance for charge sensing: the rf single-electron box (rf-SEB), and *in-situ* dispersive readout.

Note that although the resonators illustrated in figures 3(b)–(d) are formed by an inductor connected in series between the input line and the device, other resonator circuits have been used. For example, placing the inductor in parallel with C_p and using a coupling capacitor to decouple from the input line has been a particularly successful approach in dispersive readout, as it allows impedance matching at any resonant frequency by the co-selection of the inductance and coupling capacitance [95]. While impedance matching is as important in dispersive sensing as it is for the rf-SET to maximise power transfer to the device , there are other circuit-design considerations which differ for the two sensing types [31, 145]. Firstly, the signal strength in dispersive sensing is proportional to the fractional change in capacitance, mirroring the dependence of the rf-SET signal on the fractional change in resistance. To enhance the fractional change in capacitance, the total shunt capacitance of the resonator, dominated by the parasitic capacitance C_p, should be minimised, which is equivalent to maximising the characteristic impedance of the resonator. Also, the change in capacitance can be improved by maximising the lever arm, $\alpha_\mathrm{e} = C_\mathrm{e}/C_\Sigma$ where C_e is the capacitance between the resonator-coupled electrode and the dot, and C_Σ is the sum of the capacitances connected to the dot. The second main difference is that the internal damping of the resonator should be minimised, i.e. the internal quality factor should be maximised. Finally, increasing the resonant frequency can lead to improved signal, though

this is only provided that the frequency is still significantly less than the tunnel rate.

4.4.2. The rf-SEB. The rf-SEB, illustrated in figure 3(c), has several similarities with the rf-SET, but one key advantage is that only one reservoir is required. An auxiliary dot, the SEB, is formed using an additional gate, close to the qubit dot. The double-ended arrow indicates that the sensor is biased via the gate voltage to a charge transition between the SEB and reservoir, and the oscillating electric field generated by the resonator causes cyclical tunneling that gives rise to a finite quantum capacitance. Changes in the occupancy of the qubit dot affect the potential of the SEB dot via the mutual capacitance, thereby shifting the SEB transition and altering the signal reflected by the resonator. The diagram shows the resonator connected to the reservoir, where the quantum capacitance can be detected via the capacitance of the tunnel barrier, however it is similarly effective to connect the resonator to the gate electrode for detection via the gate. In some literature the rf-SEB is referred to as a single-lead QD (SLQD) [146, 147].

The rf-SEB has recently proved a very effective way to detect charge transitions of a qubit dot in the few-electron regime in foundry-compatible devices [56, 106, 114, 148–152]. The tunnel rates in the few-electron regime can be smaller than the GHz tunnel rates in the many-electron regime [112], in which case tunneling does not occur on the timescale of the rf period, and therefore no signal is detected. The above references, however, populate the SEB with 5-12 electrons to increase the SEB tunnel rate to generate a large signal, which is then modulated by charge transitions of the qubit dot due to the capacitive shift of the SEB potential. This methodology allows transitions with small tunnel rates between sensed dots to be detected. All of these report experiments performed in the same group of nanowire devices produced by CEA Leti, and all (except [152]) connect the resonator to a gate, benefiting from the large gate lever arms (up to 0.5) of the wrap-around gate structure. In terms of spin readout, both Elzerman [149] and PSB [56, 152] readout have been performed, with a maximum fidelity of 99.5% in a time window of 250 μs for the former and a fidelity of 99.2% in 5.6 μs for the latter, both reported in [106]. In the same experiment, the PSB spin readout fidelity was found to decrease to 94% in 27 μs with the refrigerator temperature raised to 1 K, which is attributed mainly to broadening of the SEB transition due to the increased temperature in the reservoir. Finally, it has been demonstrated that floating gates spanning $\sim$100 nm gaps between QDs can boost their mutual capacitive coupling, enabling readout over greater distances with the rf-SEB [148] (and SET [112]).

4.4.3. In-situ *dispersive readout.* *In-situ* dispersive readout is the simplest in terms of the nanoscale patterning and thereby would allow the highest density of qubit integration. This is because no reservoirs, dots, or gates additional to those needed by the qubits themselves are required. The resonator is connected to the qubit dot via a gate electrode, and charge transitions modulate the quantum capacitance seen by the resonator, producing a shift in the resonant frequency. The double-ended black arrows in figure 3(d) indicate that both dot-reservoir and inter-dot transitions can be detected. However, the ability to sense inter-dot transitions without any reservoir is particularly valuable, to avoid the temperature-broadening issues that limit the fidelity of other sensors at temperatures $\sim$1 K [54, 106, 132]. Besides, it is not feasible to read a single spin qubit by combining *in-situ* sensing and Elzerman spin-to-charge conversion with a nearby reservoir. This is because the Elzerman technique re-initializes the qubit in the $|\uparrow\rangle$ state after a single tunneling sequence, while the quantum capacitance signal is generated by repeated tunneling caused by the rf tone that is measured over some integration time. When detecting inter-dot transitions with *in-situ* readout, the signal strength depends on the difference between the lever arms between the gate and each of the dots involved in the charge transfer [140, 141], therefore it is important that the gate connected to the resonator has significantly different lever arms to the two dots.

In-situ dispersive sensing has been a valuable tool for investigating QDs and dopants in foundry-compatible single-gate transistors [24, 31, 96, 143, 153, 154], enabling charge sensing in regimes where the current through the channel is not measurable. In double-quantum-dot systems, PSB readout has been demonstrated of electron spins [155] and hole spins [156], and also in dot-dopant systems, readout of electron spins [24] and hole spins [153]. In each of these experiments, however, averaging over many attempts was used to improve the signal-to-noise ratio. High-fidelity spin readout with *in-situ* charge sensing is yet to be performed in foundry-compatible devices. Recently, the sensitivity has been greatly improved by switching to parallel resonators containing superconducting inductors [95], increasing the resonant frequency [57], and using quantum-limited amplification [96], though one obstacle remains. The tunnel couplings in the few-electron regime have been too small to enable tunneling in phase due to the rf oscillations, and instead experiments have been performed at higher charge occupancy, to increase the tunnel rates and where complex higher-order spin states have been observed [157, 158], and spin T_1 times are typically shorter. Spin readout at the single-electron level has, however, been demonstrated with *in-situ* dispersive sensing in a Si/SiGe heterostructure device [98], achieving a fidelity of 98% in 6 μs (where the inter-dot tunnel coupling was estimated at 2 GHz). To progress with foundry-compatible devices, there are two possible paths forward: either the inter-dot tunnel coupling must be increased, which is essentially a fabrication challenge to reduce the gate pitch and/or implement barrier gates (BG); or the spin physics of high-occupancy QDs should be studied in more detail with the aim of obtaining well-defined spin states with long relaxation and coherence times.

Overall, rf-SETs have provided an easier to use method and demonstrated the highest fidelity primarily due to the ease in achieving large fractional resistance changes compared to capacitance changes. However, their larger footprint (2 reservoirs) when compared to rf-SEBs (1 reservoir) and *in-situ* dispersive methods (no reservoir) compromise

their placement in highly connected qubit architectures. Furthermore, recent studies indicate that dispersive readout methods could become even more sensitive than rf-SETs with the appropriate resonator design (high Q, impedance and frequency) [106], pointing towards dispersive readout methods as a more scalable readout solution.

Although rf readout methods provide state-of-the-art readout fidelity, they suffer from a footprint drawback. The main limitation with using rf resonators in general is their size relative to the qubits—while the QDs are 10 s of nanometres, the resonators are typically 0.1–1 millimetres. This large size mismatch presents significant challenges for scaling up. Time multiplexing could help to alleviate this issue [159].

5. Fabrication of silicon qubits

5.1. General structural variations

The ultimate goal of fabricating nanodevices suitable for hosting spin qubits requires exquisite control of the electrostatic landscape within the silicon crystal, the ability to displace single charge carriers, controlling their energy levels and interactions at will. The different ways of creating wells and barriers (confinement), introducing or evacuating charge carriers (from and to reservoirs) can be combined on various substrate types.

5.1.1. Confinement

5.1.1.1. Field-effect gates. Prior to populating it with a small number of elementary charges, one has to electrostatically define a zero-dimensional potential well, with characteristic dimensions on the order of the Fermi wavelength to induce a discrete energy spectrum akin to the orbitals of an artificial atom.

This is most commonly achieved by means of MOS or Schottky field-effect gates patterned above the active layer, granting the ability to either accumulate or deplete charge carriers underneath. A strong z-confinement may hence be obtained by applying a voltage of opposite polarity to the charge carriers, whereas the x- and y-confinements correlate to the projected patterns of the various gate electrodes biased either in accumulation or depletion mode. Notably though more seldom, coplanar metallic electrodes obtained by highly doping the active layer (in the same way as charge reservoirs) may also be used to shape or control the potential of nearby QDs [160, 161].

5.1.1.2. Dopants. A single or a few isolated and ionized dopants within the active layer can create a deep and sharp well, with certain functional advantages. For instance, the energy spacing between the orbitals of the artificial atom are conveniently large. In addition, this configuration lends itself to qubit proposals based on coupling the spin of a bound electron to a nuclear spin, which can be that of the dopant [77]. We note however that not only are Gates still needed, but their precise alignment to the dot-defining atoms is critical. While self-aligned doping techniques are well-known, the ability to deterministically place an ideally centered dopant or dopant cluster at a given depth below a gate is an extremely challenging endeavour. In fact, combining Scanning Tunneling Microscopy-based lithography with *in-situ* epitaxial growth of silicon and phosphorus has led to atomic-level dimensional control [160–162], yet with the main drawback of a much reduced throughput.

5.1.2. Reservoirs definition

5.1.2.1. Blanket reservoirs. Reservoirs, or leads, are needed to provide charge carriers to the QDs, and can in some cases enable spin-to-charge conversion through energy-selective charge tunneling. In some device architectures, a planar heterojunction structure in combination with a carrier supply layer obtained by modulation- or delta-doping leads to the formation of a blanket 2DEG (or 2DHG). Depletion Gates are then used to isolate dots from the reservoir regions (see figure 4, top). While this approach is common in AlGaAs/GaAs systems, Si/SiGe heterostructures are usually undoped and require top gating to accumulate charge carriers [19, 163].

5.1.2.2. Localized reservoirs. Alternately, the leads may be delimited by mask-defined or self-aligned dopant implantation of the active layer (see figure 4, middle and bottom). Accumulation gates are often used to electrostatically extend the metallic region to the vicinity of the qubit-hosting QDs, thus enabling loading and unloading. Note that self-aligning the leads to the gates in a transistor-inspired process sequence [46, 164] advantageously reduces the gate count, yet it sacrifices a degree of freedom (control of the dot-lead coupling) while the diffusion of stray dopants close to the QD can become a concern.

5.1.3. Substrate

5.1.3.1. Unpatterned substrate. This is perhaps the most common configuration [29, 163, 165, 166]. Both accumulation and depletion gates are needed to simultaneously define and tune the potential of the QDs, the extent of the reservoirs and the permeability of the barriers separating them. Due to the lateral gate dimensions required for optimal functionality (see 6.2.1), an extreme precision of patterning would be required for single-level definition, and in practice multiple layers of overlapping Gates are often defined.

5.1.3.2. Patterned substrate. Masked etching of the active region can be a way of structurally assisting confinement along one direction without resorting to depletion Gates (see figure 4, bottom), as is the case of the nanowire [46, 164] or the FinFET [49, 167, 168] designs. Besides reducing the gate count, this choice can affect qubit performance negatively or

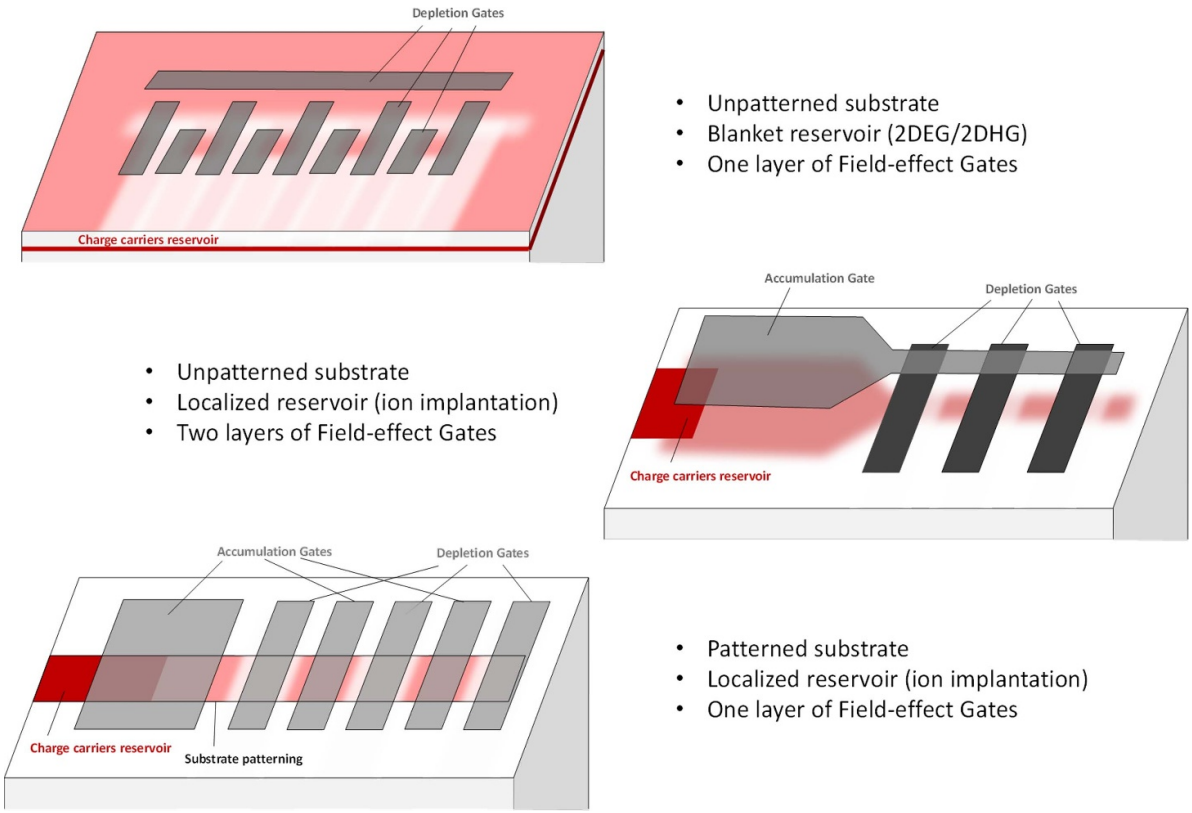

Figure 4. Examples of coupled QDs formed in semiconductors Three possible instances of building block combinations (structural confinement, reservoirs, Gates) to achieve the formation of coupled QDs.

positively. On the one hand, localizing and moving charges across non-planar structures increases the risk of exposing the qubit to a more inhomogeneous environment with rougher interfaces and defect-containing deposited dielectrics, which may negatively affect its coherence. On the other hand, a rupture of symmetry in the confinement geometry can be desirable in some cases, as the resulting anisotropy (e.g. on the g-factor) [169, 170] can be leveraged for facilitating all-electrical qubit manipulation [48]. Some device geometries combine patterned active areas with additional gates whose purpose is to push and pull the QD against and away from interfaces, using tunable symmetry breaking to balance coherence time and manipulation speed [46, 171].

5.1.3.3. Silicon-On-Insulator (SOI). In CMOS devices, the Fully-Depleted SOI technology is notable for the added possibility of modulating the conduction channel by two independent MOS gates, the second one being located below the active area, with the buried oxide (BOx) acting as gate dielectric. These back-gates can be localized, typically by masked dopant implantation of the handle substrate surface through the channel and BOx. In the frame of spin qubits, this configuration can be advantageously leveraged to either efficiently decouple accumulation and depletion gates (one type for either top or bottom interface), or achieve a finer control of vertical confinement—thus greatly facilitating the tuning strategy described in the previous paragraph.

5.1.3.4. Isotopic purification. Hyperfine interactions with nuclear spins in the host crystal can limit the coherence time of an electron spin qubit. The most abundant Si isotope (^{28}Si: 92.23%) carries no nuclear spin, but ^{29}Si (4.67%) does. Increasing the relative ^{28}Si content by has led to some of the best performing single and two-qubit gates [166, 172]. Bulk ^{28}Si substrates are rare, but a ^{28}Si epilayer can be grown on top of a natural silicon (^{nat}Si) seed using isotopically purified silane-based precursors to form the active layer [167, 173–175]. However, the diffusion of ^{29}Si in provenance of natural Si or SiO_2 layers towards the volumes of charge confinement should be avoided during the subsequent fabrication steps. Experiments [175] tracking the ^{29}Si concentration depth profile in ^{28}Si/^{nat}Si/^{28}Si stacks and its diffusion for various annealing conditions indicated that special attention must be paid for thermal budgets exceeding a few minutes at 925°C (*e.g* thermal oxidation, dopant activation or wafer bonding).

5.1.3.5. Si/SiGe stack. Since charge confinement against an amorphous dielectric may be detrimental in terms of qubit exposure to disorder, an alternative approach consists in capping the active silicon with a crystalline material having sufficient a band offset to create vertical confinement, and a minimal lattice mismatch in order to limit the emergence of defects cause plastic strain relaxation. Such a configuration arises for at the interface between tensily strained silicon and a lattice-matched SiGe cap of moderate germanium content

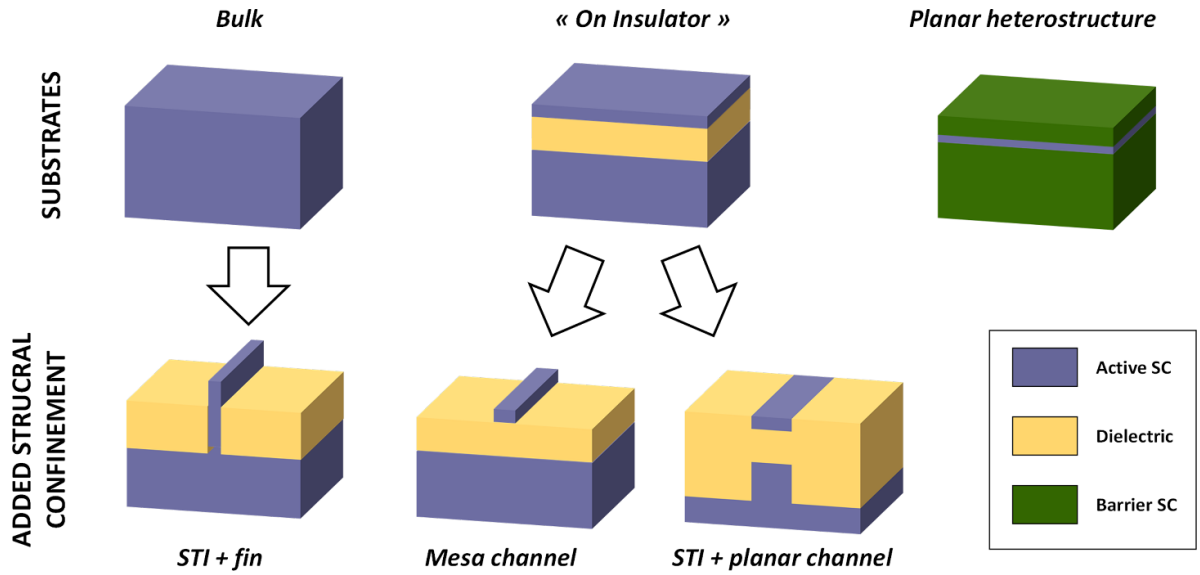

Figure 5. Types of substrates for structural confinement Simplified cross-sections for various unpatterned and patterned substrates. STI stands for Shallow Trench Isolation. Patterning planar heterostructures (e.g. SiGe/Si/SiGe) is generally avoided as it would lead to stress relaxation and defects in the active layer.

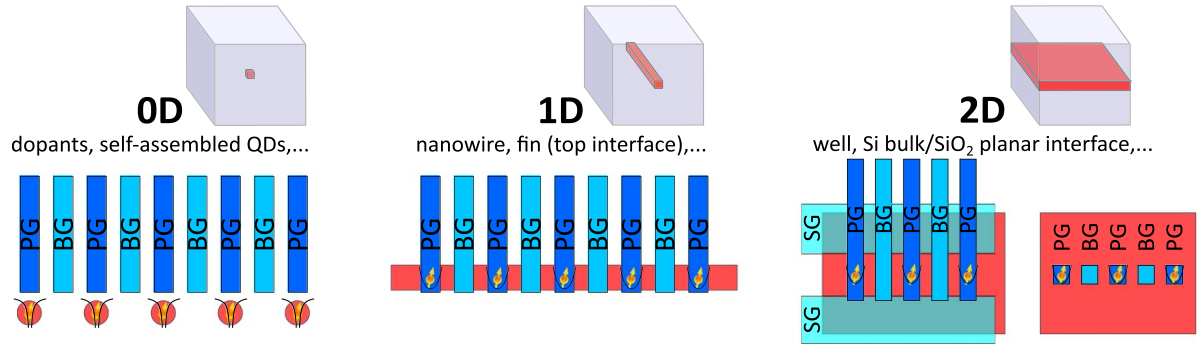

Figure 6. Gates placement depending on different levels of structural confinement. Green areas represent the confinement geometry obtained by various means of combining substrates and dopants. PG in dark blue symbolize Plunger Gates, the electrodes controlling the electrostatic potential of the dot. BG in light blue represent BG, controlling the coupling between dots. SG in cyan stand for Side Gates. They are typically overlapped with BG and PG and can be used in depletion or accumulation to electrostatically assist structural confinement. In the case of native 0D confinement, e.g. single dopants in silicon, a challenge is their precise positioning in a regular array. In 1D structures, such as nanowires or fins, QDs can be created at the intersection of electrostatic gates and the 1D active layer, relaxing the alignment constraints between the different elements. 2D structural confinement reduces the number of interfaces, but it usually implies a more complex gate integration, either relying on the superposition of multiple gate layers (e.g. use of Side Gates) or ultimately the fabrication of dot-shaped gate arrays [75, 178].

(molar fraction typically around 0.3) [176]. An underlying strain-relaxed graded buffer of SiGe is grown to set the lattice parameter, and the tensile Si quantum well layer is usually in the 10 nm range, which is well below the critical thickness. Notably, this type of substrate was used in the very recent demonstration of a six-qubit processor in silicon [41], and is now being evaluated in parallel with Si MOS in advanced fabrication facilities [177].

Figure 5 shows the main types of unpatterned substrates, and several ways patterning them can provide added structural confinement. Figure 6, a more abstract generalization of figure 4, illustrates how Gate electrodes can be placed in order to control the potential and mutual couplings of QDs for various levels of structural confinement.

5.2. *Functional impact of technological processes*

Successfully transitioning from lab to fab will require translating the general structural variations described in the previous part into foundry-compatible integration schemes, specifying process control targets based on the impact of each step on key qubit characteristics, which themselves need to be defined and automatically monitored. Foundry-compatible integration may be loosely defined as a sequence of process steps that can be transferred to an industrial-grade processing line while minimally impacting its global yield and throughput. In the following, we narrow the scope of the review to recent results on MOS-Gated QDs in silicon-based substrates.

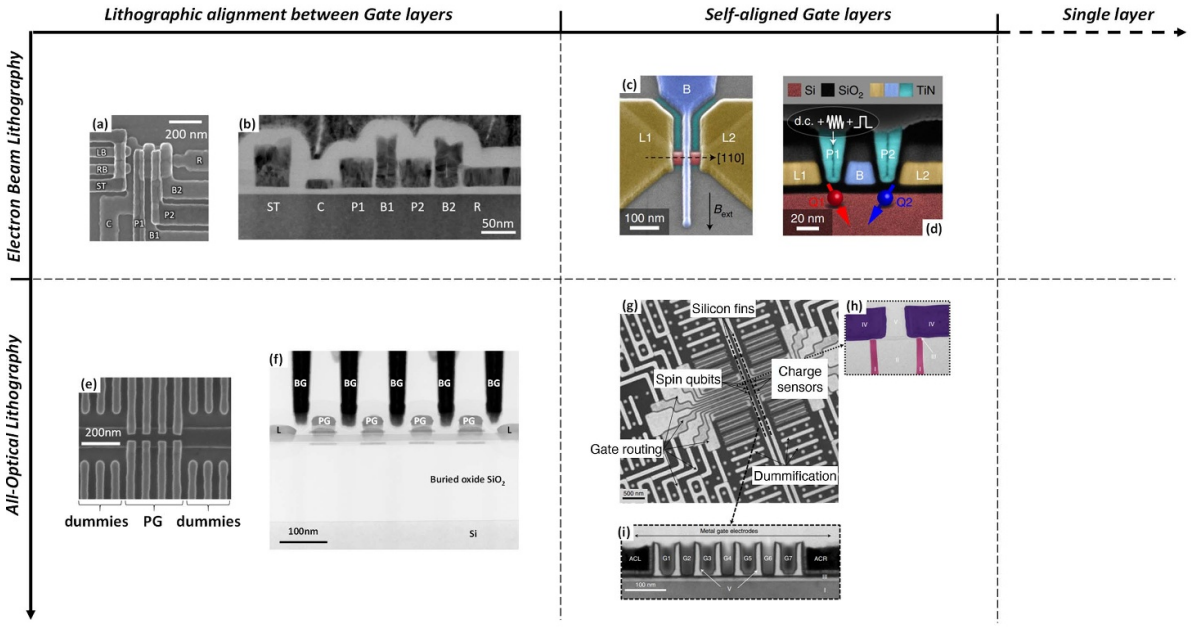

Figure 7. Examples of Si MOS QD prototyping platforms and corresponding Gate patterning strategies. (a) and (b) imec: three mutually-aligned, EBL-defined Gate levels on unpatterned substrate. ((a) and (b)) © [2020] IEEE. Reprinted, with permission, from [179]. (c) and (d) IBM Research: Si fins are patterned using EBL. Barrier and Lead Gates are defined on the same E-Beam layer, Plunger Gates are then formed by a self-aligned process. ((c) and (d)) Reproduced from [49], with permission from Springer Nature. - (e) and (f) CEA-Leti [183]: Si mesas are patterned by optical lithography on an SOI substrate. Two levels of mutually-aligned iDUV Gate levels are then formed. (g)–(i) Intel: Si Fins are patterned using optical lithography, followed by a Shallow Trench Isolation process. A first layer of (even-numbered) Gates is defined by iDUV lithography and a replacement metal gate process. The second layer of (odd-numbered) Gates is formed in the remaining space after masked selective removal of a planarized encapsulation oxide. ((g)–(i)) Reproduced from [168]. CC BY 4.0 Results obtained on devices with a single layer of optical EUV lithography-defined Plunger and BG are also published in [178] (no pictures shown).

5.2.1. Dimensional control and density. For practical purposes, the spacing between orbital energies of the artificial atom formed by the QD should be much larger than the thermal energy kT (for example, 1meV is about 12kT at T = 1 K and hence a reasonable target). Given the relatively large effective masses in silicon, this means that the characteristic length of Plunger Gates (PG) should be a few tens of nm, which by itself is well in the range of achievable feature sizes in advanced Front-End-Of-Line processes. In the widely adopted nearest-neighbor architecture however, adjacent QDs are separated by and coupled through tunnel barriers, themselves preferably tunable and directly controlled by BG. Therefore, not only should the PG pitch be in the range of 100 nm or less, but the PG spacings should also be filled with interdigited BG with same pitch. These density requirements are very strenuous, even by today's industrial standards. Current state-of-the-art prototypes often resort to multiple advanced lithography steps, and sometimes rely on self-alignment, thereby eliminating the die-to-die variability related to uncontrolled shifts between successively exposed patterns. Below is a brief review of the most recent high-density demonstrations achieved on the more foundry-friendly integration routes.

Bulk Si MOS devices from imec [179, 180] feature three levels of e-beam lithography (EBL)-defined Gates (no self-alignment), and can be described as an adaptation of the approach in [29] to a 300 mm processing line (figures 7(a) and (b)). The substrate being unpatterned natural silicon with local doping, one layer of accumulation Gates is dedicated to extending the remote charge reservoirs to the vicinity of the QD. PG and BG are materialized by two superimposed Gate layers which are mutually insulated by a thin dielectric (5 nm SiO_2). A pitch of roughly 65 nm is obtained with EBL, leading to effective BG and PG lengths of about 25-30 nm.

FinFET-like devices studied in collaborative work between the University of Basel and IBM Research [49, 181] propose a self-aligned process for defining the PG (figures 7(c) and (d)). Leads and BG are first defined using the same EBL level on top of fins patterned in bulk natural silicon, before being covered by ALD-deposited silicon dioxide. PG are then defined by merging conductive spacers in the gaps left between the leads/BG, thus reaching a high density with 15 nm length and 45 nm spacing (60 nm pitch).

The devices fabricated at CEA-Leti on 300 mm wafers are similar to planar SOI MOSFETs. In a first generation [164], active areas are mesa-patterned nanowires of natural silicon. A single EBL level is used to define PG with a 65 nm pitch, and the reservoirs result from self-aligned doping masked by silicon nitride spacers wide enough to mask the spacings between PG. Instead of BG, the SOI back-Gate was used to control inter-dot coupling. In a main design variation, sensor QDs could also be defined along the opposite edge of the same

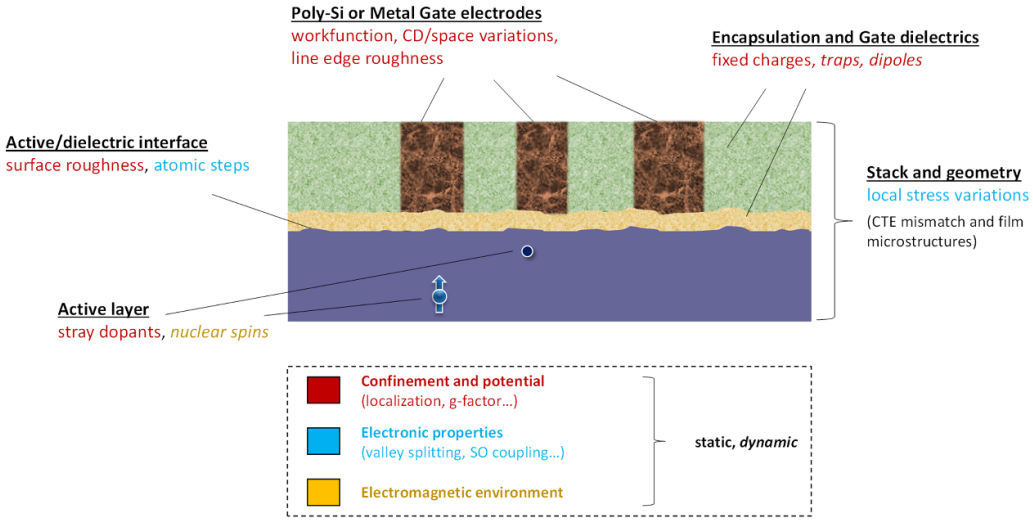

Figure 8. Sources of static and dynamic noise in Gate-defined Si QDs. Schematic cross-sectional view of a Gate-defined Si QD device. For each of the main building blocks, sources of process-induced variability are listed, and categorized according to the way they could affect basic characteristics of the QD.

mesa thanks to the split-gate geometry [182]. In more recent demonstrations [183], immersion Deep Ultra Violet (iDUV) optical lithography is used for defining PG, while the BG are formed through a subsequently aligned trench contacts-like level (with incomplete etching). In this version, the plunger-barrier gate pitch is 80 nm (figures 7(e) and (f)).

Devices akin to FinFETs are also made by Intel on isotopically-purified 300 mm Si substrates (epi-layer of ^{28}Si). Charge sensors can be hosted in capacitively coupled adjacent fins (fin spacing: 120 nm). In a first generation [167, 168], the lead and plungers Gates are optically defined by iDUV. In contrast with [183] though, the BG are self-aligned (figures 7(g), (h) and (i)). The plunger-barrier pitch is around 100 nm (PG and BG are around 25 nm long and separated by 25 nm dielectric spacers). The latest publications [177, 178] announce a plunger-barrier pitch scaled down to 50 nm using a single pass of Extreme Ultra Violet (EUV) lithography. Two versions of these devices are investigated in parallel, one with a Si MOS confinement, the other in the Si/SiGe quantum well configuration. Interestingly, this latter approach seems to be currently leading in terms of single-qubit gate fidelity [178].

Certainly, the control of critical dimensions, density and inter-layer alignment is not the only aspect of processing that can significantly impact the performance, coherence and reproducibility of Si qubits, as will be commented in the next paragraph and illustrated in figure 8.

5.2.2. Sources of static and dynamic disorder

5.2.2.1. Larmor frequency. Qubit rotations are carried out by resonant manipulation. It is hence critical to efficient addressing and fast operation that the Larmor frequency should be accurately predicted, with small device-to-device dispersion, and stable over time. The g-factor, being roughly speaking linked to the shape of the confinement potential, is quite sensitive to static (interface states, point defects) and dynamic (charge trapping/detrapping, dipole switching) electrostatic disorder. This warrants particular caution with process features such as dopant implantation and diffusion, presence of sub-stoichiometric dielectric layers in the vicinity of the confinement volume, interface or line edge roughness.

The other component, i.e. the static magnetic field as perceived by the qubit, may also vary between nominally identical devices due to uncontrolled dimensional variations in the stripline or micromagnet design, as well as the presence of dopant or Si isotopes carrying a non-zero nuclear spin (such as ^{31}P or ^{29}Si).

5.2.2.2. Energy spectrum and valley states. We mentioned earlier the need for separation between orbitals to be larger than the thermal energy. In the case of electron spin qubits in Si, the fact that the conduction band contains six valleys further adds complexity to the spectrum [184], and sets valley splitting as the critical energy scale [185, 186]. While inter-valley coupling may sometimes be leveraged for electrical spin manipulation schemes [171], in the general case a large splitting between the two lowest-lying valleys is desired, which can be robust against variability caused by local strains. Strong vertical confinements are associated to larger splittings, which tends to be the case in Si MOS configurations as compared to Si/SiGe quantum wells [187], where the Gates are more remote.

5.2.3. Figures of merit and device monitoring techniques. We gave qualitative indications of some impactful morphological and electrical parameters. Figures of merit (FoM) have yet to be specified to enable monitoring. As of yet, they are typically inherited from characterization techniques developed for devices operating at RT and larger charge density, and provide a somewhat indirect measure of the phenomenon to observe. Defining quantitative targets is no easy task either,

since requirements would vary according to the qubit flavor, as well as architecture-level choices.

Hall mobility is often used in the literature as FoM for the smoothness of the electrostatic potential landscape [51]. The intuition is a large low-field mobility is representative of reduced Coulomb scattering, hinting at a lesser electrostatic disorder. Extracting a percolation density provides a more direct metrics [188], since it describes the carrier density above which charge trapping no longer prevents a 2DEG (or 2DHG) from forming. Threshold voltage statistics measured on MOSFETs are also believed to be a proxy for evaluating the variability on biasing conditions to load the first few charges in co-processed QD devices.

Gathering statistical data at the relevant cryogenic temperatures (around 1 K) has long been an issue, since dilution fridge setups generally require wirebonding and small sample sizes. Very recently, high throughput cryoprober prototypes allowing automated 300 mm waferscale characterization have been used with the aim to speed up and refine screening protocols [189]. Ideally, these FoMs gathered on co-integrated test devices should be correlated to actual QD device measurements, such as stability diagrams. However, selecting biases to find the correct regimes, extracting and analyzing the relevant information from these plots can be quite lengthy and is usually performed by a human expert. Machine Learning-enabled approaches were proposed recently to automate this process as well [190], even serving as the basis to tuning algorithms and quantitative variability evaluation [191].

Still a developing field, the emergence of reliable and high-throughput data collection and monitoring methods that are relevant to spin qubit functionality will be a crucial enabler for process control and maturity ramp-up in an industrial setting.

6. Classical electronics for qubit control and readout

6.1. Cryogenic vs. RT electronics

Controlling a qubit or an ensemble of qubits, or quantum processors, involves a so-called classical controller, which actually performs the control and readout of the qubits, as shown in figure 9. The purpose of the classical controller is to read the state of qubits and to make decisions on how to control them to maintain e.g. coherency or to correct an error due to imperfect or incomplete rotation of a qubit on the Bloch sphere. It is also used to issue instructions to the quantum processor, thereby achieving a certain rotation. The quantum processor is cooled typically at 10–100 mK for solid-state qubits, even though higher temperatures can also be used, while the classical control electronics generating the electrical signals needed for quantum instructions and for reading the state of the qubits, is usually placed at higher temperatures. Today, in most cases, these electronic circuits are placed at RT outside the dilution refrigerator and the connections from RT equipment to cryogenic qubits require long coaxial cables and several steps of thermalization. When scaling to larger quantum processors, the use of off-the-shelf equipment starts to show limitations, whereas extending a 2-qubit to a 100-qubit experiment may be unfeasible due to cost and size. This has led to ad hoc designs [193, 194].

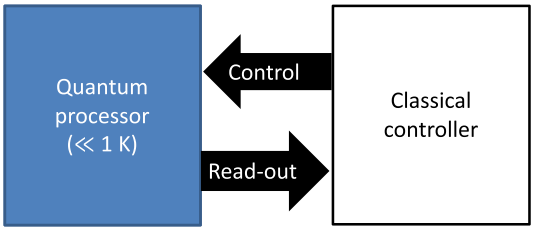

Figure 9. Conceptual Architecture of classical control of quantum processors [192]. A classical controller is used to issue control instructions for qubits that are also used for quantum error correction. A readout route is used to ascertain the state of qubits for evaluation and correction. © [2016] IEEE. Reprinted, with permission, from [192].

In 2016, some of us have proposed to move the control functions to cryogenic temperatures, close to those of the qubits, so as to achieve a more compact and scalable solution [192, 195]; the most important advantage of this solution, however, is reliability. In this context, many components necessary to control qubits were implemented in standard CMOS technologies and successfully tested at 4 K [109, 159, 196–201]. Recently, Google and IBM, along with others, have followed similar approaches and produced integrated solutions that will be described later.

6.2. Cryo-CMOS electronics

6.2.1. QC stack. The control of a qubit starts from a quantum algorithm, described in a certain programming language that is compiled into quantum circuits, i.e. a sequence of operations to be applied on a set of qubits. Quantum arithmetic is also used in this context, along with compilation of certain functions into a quantum instruction set used for quantum execution (QEX) and QEC. Finally, the QEX and QEC are implemented using the quantum–classical interface, which operates directly on the qubits. This process is depicted in figure 10 and is referred to as the quantum-computing stack.

Quantum-computing stacks may be distributed in space and involve an increasing temperature of operation, whereas the bottom of the stack is always at the base temperature of qubits and the top at RT. While most classical control systems are implemented in field-programmable gate-arrays (FPGAs) today, increasingly, application-specific integrated circuits (ASICs) are being designed, whereas cryogenic CMOS (cryo-CMOS) or cryogenic SiGe BiCMOS are emerging as the technology of choice. The proposed ASICs generally implement the same functionality of FPGAs, albeit with specifications that are designed for lower temperature of operation. Deriving specifications for the ASICs is a complex undertaken, as it requires one to know all the detailed relations between performance of a given component and fidelity of the operation. Generally, one begins from fidelity working backwards to e.g. the signal-to-noise ratio (SNR) of the down-converter or the noise figure of the low-noise amplifier (LNA). Spectra of

Figure 10. The quantum-computing stack from the public talk in [192]. Drawing by Harald Homulle (2016). It includes all the components required to execute quantum algorithms in hardware. QEX and QEC and QEC, respectively. Reproduced with permission from Harald Homulle, 2016.

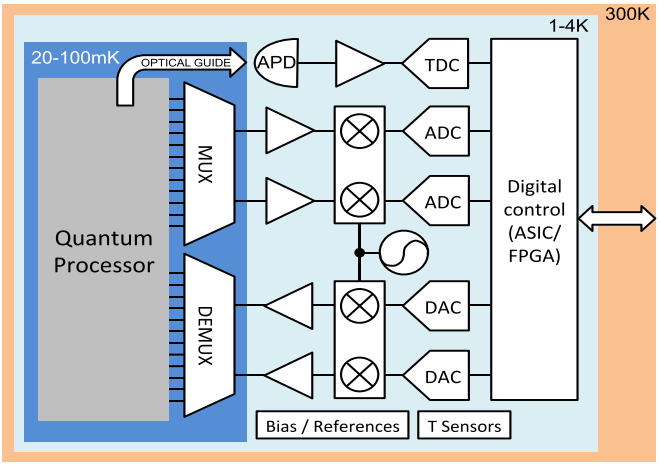

Figure 11. Generic architecture of quantum–classical interface for the control of qubits [192]. It is similar to a radio-frequency transceiver used in radios, including LNAs, down- and up-converters, A/D and D/A converters, and a logic block to make decisions on QEC. An optical path for reading ion trap states optically, is also present. © [2016] IEEE. Reprinted, with permission, from [192].

the control signals may also be optimized, so as to minimize qubit kick-back and this is something for which a software-defined controller can be very useful, as we will see later.

6.2.2. Control architectures. CMOS/BiCMOS technologies operating at deep-cryogenic temperatures are known collectively as Cryo-CMOS integrated circuits and, while theoretically possible, so far, no IC has been demonstrated for the control of qubits that also includes detection and correction of errors for a full-tolerant quantum computer. The proposed quantum–classical interface based on cryo-CMOS is shown in more detail in figure 11. The signals generated with a very tight control in amplitude, frequency, and phase use an envelope that must be programmable both in shape, usually Gaussian or raised-cosine, or even square, and in duration, generally around 20 to 60 ns.

Once the components of the quantum–classical interface are defined, one must implement them, so as to meet the specifications at a wide range of temperatures, including the nominal temperature of operation of 1–4 K. To determine the specifications of each component one usually starts from the system fidelity, generally 99.99% in most cases. Using appropriate simulators, such as SPINE or QuTIP, assuming the Hamiltonian of the qubits is known, one can propagate the fidelity to critical specification, like input-referred noise, phase and frequency noise, and SNR. This is the first challenge in the design of the classical control of a quantum processor, for more details on this process, we refer to a comprehensive study of the impact of any non-ideality of the control electronics on fidelity by way of simulations and analytical derivations [202, 203].

For a truly scalable quantum computer though, over 1000 qubits need to be planned. Thus, an overall power dissipation per qubit of cryo-CMOS control will need to be restricted to about 1 mW/qubit to enable todays refrigeration units to absorb the thermal emissions of the control circuits. This is currently one of the hardest challenges. Furthermore, in the case of cryo-CMOS circuits the design process must be supported by proper modeling of transistors and passive elements. This requires an intimate knowledge of all components and the interaction between each other at low temperature.

6.2.3. Circuits and systems. Figure 11 shows the basic components required in typical controller. These include LNAs, up-and down-converting mixers, A/D and D/A converters, a frequency synthesizer, and a digital controller. The most critical of all these components are the LNAs, whose input referred noise, often referred to as noise-equivalent temperature, determines a major bottleneck of the system. Jeroen van Dijk derived specifications for all the components required in the control of spin qubits [202, 203], which were eventually used for the design of the Horse Ridge chip. As it turns out, for example, the timing jitter inaccuracy for the pulse length, set at 3.6 ns, could be easily met in the target CMOS technology and thus other specifications requiring more power could be met with more ease. These trade-offs are common in these circuits to enable the overall power budget at system level to be met.

6.2.4. Models Modeling is the first consideration when designing cryo-CMOS circuits and systems. For this reason, in 2015, so-called transistor farms were designed in 0.16 μm and 40 nm CMOS technologies [204], where MOS transistors of type N (NMOS) or P (PMOS) and with geometries of varying aspect ratios, long or narrow, and varying dimensions were implemented. The characterization of these mature CMOS processes enabled the creation of models based on the underlying physics that could explain the behavior of transistors at K or mK temperatures.

Next, existing models such as PSP or BSIM4 were augmented with physical effects observed in the characterization of the farms, starting from $I_d - V_{ds}$ and $I_d - V_{gs}$ characteristics

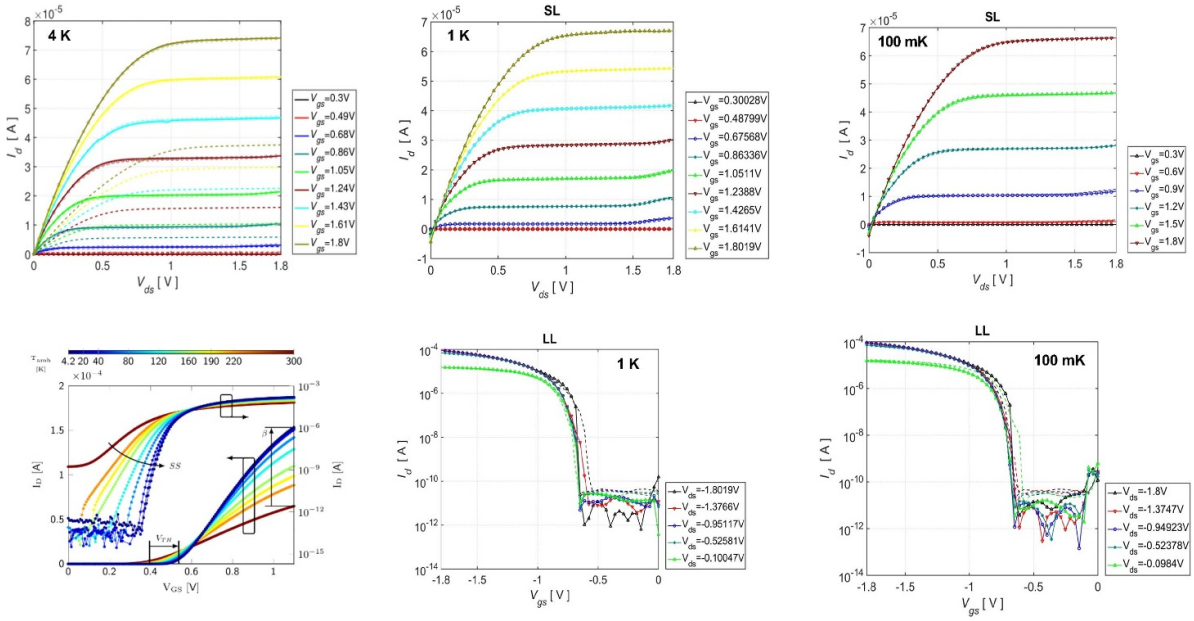

Figure 12. Top: 0.16-μm NMOS $I_d - V_{ds}$ curves for various values of V_{gs} and temperatures. For the definition of SL/LL/SS: see text. Bottom left: $I_d - V_{gs}$ curves for 40-nm PMOS and NMOS transistors as a function of temperature. Bottom center and right: large NMOS $I_d - V_{gs}$ as function of V_{ds} for two temperatures [205, 206].

shown in figure 12 and continuing with subthreshold slope characterization that is essential in the behavior of both analog and digital circuit dynamics at low temperature. Characteristics $I_d - V_{ds}$ and $I_d - V_{gs}$ refer to the drain current as a function of the voltage difference between drain (d) and source (s) and as a function of the voltage difference between gate (g) and source, respectively. In the figure, 'L' means large and 'S' small referred to the width and length of transistors, respectively.

There are other physical phenomena observed at 4 K not present in the standard temperature interval; such is carrier freeze-out of the substrate, which refers to the suppression of carrier availability in the substrate at cryogenic temperatures. Another physical effect observed at cryogenic temperatures in deep submicron (DSM) MOSFETs is the discontinuous or noisy behavior of the subthreshold current explained by the incomplete ionization of dopants and Coulomb barrier [207]. This behavior limits subthreshold operation as a choice for analog circuits and sets a lowerbound for the supply voltage in digital circuits.

Different behaviors of MOSFETs are observed at cryogenic temperatures depending on the technology, by which they are fabricated; thus, fully-depleted silicon-on-insulator (FDSOI) MOSFETs and FinFETs show different behavior at 4 K than a standard bulk CMOS process. All MOSFETs in state-of-the-art technologies, however, show correct transistor operation in moderate and strong inversion.

From a circuit design point of view, the important differences at cryogenic temperatures are the increase in transconductance efficiency (g_m/I_d) and the reduction in leakage by up to 3-4 times in weak inversion [204, 205]. However, other effects such as device variability, mismatch and self-heating is generally higher at cryogenic temperatures, as detailed in the following subsection. Additionally, while thermal noise is lower, other types of noise, such as flicker noise can be significant, thus especially impacting analog and mixed-signal circuits [192, 196, 206, 208–213].

6.3. Case studies

6.3.1. Horse Ridge. The design is a cryo-CMOS controller for both superconducting and spin qubits. The chip comprises a set of numerically-controlled oscillators (NCOs), which feed two mixers in quadrature upon phase and amplitude control and a mechanism for image rejection, all implemented in a digital back-end. Upon D/A conversion, and independent variable-gain amplifiers, the I and Q signals are low-pass-filtered and mixed with a local oscillator (LO), which is used to achieve the final frequency of 2 to 20 GHz. Figure 13 shows the architecture of the controller, capable of providing a 44-dB output power range from −60 to −16 dBm. The controller generates pulses with programmable duration from 50 to 500 ns and 5 different envelopes (Cosine, Raised-cosine, Rectangular, Gaussian, and Triangular), with a phase imbalance of the carrier frequency of at most 0.2 degrees, an SNR of 50 dB in 10 MHz bandwidth, and an HD3 of −44 dB in the analog front-end [197]. In the digital front-end, the NCO frequency has a 22-bit resolution, with a SNR of and an SFDR both of 54 dB. The lookup table generates the envelope using a 10-bit word, while the envelope phase and the correction network have a resolution of 10 and 9 bits, respectively.

The chip, fabricated in a 22 nm FinFET CMOS technology, occupies an area of 4 mm^2 and dissipates 384 mW, operating at 3 K. Horse Ridge was used to control two SiGe spin qubits enabling the implementation of a Deutsch-Jozsa

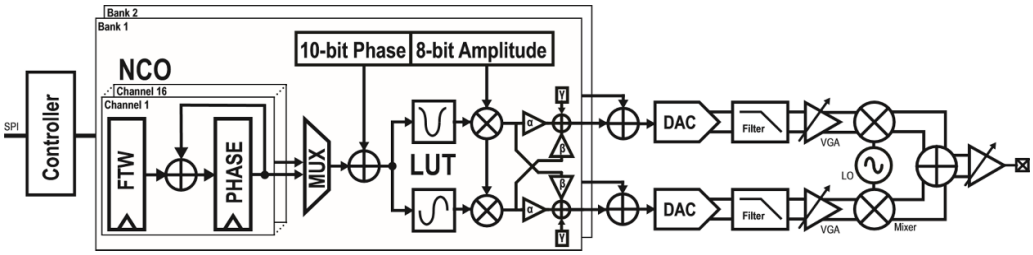

Figure 13. Architecture of the controller employing direct digital synthesis in a large digital back-end. Single-sideband modulation is implemented in the analog front-end, where it is filtered and amplified [197]. Adapted from [197]. CC BY 4.0.

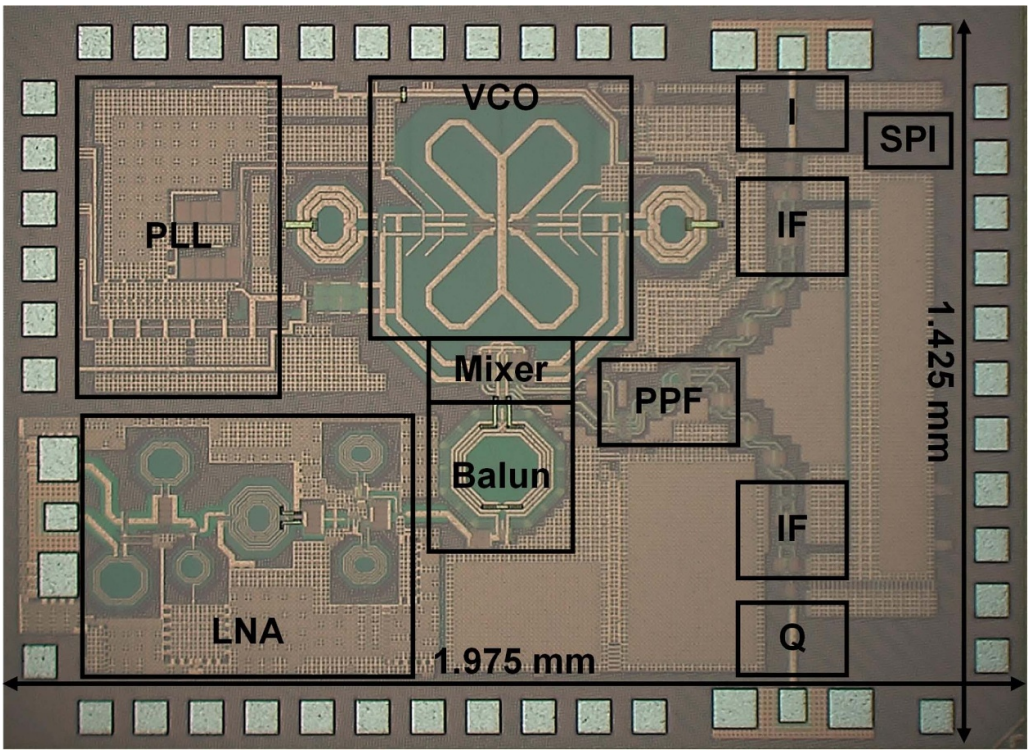

Figure 14. Photomicrograph of the chip Quadro. The chip's specifications and measurements can be found in [215]. Reproduced from [215]. CC BY 4.0.

algorithm [214]. The control of qubits was compared with RT control using conventional instrumentation, via electromagnetic switches and a RT readout system. Randomized benchmarking on 60 Clifford gates yielded a fidelity of 99.69% vs. 99.71% obtained with RT control.

6.3.2. Quadro. The design is a cryo-CMOS system for the readout of the state of spin qubits integrated in standard 40-nm CMOS technology. The readout system was designed to perform radio-frequency reflectometry readout of semiconductor qubits/QDs. The chip comprises a wideband LNA, a quadrature mixer, a complex filter, a pair of in-phase/quadrature (I/Q) intermediate frequency (IF) amplifier chains, and a type-II charge pump phase-locked loop with a programmable frequency divider providing LO signals.

The LNA and the quadrature active mixer were designed to obtain the required noise and linearity performance to be interfaced with QDs. A mode-switching complementary voltage-controlled oscillator was used to achieve low-power and low phase noise in a wide frequency tuning range (46.5%). Several circuit modifications were applied to the charge pump design to make the cancellation of mismatch and the mitigation of charge sharing robust for cryogenic temperature operation. Furthermore, additional cryogenic design considerations for the were used in this design.

Measurements showed that the readout could provide an average gain of 65 dB, a minimum noise figure of 0.5 dB, an IF bandwidth of 0.1-1.5 GHz, and an image rejection ratio of 23 dB at 3.5 K with a power consumption of 108 mW, which results in 1.5 mW/qubit when frequency multiplexing is applied. This cryo-CMOS receiver with frequency synthesizer for qubit readout is a first step towards fully-integrated qubit readout and control. Figure 14 shows a micrograph of the readout chip Quadro with the overall specifications that can be found in [215].

7. Scalability and applications

There are two kind of commercial quantum computer projects involving spin qubits in silicon. Like for other technologies, the former is represented by public companies such as Intel, while the other is constituted by recent startups, such as Silicon QC, Quantum Motion, Diraq and Equal1. In this section, the results of such companies are summarized and the potential application of the current technology is outlined.

7.1. Intel

In order to reaching fault tolerance, Intel plans to achieve million qubits. The goal is planned to be achieved as third development phase after a phase for a proof of concept, targeting 50+ qubits, to show that the computational power exceeds supercomputers, intended to serve as learning test bed for quantum systems. The next phase targets a 1000+ qubits chip, for small problems such as chemistry, material design, optimization, involving a limited error correction. Intel has already developed Horse Ridge 1 and 2 to address spin qubits, designed to operate at 4 K by the Intel 22 nm FinFET technology. Horse Ridge 1 performed coherent qubit control, randomized benchmarking and two-qubit algorithm on a 2-qubit quantum processor. Horse Ridge 2 handles all the control functions of drive, readout and gate bias pulsing [216]. Advanced semiconductor manufacturing is exploited in the attempt of making massively scaled transistors devices and apply them to spin-qubit devices. A 300 mm cryoprober was developed to measure entire wafers at 1.6 K to allow down-selection of spin qubit devices for measurements in a dilution fridge. The information extracted by such method enabled first to process highly coherent Si/SiGe spin qubit devices fabricated using EUV lithography. Controlled and stable quantum dot devices with independent barrier control have been achieved, including qubit control by EDSR with on-chip micromagnets [214]. Intel claims that the results are reproducible on multiple devices and fridges. [177] The company reported the demonstration of two-qubit gates on Si/SiGe QD devices made with 300 mm EUV technology. [217] The spin qubit is based on a single electron confined in a QD. Also in this case the single-qubit gates are performed via EDSR, with nearby micromagnets aimed at providing the artificial spin–orbit coupling and the qubit frequency separation. The exchange coupling between two qubits is obtained by rapid voltage pulses, enabling the realization of various types of two-qubit gates. In parallel, Intel has developed a surface code including 5 stabilizer terms (executed on the QuTech Quantum Inspire superconducting quantum processor) [218] In April 2022 the company announced they achieved a process that could fabricate more than 10 000 arrays with several silicon-spin qubits on a single wafer with greater than 95 percent yield [168].

7.2. Start-ups

Surprisingly, three out of four silicon quantum startups have been created in the same year, namely in 2017.

Silicon QC (2017) is an Australian-based startup (https://sqc.com.au/) who raised about 56 M USD. The roadmap of SQC is of achieving 10 qubit 2023, 100 qubits in 2030 and UQC mid-2030. The company bases the fabrication of the quantum bits on the deterministic doping of silicon so to obtain a qubit per single donor atom. In 2022, the company announced [219] the engineering of topological states in atom-based semiconductor QDs. Here, the quantum states are used to produce a small quantum simulator, such as a controllable fermionic quantum systems taken as example of condensed-matter physics.

High-fidelity single-shot electron spin readout using a nanoscale single-lead QD (SLQD) sensor has been developed, capable of reading multiple qubits. Such gate-based SLQD sensor is deployed in an all-epitaxial silicon donor spin-qubit device, so to demonstrate single-shot readout of three P donor QD electron spins with a maximum fidelity of 95% [220].

Quantum Motion (2017) is a British startup (https://quantummotion.tech/) who raised 9.8 M USD in two rounds. In [149] they reported the measurement of an electron spin in a singly occupied gate-defined QD, fabricated using CMOS-compatible processes at the 300-mm wafer scale. The readout is based on spin-dependent tunneling with a single-lead quantum-dot charge sensor, measured by using rf gate reflectometry, which allows to obtain a maximum electron-spin relaxation time $T1$ of 9 s at 1 T. Next, the company [106] presented the demonstrations of high-fidelity single-shot readout of spins in silicon QDs using a dispersive charge sensor. The spin read-out fidelity results of 99.2%.

Diraq (2022) is based in Australia and it has been funded by a Series A round at its foundation. It intends to exploit the patented single qubits in SiMOS in 2014 and two-qubits in 2015 [165] respectively, and a fully integrated architecture proposal. The research group at University of New South Wales, after proposing a logical qubit in 2018, and proving a high fidelity one qubit (record) and two-qubit gate in 2019, demonstrated hot qubit operation at 1.5 K and patented coherent electron shuttling and global control in a resonator [221] in 2021, and on-demand electrical control in 2022. All the related publications of the group have been patented by the UNSW. The roadmap of the next ten years concern a 9-qubit logic processor and next the transition from physical to logical qubits by a 256-qubit foundry device, towards full QEC. The Diraq company maintains 28 patents and patent applications conceived at the USW across major jurisdictions, including the US, Europe, Australia, China, Japan, South Korea and India. The portfolio involves the design and operation of silicon spin qubits compatible with CMOS foundry manufacturing, including CMOS-based architecture for billions of qubits, capable of full error correction.

Finally, Equal1 (2017) is an Ireland-based startup (www.equal1.com/) who raised 11.3 M USD in two rounds.

The company is exploring both CMOS charge qubits implemented in 22 nm FD-SOI and also Su-Schrieffer-Heeger (SSH) type QD arrays to implement qubits on collective electronic states [222], the latter involving electronic read-out by doing measurements of the first and last dots in the structure. As the qubits are co-integrated within the

control 22 nm FDSOI technology electronics, the single-charge readout is managed by the integrated circuit itself.

7.3. Maturity of the technology with respect to applications

At the current stage of development, the study of small circuits of qubits look feasible, with a special emphasis on their usage to simulate small quantum systems. The recent demonstration of universal operations on six physical qubits entangled by ZZ gate operations [41], show how small quantum circuits like for generating a three qubits GHZ state is currently possible.

In current Noisy Intermediate Scale Quantum computing era, six qubits are sufficient to demonstrate even evolved algorithms like Grover's [223] and quantum simulation of molecules [224]. Because of the short depth which can be achieved without QEC schemes—the number of qubits is largely insufficient—such application are of little practical use but at the same time they are valuable to enabling tests on this platform and benchmarking the overall performances of the technology compared to the others.

As said, such applications can be extended by those of the silicon quantum chip exploited not as gate model quantum computer but instead as quantum simulator, as done by Silicon Quantum Computing LTD company [219], who reported the simulation of many-body SSH with $N = 10$ sites.

The current maturity of silicon platform can be compared to that of superconducting qubits in 2016, when 5 qubits where made available by the IBM Q 5 Tenerife, which justifies the optimism around the silicon platform.

8. Conclusion and outlook

In this topical review we covered the different aspect of silicon spin qubits, in particular to those central for the transition from a laboratory scale to an industrial one. Modeling and figures of merit on experimental performances of qubits defined in spin degree of freedom of charge carriers confined in QDs and donors in silicon devices have been considered. Aspects on readout schemes and on qubit fabrication with foundry compatible approaches have been included as well as state-of-the-art classical electronics circuits for qubit control and readout. A final section focused on scaling up and first applications of small silicon quantum processors promoted by both industries and start ups completes the topical review.

As an outlook on this review topic, silicon spin qubits will continue to benefit from the MOS technology available for classical processing devices. A quantitative analysis to identify eventual critical roadblocks in the way to reach yields comparable to those achieved on classical computing devices has to be carried on but there is a clear potential for a significant qubit scaling and miniaturization when compared to other QC technologies, such as super conducting qubits, due to their smaller size that, conversely, is responsible of the more stringent fabrication requirements. Those requirements are leading to a slower development of large silicon qubit arrays but progress is notable. As a closing remark, all the quantum computing platforms become usable if fault-tolerance can be reached due to the fact that practical applications require operations with a such stringent low error rate not achievable without QEC. A wider research on the QEC field would have potential to lead to a faster development of silicon-based quantum computers.

Data availability statement

No new data were created or analysed in this study.

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