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Article

Direct Comparison of the Effect of Processing Conditions in Electrolyte-Gated and Bottom-Gated TIPS-Pentacene Transistors

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Abstract: Among the plethora of soluble and easy processable organic semiconductors, 6,13-Bis(triisopropylsilylethynyl)pentacene (TIPS-P5) is one of the most promising materials for next-generation flexible electronics. However, based on the information reported in the literature, it is difficult to exploit in field-effect transistors the high-performance characteristics of this material. This article correlates the HMDS functionalization of the silicon substrate with the electrical characteristics of TIPS-P5-based bottom gate organic field-effect transistors (OFETs) and electrolyte-gated organic field-effect transistors (EGOFETs) fabricated over the same platform. TIPS-P5 transistors with a double-gate architecture were fabricated by simple drop-casting on Si/SiO_2 substrates, and the substrates were either functionalized with hexamethyldisilazane (HMDS) or left untreated. The same devices were characterized both as standard bottom-gate transistors and as (top-gate) electrolyte-gated transistors, and the results with and without HMDS treatment were compared. It is shown that the functionalization of the silicon substrate negatively influences EGOFETs performance, while it is beneficial for bottom-gate OFETs. Different device architectures (e.g., bottom-gate vs. top-gate) require specific evaluation of the fabrication protocols starting from the effect of the HMDS functionalization to maximize the electrical characteristics of TIPS-P5-based devices.

Keywords: organic electronics; TIPS-Pentacene; EGOFETs; HMDS

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1. Introduction

In the last years, the field of organic electronics received increasing attention from many research teams worldwide. The interest in this area arises from both the technological advantages (e.g., fast and low-cost fabrication processes) and the distinguishing properties of the materials (e.g., lightweight, flexibility, and semi-transparency), which make organic electronics suitable for a plethora of applications, ranging from flexible displays [1–4] to wearable electronics [5–7], from the environmental and biological sensing [8–11] to the internet of things [12–14].

Among many organic semiconducting materials, 6,13-Bis(triisopropylsilylethynyl) pentacene (TIPS-P5) appears as a promising candidate for printable [15], biocompatible [16], and high mobility [17] electronics. In addition, TIPS-P5 can be easily implemented for the fabrication of standard organic field-effect transistors (OFETs) as well as electrolyte-gated OFETs (EGOFETs) [18–21], where a liquid medium (either an electrolyte or pure water) is used to implement the gate of the transistor. EGOFETs, in particular, are very attractive because they can be operated at very low voltages (below 1 V), and their compatibility with liquid mediums makes them an ideal choice to be interfaced directly with physiological solutions, paving the way toward biochemical applications like chemical sensors [22] and neural interfaces [23].

Up to now, several research articles have been published exploiting the use of TIPS-P5 by investigating several deposition techniques, ranging from the top quality high-vacuum

sublimation [24,25] to the simplest drop-casting deposition [26–28]. One of the highest advantages of TIPS-P5 is its easy solution processability. In fact, aside from drop-casting, researchers have investigated OFET fabrication where TIPS-P5 was deposed by means of spin-coating [29–31], slot die coating [32–34], and ink-jet printing [15,35], highlighting the excellent suitability of TIPS-P5 for large area and low-cost electronics.

Even though TIPS-P5 can be easily deposited directly on top of several supporting materials, such as paper [36] and polydimethylsiloxane (PDMS) [28], Si/SiO_2 is still the most used substrate for the fabrication of bottom-gate (BG) bottom-contact transistors [17–19,29–32], as well as top-contact transistors [24–26]. Si/SiO_2 substrate is indeed a gold standard reference for the fabrication of organic transistors thanks to its high quality (e.g., finely polished surface and SiO_2 insulator with low defect density), simple and reproducible processability, and the "built-in" BG electrode (Si) and BG insulator (SiO_2). Furthermore, exploiting the double-gate architecture is of particular interest since it can embody the device with additional features, such as improved stability [37] and sensitivity [38].

However, the scientific literature does not provide a clear and consistent picture of the best suitable fabrication platform for TIPS-P5 transistors either in bottom-gate or in top-gate (TG) OFET and EGOFET architectures [16–21]. In fact, even though it is well known that the suitable functionalization/treatment of the Si/SiO_2 substrate prior to the deposition of the semiconducting material can dramatically improve the quality of the deposed film and, in turn, the device performances [39–41], this is not a general rule. For example, TIPS-P5 OFETs are reported with fairly good performance both on treated [24–26] and untreated Si/SiO_2 substrates [29–33]. Therefore, it is not clear whether it is worth functionalizing the Si/SiO_2 substrate for the optimization of the material deposition and device performance. Furthermore, to the best of our knowledge, none of the work so far presented in the literature considered the possible impact that the functionalization of the substrate may have on the conduction of the semiconductor top interface in EGOFETs.

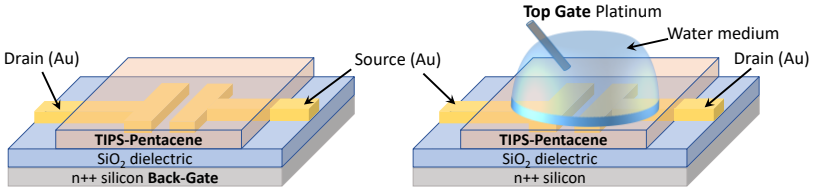
In this work, we perform a comparative investigation of the effect of the functionalization of the Si/SiO_2 substrate on the electrical performances of TIPS-P5-based OFETs and EGOFETs. For this purpose, transistors with a double-gate architecture are the perfect choice because, regardless of the repeatability of the fabrication, a single device can be characterized as BG-OFETs as well as TG-EGOFETs sharing the same semiconducting film, allowing to clarify the effects of functionalization on the characteristics of the bottom and top semiconductor interface. Classical BG-OFETs are readily fabricated using the highly doped Si substrate as the gate electrode, with SiO_2 as the gate dielectric. The same device is also characterized as TG-EGOFET by simply adding a drop of water (deionized water as well as an electrolyte) directly on top of the semiconductor and immersing a conductive wire into the liquid to act as a gate electrode. To analyze the effects of the Si/SiO_2 substrate functionalization on TIPS-P5-based transistors, one-half of the substrates were left untreated (no functionalization). In contrast, the other half were treated with hexamethyldisilazane (HMDS) prior to the deposition of the TIPS-P5 solution. Furthermore, to gain a deeper understanding of how the fabrication process affects the performance of the devices, two solutions of TIPS-P5 with different concentrations were used for film deposition, each deposited at three different substrate temperatures. Finally, a complete electrical characterization allows for comparison of the figures of merit of the fabricated devices, showing how the effects of HMDS functionalization on EGOFETs performances are opposite to those on OFETs, thereby providing essential information for the fabrication of TIPS-P5-based devices over Si/SiO_2 substrates.

2. Materials and Methods

2.1. Devices Fabrication

BG-OFETs and TG-EGOFETs (depicted in Figure 1a,b, respectively) were fabricated onto the same Si/SiO_2 substrates with interdigitated source and drain electrodes (purchased by Fondazione Bruno Kessler, Trento, Italy). In detail, 200 nm of SiO_2 was thermally grown over a heavily doped n-type Si wafer forming the back-gate (n++ Si) and the back-gate

dielectric (SiO_2). Bottom contacts interdigitated source and drain gold electrodes with a thickness of 100–150 nm were obtained by photolithography above a chrome adhesion layer of 3–5 nm, defining the transistor channel with an aspect ratio Z = 560 (each substrate contains four transistors: two with channel length L = 20 µm and W = 11.2 mm, two with L = 40 µm and W = 22.4 mm). Finally, substrates were covered with a layer of photoresist to protect the gold electrodes during shipment.



(**a**) BG OFET (**b**) TG EGOFET

Figure 1. Graphical representation of the BG-OFETs (**a**) and TG-EGOFETs (**b**) architectures.

As received, the substrates were cleaned in an ultrasonic bath with acetone to remove the protective layer of photoresist and other process residuals. A subsequent ultrasonic bath with isopropyl alcohol was done to remove any acetone residuals, promoting a less hydrophobic surface that allows for a better deposition of the semiconductor solution. After the cleaning procedure, half of the prepared substrates were treated with HMDS purchased from Sigma-Aldrich Chemical Co., St. Louis, MO, USA, whereas the other half were left untreated. The HMDS functionalization was performed by exposing the substrates for 2 h to HMDS vapor in a low vacuum chamber.

Two TIPS-P5 solutions (1% and 5% in weight) were prepared by dissolving the organic semiconductor using toluene as an organic solvent. Prior to the semiconductor deposition, the substrates were placed over a hot plate for about 15 min, allowing them to reach the preset deposition temperature (30 °C, 60 °C, and 90 °C). TIPS-P5 solution was drop-cast over each substrate (covering all four transistors in the sample) that was kept at the preset deposition temperature for about 15 min to promote the complete evaporation of the solvent. Before characterization, the samples were stored at room temperature in a nitrogen-saturated environment. High-resolution optical images of the deposed semiconductor are reported in Supplementary Figure S1 for the three deposition temperatures. In contrast, Supplementary Figure S2 shows contact angle measurement confirming the hydrophobicity of the semiconductor.

Notice that such fabrication protocol does not allow for fine control of the semiconductor deposition (thickness, morphology, and molecular ordering). However, thanks to the implementation of a double-layer architecture, BG-OFETs and TG-EGOFETs share the same semiconducting film. Therefore, performing electrical characterizations of the same device in both the BG and TG configurations ensures that performance differences between TG-EGOFETs and BG-OFETs in dependence on the HMDS functionalization are indeed due to the presence/absence of HMDS and not to the process variability.

2.2. Characterization Procedure

Electrical characterizations were performed in the dark inside a grounded Faraday cage using an Agilent B1500 parameter analyzer equipped with two high-power and two high-sensing source measurement units. The samples were initially characterized as standard BG-OFETs without putting the water drop on top of the semiconductor (no top gate). This allows us i) to avoid the capacitive coupling between the BG electronic channel and the TG electrode and ii) to perform a wider voltage scan (up to –20 V), avoiding any risk of electrolysis and preventing any damage to the organic semiconductor. Immediately after the BG measurements, the same transistors were characterized as TG-EGOFETs by using a MilliQ drop as gate medium and a 0.6 mm-thick platinum wire as the gate contact in Figure 1b.

For both BG-OFETs and TG-EGOFETs transfer ($I_{DS}V_{GS}$) and output ($I_{DS}V_{DS}$) double-sweep measurements were performed:

- $I_{DS}V_{GS}$ curves were taken by scanning V_{GS} from +5 V to −20 V (with constant V_{DS} = −1 V and −20 V) during BG-OFETs characterizations, whereas V_{GS} was scanned from +0.1 V to −0.5 V (with constant V_{DS} = −0.2 V and −0.5 V) during TG-EGOFETs characterizations.
- $I_{DS}V_{DS}$ curves were taken by scanning V_{DS} from 0 V to −20 V (with constant V_{GS} = −10 V and −20 V) during BG-OFETs characterizations, whereas V_{DS} was scanned from 0 V to −0.5 V (with constant V_{GS} = −0.2 V and −0.5 V) during TG-EGOFETs characterizations.

All the TG-EGOFETs measurements were performed by grounding the back-gate silicon electrode.

3. Results and Discussion

To investigate how the HMDS functionalization affects the performance of TIPS-P5 OFETs and EGOFETs, the samples were fabricated following the chart in Figure 2. In particular, we fabricated four samples for each deposition condition, and each sample contains four transistors (sixteen transistors for each case).

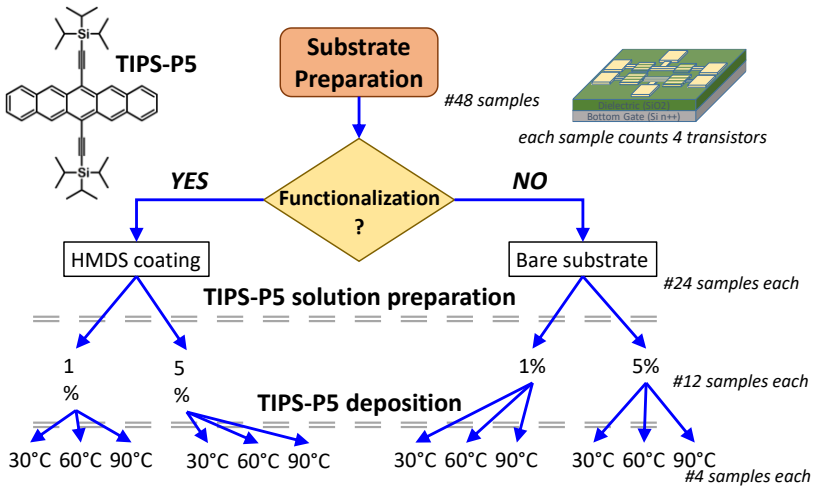


Figure 2. Flowchart of the devices' fabrication procedure.

Figure 3 shows some representative OFET transfer and output characteristics (T = 90 °C and TIPS-P% solution = 1%) for HDMS treated and untreated samples. As can be seen from both transfer and output characteristics, BG-OFETs without HMDS feature small I_{DS} currents and large clockwise hysteresis, which are an index of high molecular disorder and charge trapping at the SiO_2/semiconductor interface [42]. OFETs fabricated using HMDS are characterized by higher currents and much smaller hysteresis, confirming that the use of HMDS for the fabrication of TIPS-P5-bases OFETs promotes a more favorable molecular arrangement for charge transport at the SiO_2 interface.

In order to perform a direct comparison of the electrical characteristics of the fabricated devices, the mobility of the transistor μ_{FET} and threshold voltage V_T were extrapolated from the saturation regime using the following equation:

$$I_{DS} = \frac{1}{2} C_G \frac{W}{L} \mu_{FET} (V_{GS} - V_T)^2 \quad (1)$$

with C_G is the gate capacitance that is equal to 17 nF·cm^{-2} for our BG transistors (200 nm-thick SiO_2 dielectric). Note that Equation (1) is an approximated model that, in particular, neglects the increase of μ_{FET} with the overdrive voltage. Indeed, the literature

reports several accurate models for charge transport in thin film and organic field-effect transistors [43–45]. However, more accurate models are characterized by more complex parameter extrapolation procedures that cannot always be applied due to the transistor's non-ideality and non-stationary conditions. In this work, we chose to extrapolate the data using Equation (1) in order to allow good and reliable statistics to compare all the devices. However, when possible, we also implemented the more complex techniques cited above to check the validity of the data reported in this manuscript (as a reference, Supplementary Tables S1 and S2 report the BG-OFETs and TG-EGOFETs parameters extrapolated using the trans-conductance method).

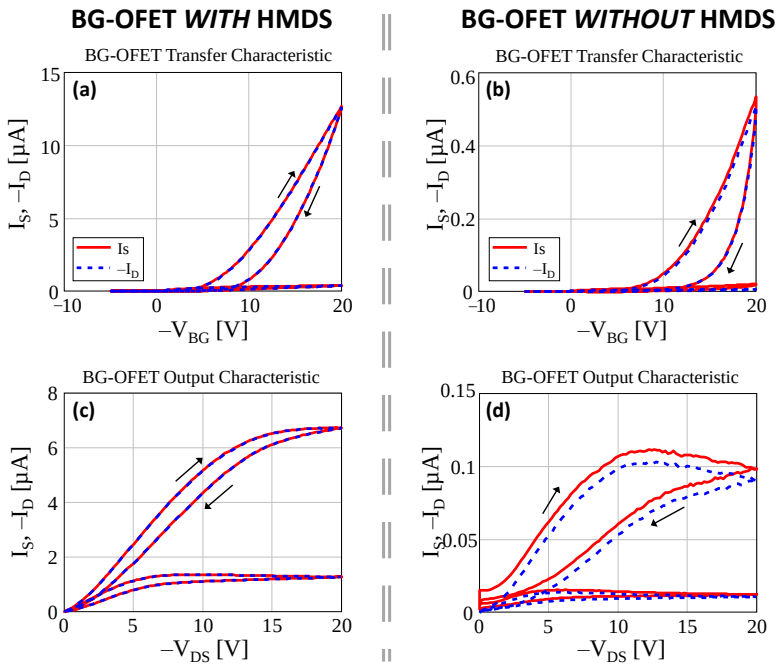


Figure 3. BG-OFETs characterizations with and without HMDS functionalization: (**a**) Transfer characteristics with HMDS; (**b**) transfer characteristics without HMDS; (**c**) output characteristics with HMDS; (**d**) output characteristics without HMDS. Discrepancies between the source (I_S) and drain (I_D) currents are due to BG leakage current (see Supplementary Figure S3).

The comparison of the extrapolated data, summarized in Table 1, clearly shows that OFETs fabricated using HMDS features higher field effect mobility, as expected. Furthermore, for both HMDS-treated and -untreated samples, the mobility increases by increasing the deposition temperature, suggesting that higher temperatures allow a more efficient molecule arrangement that improves the charge transport at the SiO_2/TIPS-P5 interface. In addition, HMDS-treated devices show a reduction of the threshold voltage (in absolute value) with the increase in temperature. In contrast, no evident trend is observed in the threshold voltage of untreated devices. Hence, the combination of deposition temperature and HMDS functionalization can help in tuning the threshold voltage allowing the fabrication of devices for applications such as amplifiers and complementary logic gates, where the fine control of mobility and threshold voltage is of fundamental importance.

Right after the devices were characterized as standard BG-OFETs, a MilliQ drop was put directly on top of the semiconductor, as shown in Figure 1b, and the samples were characterized as TG-EGOFETs. EGOFETs working principle is very similar to OFETs, but instead of an insulator, it relies on the formation of an electrical double-layer as gate capacitance, thus allowing for very low top-gate voltages to drive the accumulation of carriers at the interface with the water (the reader may refer to [46] for a comprehensive review).

Table 1. BG-OFETs parameters extrapolated using Equation (1). All the reported values are averaged over 16 transistors.

TIPS-P5 Solution	Deposition Temperature (°C)	With HMDS Functionalization		Without HMDS Functionalization	
		Mobility ($cm^2\ V^{-1}\ s^{-1}$)	Threshold Voltage (V)	Mobility ($cm^2\ V^{-1}\ s^{-1}$)	Threshold Voltage (V)
1%	30	1.62×10^{-3}	−8.37	5.17×10^{-4}	−6.98
	60	2.44×10^{-3}	−5.95	7.15×10^{-4}	−6.29
	90	3.86×10^{-3}	−4.68	1.16×10^{-3}	−6.44
5%	30	1.35×10^{-3}	−6.35	2.60×10^{-4}	−3.22
	60	1.34×10^{-3}	−2.72	4.19×10^{-4}	−6.24
	90	2.70×10^{-3}	−3.07	1.17×10^{-3}	−5.21

Representative transfer and output curves are reported in Figure 4, highlighting a quasi-hysteresis-free behavior typical of well-performing EGOFETs. Table 2 summaries the threshold voltage V_T and field-effect mobility μ_{FET} estimated using Equation (1), where C_G is now the double-layer capacitance that we estimated to be around 3.8 μF·cm^{-2} by means of electrochemical impedance spectroscopy measurements [47]. Notably, the TG capacitance is much larger than the BG capacitance, allowing us to neglect the capacitive coupling between the Si BG electrode and the TG electronic channel of the EGOFETs [48].

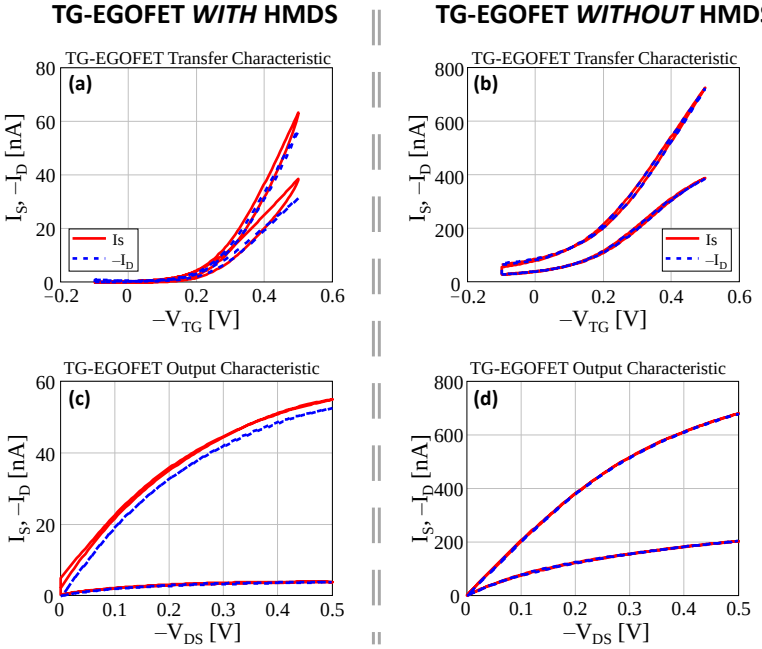


Figure 4. TG-EGOFETs characterizations with and without HMDS functionalization: (**a**) Transfer characteristics with HMDS; (**b**) transfer characteristics without HMDS; (**c**) output characteristics with HMDS; (**d**) output characteristics without HMDS. Discrepancies between the source (I_S) and drain (I_D) currents are due to the TG leakage current (see Supplementary Figure S4).

Remarkably, TG-EGOFETs performance appears to have an opposite trend compared to BG-OFETs. Despite HMDS treatment having a beneficial effect on the BG transistors, it seems to impair EGOFETs performance. In fact, EGOFETs without HMDS treatment feature higher currents and higher mobilities than EGOFETs with HMDS treatment. Furthermore, increasing the deposition temperature no longer improves the performance of the device but, on the contrary, reduces the EGOFETs field-effect mobility. Notably, comparing TG-EGOFETs with BG-OFETs, we notice that devices fabricated without HMDS from 1% solution at 30 °C (i.e., best for EGOFETs performances) show larger TG mobilities than BG mobilities. This suggests that the charge transport is more favorable at the top

semiconductor/liquid interface than at the bottom. Such a result is a further confirmation of the beneficial (almost mandatory) effects of HMDS in BG-OFETs, whereas it indicates that HMDS functionalization should be avoided when fabricating TIPS-P5-based EGOFETs.

Table 2. TG-OFETs parameters extrapolated using Equation (1). All the reported values are averaged over 16 transistors.

TIPS-P5 Solution	Deposition Temperature (°C)	With HMDS Functionalization		Without HMDS Functionalization	
		Mobility ($cm^2\ V^{-1}\ s^{-1}$)	Threshold Voltage (mV)	Mobility ($cm^2\ V^{-1}\ s^{-1}$)	Threshold Voltage (mV)
1%	30	4.42×10^{-4}	−136.99	1.15×10^{-3}	56.99
	60	1.41×10^{-4}	−15.17	7.23×10^{-4}	26.19
	90	1.39×10^{-4}	−19.88	4.55×10^{-4}	−3.75
5%	30	1.63×10^{-4}	−54.18	1.53×10^{-4}	75.94
	60	2.81×10^{-5}	146.36	4.91×10^{-4}	128.08
	90	3.08×10^{-5}	102.57	2.19×10^{-4}	96.50

Another important remark regarding EGOFETs threshold voltage is worth doing. EGOFETs without HMDS show an important positive threshold voltage shift compared with the threshold voltage of HMDS-treated EGOFETs. One might speculate that the introduction of the HMDS layer in the fabrication steps may introduce a different energy level alignment between the SiO_2 dielectric and the semiconductor (via an interface dipole or by introducing/removing interface trap states). However, the same reasoning should also apply to BG-OFETs, which do not show a threshold voltage shift consistent with what is observed with the TG-EGOFETs. Therefore, we can rule out such a hypothesis. Tentatively, we could explain this threshold voltage shift as a consequence of different growth modalities of the semiconductor over the treated and untreated substrates. In fact, different molecule arrangements (orientation and grade of disorder) might lead to different semiconductor/liquid interfaces with an important impact on the threshold voltage during TG-EGOFET operation, but not during BG-OFET operation (which were characterized before putting the water on top). Furthermore, from contact angle measurements (Supplementary Figure S2), we observe that the EGOFETs with HMDS treatment feature larger contact angles than the EGOFETs fabricated without HMDS. Therefore, the EGOFETs with HMDS are more prone to repel water molecules; thus, higher gate voltages are required for charge accumulation, explaining both the positive threshold voltage shift and the higher field-effect mobility of EGOFETs without HMDS.

Finally, we cannot rule out the possibility of device degradation during the characterization protocol. In fact, in previous work, we showed that the TIPS-P5 EGOFETs (without HMDS) features an initial positive threshold voltage shift during stress [16]. Note that the voltage shift reported in [16] becomes appreciable after several hours of stress, which is not the case with our characterization protocol, which lasts only a few minutes. The entity of such variation could depend on the stress/characterization protocol and the morphological structure of the semiconductor layer, and it may be the subject of future studies.

4. Conclusions

In this work, we fabricated transistors using a double-gate architecture as a versatile platform to study the transport properties of a material in the BG and TG transistor architecture. In particular, we investigated how the HMDS treatment of Si/SiO_2 substrates impacts the TIPS-P5 EGOFETs performance, showing that, as opposed to BG-OFETs, the HMDS functionalization negatively affects EGOFETs performance by reducing the carriers' mobility. Our approach allows a direct comparison of the TG and BG performances of the devices independently, particularly on the film morphology and structure characteristics. This is ideal to compensate for the variability of the solution processing and can be used as a general platform for a self-consistent characterization of amorphous thin-film semiconductors. Among the investigated fabrication parameters, the substrate treatment shows the

largest impact on both OFETs and EGOFETs performance, followed by a dependence of the estimated figures of merit with the deposition temperature. Conversely, the comparison of the solution concentration shows how both the BG and TG devices, either with or without HMDS treatment, share similar behaviors. This points to the fact that a low (1%) TIPS-P5 concentration is favorable for device fabrication since it enables OFETs and EGOFETs with higher field-effect mobility than devices fabricated using a high (5%) concentration.

Considering the HMDS treatment instead, we can conclude that achieving high-performing TIPS-P5-based BG transistors on Si/SiO_2 substrates means HMDS treatment should be a mandatory step in the fabrication process. Moreover, the deposition temperature should be carefully selected to improve the field-effect mobility and tune the transistor threshold voltage to get the desired value. Conversely, the opposite observations can be taken for the TG-EGOFETs, for which the HMDS treatment should be avoided. Furthermore, the deposition temperature should be trimmed to match the complete evaporation of the solvent (which is favored at high temperatures) and to ensure good field-effect performances (which may be degraded by an excessively high deposition temperature).

We believe that this work provides useful hints for the fabrication of TIPS-P5 devices, not only for the drop-casting process over standard Si/SiO_2 substrates but also for emerging flexible ink-jet printing technologies. Indeed, during the printing process, substrate choice and functionalization are critical steps to ensure material deposition and adhesion. At the same time, reducing the number and complexity of the fabrication processes is the key to low-cost and fully printed electronics.

Supplementary Materials: The following supporting information can be downloaded at: https://www.mdpi.com/article/10.3390/electronicmat3040024/s1, Figure S1: TIPS-P5 optical images; Figure S2: Contact angle measurements; Figure S3: BG-leakage currents; Figure S4: TG-leakage currents; Table S1: BG-OFETs additional parameters; Table S2: TG-EGOFETs additional parameters.

Author Contributions: Conceptualization, N.L. and M.B.; methodology, M.B. and F.P.; validation, N.L. and M.B.; formal analysis, N.L.; investigation, N.L. and M.B.; resources, S.T. and M.M.; data curation, N.L. and M.B.; writing—original draft preparation, N.L.; writing—review and editing, N.L., M.B., F.P., S.T., M.M. and. A.C.; visualization, N.L.; supervision, S.T. and A.C.; project administration, A.C.; funding acquisition, A.C. All authors have read and agreed to the published version of the manuscript.

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