ASYNCHRONOUS MODULAR SYSTEMS

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Systems constituted by interconnected asynchronous sequential circuits are examined, on the hypothesis that the reaction time of every circuit is unknown, and delays of arbitrary size are present on the interconnection wires. Three system properties are considered, i.e. the well-driveness (the input state of every circuit changes only when the circuit is internally stable), the persistence (every signal is always absorbed by the unit to which it is directed) and the liveness (no situation is reached starting from which a signal is never sent in a given interconnection wire). An abstract model of a circuit and of a system is given in order to analyze the system properties. The synthesis problem is approached in terms of rules that allow us to obtain a larger system by interconnecting smaller ones, preserving the considered properties.

INTRODUCTION

The trend in digital system design is towards structures in which mutually asynchronous blocks operate concurrently. In such systems, not controlled by a master clock, the activity of every block is regulated by signal exchanges with the other blocks. Asynchronism can improve the hardware utilization, since as soon as one activity terminates, another activity can initiate, without waiting for the end of a given time interval, as in the synchronous case. The information exchange among the blocks can be of two types: *control signals* and *data* [1] . A control signal consists of a binary transition in a control wire, while a datum consists of a binary level in a datum wire.

A block can not know if a new datum has reached its input by examining the datum value only. Therefore, a control signal must be generated when a new datum has been produced, and when such signal reaches the input of a block, the block must be guaranteed that the new datum has also arrived. This can be accomplished by generating the control signal slightly later than the new datum value, and by designing the datum path so that the control signal precedes the datum.

We want to investigate the behaviour of systems constituted by blocks whose operation speed is unknown, and on the hypothesis that delays of arbitrary size are present on the control interconnection wires. The delays on data wires must be properly related to those on the control wires, in order to allow a correct data notification.

In a system we shall consider explicitly only the control information flow among the blocks, that is, the set of all the control signals and the set of those particular data (*parameters*) that condition such control signals. The system behaviour will be examined independently from the actual data values, and, therefore, the law that determines the parameter values is not explicitly considered, and the parameters are regarded as independent input variables of the blocks.

Let us suppose that a block, in relation to the control information flow, is an asynchronous sequential circuit, without hazards and critical races. In order to have a determinate behaviour of every circuit, an input variable of a circuit must switch only when the circuit is internally stable (*well-driveness*) [2] . Moreover, to assure a correct behaviour, no signal must be sent on an interconnection wire before the previous signal on the same wire has been absorbed by the circuit to which it was directed (*persistence*) [3,4] . Finally, no situation must be reached starting from which no signal is ever sent on a given interconnection wire (*liveness*) [4,5] .

In this work the structural model of an asynchronous circuit is discussed, in order to implement asynchronous circuits that are to be inserted in asynchronous systems, and an abstract model is deduced, that allows us to schematize the circuit behaviour and to make an easier analysis of the system properties. Well-driven, persistent and active systems are considered, and rules are given that allow us to obtain a larger system starting from two smaller ones, preserving the previous properties.

CIRCUITS AND SYSTEMS

Let us consider an asynchronous sequential circuit in which each output variable coincides with an internal variable (see Fig.1).

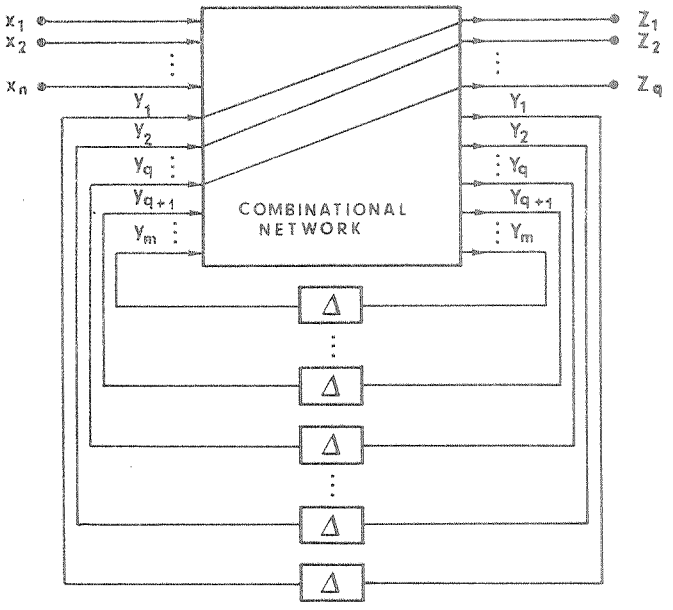


Fig.1

Each asyncrhonous sequential circuit and each combinational circuit can be reduced to this particular schema, by regarding the output variables as internal variables. Let us suppose that in a transition from a stable internal state to another stable internal state, all the variables which must change are allowed to change simultaneously without critical races. Let us also suppose that the circuit is free of any types of influent hazards. If at a given time, due to an input state change, the circuit becomes internally unstable, the circuit is internally stable again after a time (*reaction time*) :

$$T_s = \max(T_x) + \max(T_d) + \max(T_y)$$

where:

T_x is the time required by the combinational network to evaluate the new value of an internal variable;

T_d is the time employed by the new value of an internal variable to propagate from the output to the input of the combinational network, through the feedback path;

T_y is the time employed by the new value of an internal variable to propagate through the combinational network.

The first new value of an output variable could be evaluated after a time:

$$T_z = \min(T_x) + \min(T_d)$$

If we want the new values of the output variables to reach the external world of the circuit only when the circuit is internally stable again, it is sufficient to insert at each output terminal a delay δ , whose size is (see Fig. 2):

$$T_i = T_s - T_z$$

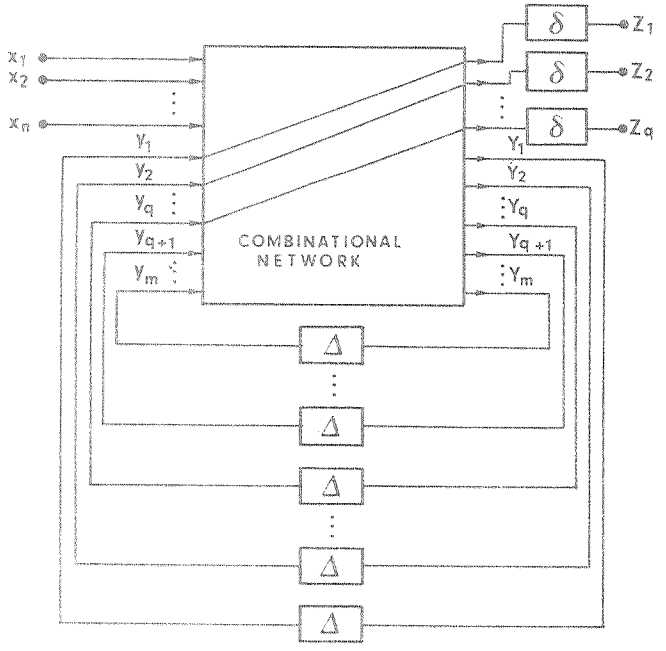


Fig. 2

The input variables of a circuit are partitioned into two classes: *control variables* and *parameters*. Let us suppose that an internal state change happens only in response to control variable changes. In a system a circuit must be well-driven. From the reasoning given in the introduction, it follows that if a circuit is well-driven in relation to the input control variables, it is also well-driven in relation to the parameters. As the system properties are analyzed on the hypothesis that the actual reaction time is unknown, the only way to state that a circuit is again internally stable after the change of some input variable values, is to verify that at least one of the new output variable values has reached the corresponding output terminal of the circuit. This implies that only circuits for which an internal state change always produces an output state change, must be considered. If a circuit is well-driven, everything happens as if the combinational network and the feedback path are delay free and at each output terminal a delay τ (possibly not constant) is present, that simulates the time interval between a transition of some input variables and a transition of the output variable on the considered wire. We obtain an ideal model (*element*) as shown in Fig. 3.

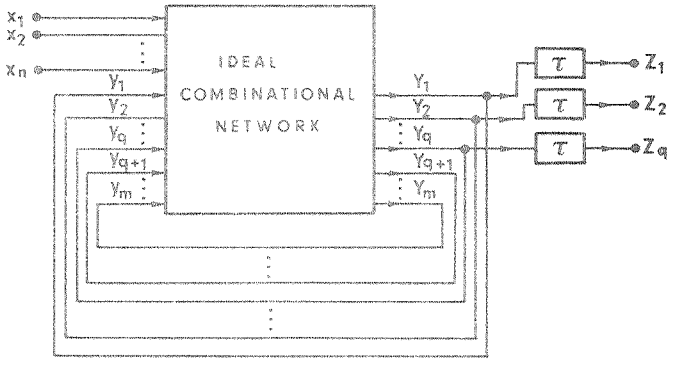


Fig. 3

An ideal model of a circuit will cover the whole class of physical circuits having the same input-output sequential function, no regard being made on the actual reaction

time. Then let us suppose that the delays associated with the outputs of the ideal model have an arbitrary but finite size. In the considered systems an output terminal of a circuit C^h is connected to only one input terminal of another circuit C^k, by means of a wire having a delay of arbitrary but finite size. The connection of an output terminal with more than one input terminal can be accomplished too, by considering a fork of wires as a circuit. The delay introduced by the interconnection wire can be taken as a whole with the delay associated to C^h at the considered output terminal.

In order to analyze the system properties, we schematize the system as an interconnection of elements. Such interconnection will be called *net*. The behaviour of a net will simulate the behaviour of the corresponding system only if the net is *self-regulating* (see Definition 7).In fact such condition assures that each circuit in the system is well-driven. In the next section, elements and nets will be precisely defined.

ELEMENTS AND NETS

Definition 1. An *element* is a device with n input variables $x_1, x_2, \ldots, x_n$, m internal variables $y_1, y_2, \ldots y_m$, p parameters $\varphi_1, \varphi_2, \ldots, \varphi_p$, $q \leq m$ output variables $Z_1, Z_2, \ldots, Z_q$, that realizes :

ii) m logical functions

$$Y_i = f_i(x_1, x_2, \ldots, x_n, \varphi_1, \varphi_2, \ldots, \varphi_p, y_1, y_2, \ldots, y_m) \quad i=1,2,\ldots,m;$$

ii) q transfer operations

$$Z_j \leftarrow y_j \quad j=1,2,\ldots,q.$$

Each logical function $f_i(.)$ gives the new value of the internal variable y_i. When $Y_i \neq y_i$, the variable y_i is *unstable*, and the time required for the variable to attain its new value (to *switch*) is supposed to be equal to zero. Each output variable Z_j takes the value of the corresponding variable y_j. When $Z_j \neq y_j$, the variable Z_j is *excited*, and the time required for the variable to switch is neither constant nor bounded, but finite. Each parameter is linked with one or more input variables in the sense that its value can change only when the value of at least one of such input variables changes.

Definition 2. An element is *normal* if:

i) for every value combination of the input variables and of the parameters, each unstable internal variable, when it switches, becomes stable, and each stable internal variable remains stable until the value of at least one input variable changes;

ii) every time some internal variables become unstable, at least one output variable becomes excited when such internal variables switch.

In the following, we shall always refer to normal elements. In Fig. 4 some simple elements are described.

Definition 3. A *net* is an interconnection of elements, where each input (output) terminal of an element is connected to exactly one output (input) terminal of another element. No delay is present on the interconnection wires.

Note that a set of elements connected to an external world constitutes a net, according to the previous definition, if the external world is regarded as one or more elements.

Definition 4. In a net, all the output variables of the elements are called *connection variables*. The connection variables and all the internal variables of the elements are called *state variables*. Every value combination of the state variables constitutes a *state* of the net. The four values of a pair of variables (y_j^h, Z_j^h) of an element E^h, i.e. 00, 01, 11, 10, are respectively denoted by 0, 1^*, 1, 0^*.

Definition 5. Let S_a and S_b be two states of a net. S_b is *consecutive* to S_a if it is

immediately reached from S_a when some output variables of some elements, excited in S_a, switch.

Let Z_j^h be a connection variable in a net, and let Z_j^h be excited in a state S_a. If there is a parameter φ_k linked to Z_j^h, then the actual state the net reaches when Z_j^h switches depends also on the actual value of φ_k.

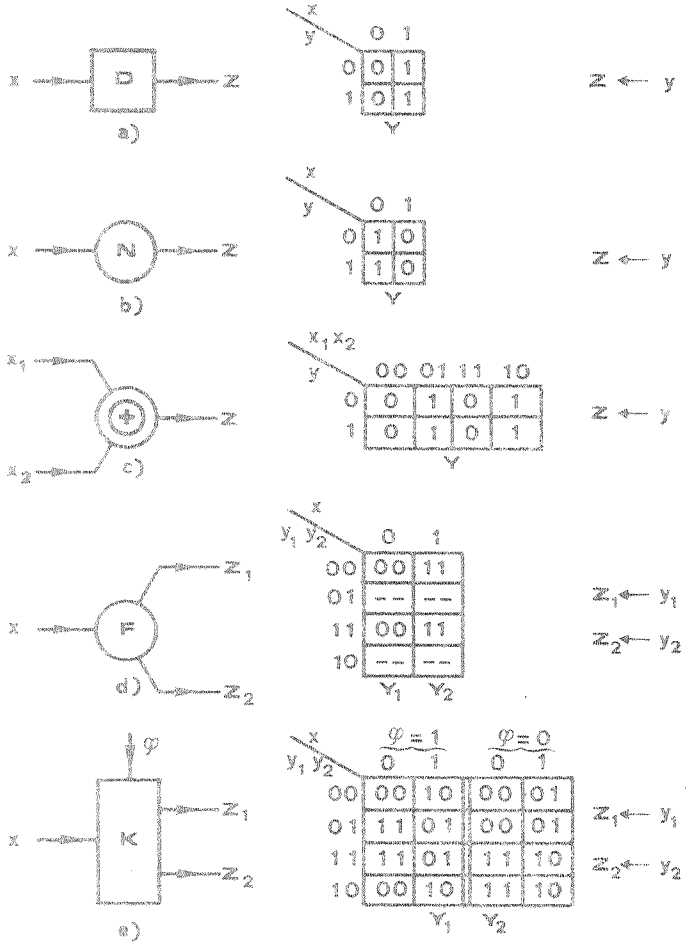


Fig. 4. a) A Delay element;
b) a Not element;
c) an Exclusive-or element;
d) a Fork element;
e) a Decider element.

Definition 6. A sequence of states of a net $S_a, S_{a+1}, \ldots, S_{a+u}, S_{a+u+1}, \ldots, S_b, \ldots$, such that S_{a+u+1} is consecutive to S_{a+u}, is an *allowed sequence* starting from S_a. A state S_b is *successive* to a state S_a, if S_b follows S_a in an allowed sequence.

The behaviour of a net, placed initially in a state S_a, is represented by a *state diagram* with respect to S_a, i.e., by a directed graph in which the nodes are associated with the states of the allowed sequences starting from S_a, and a directed arc connects the node associate with a state S_b, to the node associate with a consecutive state of S_b. If a state S_c is consecutive to a state S_b for a combination Φ of the parameter values, the directed arc connecting the nodes associated with S_b and S_c, respectively, is marked by Φ.

Definition 7. In a net an element E^h is *well-driven* with respect to a state S_a, if in every allowed sequence starting from S_a, every time some output variables $Z_i^h, Z_j^h, \ldots, Z_w^h$ of E^h become excited, no input variable of E^h switches until at least one of the variables $Z_i^h, Z_j^h, \ldots, Z_w^h$ switches. A net A is *self-regulating* with respect to a state S_a if all the elements of A are well-driven with respect to S_a.

Note that a simple rule, sufficient to assure the self-regulation property consists in verifying that an input variable and an output variable of an element are never both excited.

Definition 8. In a net, a connection variable is *persistent* with respect to a state S_a if, in each allowed sequence starting from S_a, the variable, when it is excited, remains excited until it switches. A net is *persistent* with respect to a state S_a if each connection variable is persistent with respect to S_a.

Note that in a persistent net each signal is always absorbed, i.e., no signal is lost. The persistence property is an extension to our nets of the "semimodularity" introduced in [3].

Definition 9. In a net a connection variable

is *live* with respect to a state S_a if, the net placed in S_a or in a state successive to S_a, it is possible to give a proper combination of the parameter values such that in a finite time the variable becomes excited. A net is *live* with respect to a state S_a if each connection variable is live with respect to S_a.

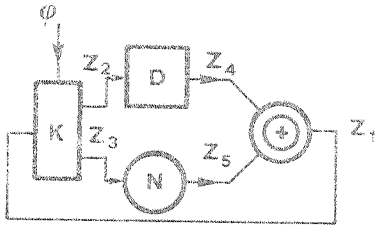
The liveness property is similar to the homonymous property in Petri Nets [4] .

A self-regulating, persistent and live net with respect to the state $S_1 = 0^*0\ 0\ 0\ 1$ is given in Fig. 5a), and its state diagram with respect to S_1 is given in Fig. 5b). In each state of the diagram the i-th symbol represents the value of the i-th state pair (z_i, y_i) , i=1,2,3,4,5.

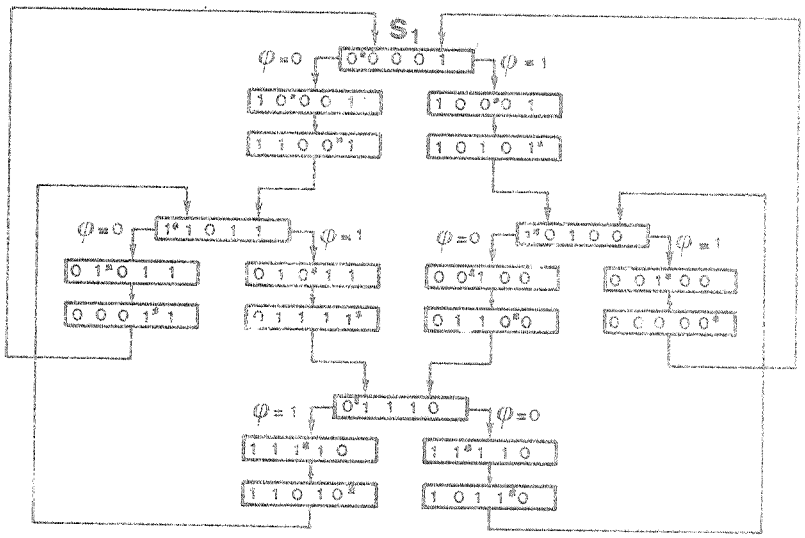
In the next section, the problem of obtaining a larger net by starting from two smaller ones, is considered. Rules are given in order to assure that the resulting net is self-regulating, persistent and live.

INTERCONNECTING NETS

In the following, we shall consider also *virtual elements*, that is, devices that satisfy Definition 1, excluding the limitation that the time required for an output variable to switch, when excited, is finite. Such elements do not simulate the behaviour of a circuit, but the behaviour of a set of circuits, as viewed by a circuit in a system. For example, for each element in Fig. 4 , the corresponding virtual element may be defined.



a)



b)

Fig. 5.

The following statements hold.

Statement 1. Let A be a net constituted by a set B of elements and by a Delay D. If A is persistent with respect to a state S_a, then, starting from S_a, the set B can be regarded as a Virtual Not.

Proof. Let S_k be a state of A such that S_k is equal to S_a or S_k is a successive state to S_a. Two cases can exist: 1) In S_k it is $Z_1 = \bar{Z}_2$ (see Fig. 6), and, then, in S_k the variable Z_2 is excited. As A is persistent with respect to S_a, the value of Z_1 can not change until Z_2 switches. 2) In S_k it is $Z_1 = Z_2$ and, then, in S_k the variable Z_2 is not excited. The value of Z_2 can not change until Z_1 switches. Z_1 may or may not switch depending on the liveness of A and on the parameter values. In both cases B behaves as a Virtual Not.

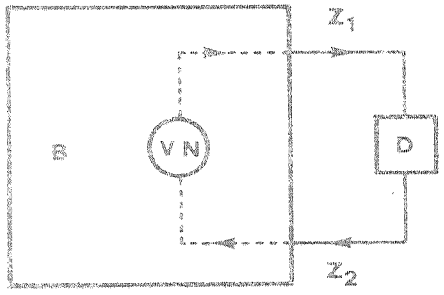


Fig. 6

Statement 2. Let A be a net constituted by a set B of elements and by a Not N. If A is persistent with respect to a state S_a, then, starting from S_a, the set B can be regarded as a Virtual Delay.

Proof. It is similar to the proof of Statement 1.

Statement 3. Let A be a self-regulating and persistent net with respect to a state S_a, and let E^h be an element of A. The net A', obtained by substituting E^h with the corresponding virtual element E^h_v, is self-regulating and persistent with respect to the state S'_a in which the value of each state variable is equal to the value of the corresponding state variable of A in S_a.

Proof. The state diagram of A' with respect to S'_a is a subgraph of the state diagram of A with respect to S_a. The Statement is obviously true.

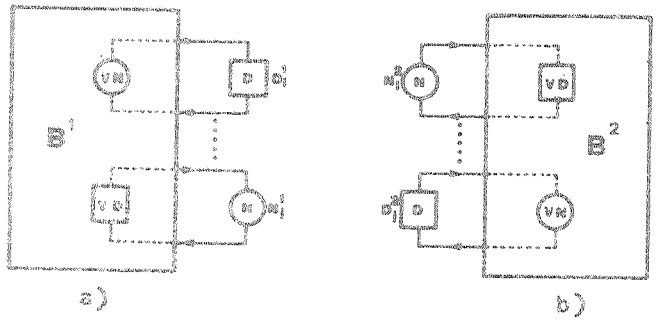
The previous Statements suggest constructing larger nets by merging Not elements and Delay elements of two smaller nets, as stated in the next Definition.

Definition 10. Let A^1 be a net constituted by a set B^1 of elements, by r Delay D^1_i, $i = 1,2,\ldots,r$, and by s Not N^1_j, $j = 1,2,\ldots,s$, where $r+s \geq 1$. Let A^2 be a net constituted by a set B^2 of elements, by r Not N^2_i and by s Delay D^2_j. If there are two states S^1_a and S^2_b of A^1 and A^2, respectively, such that the value of the input variable of D^1_i (N^1_j) is equal to the value of the output variable of N^2_i (D^2_j), and the value of the output variable of D^1_i (N^1_j) is equal to the value of theinput variable of N^2_i (D^2_j), then A^1 and A^2 are two *connectible nets* with respect to the states S^1_a and S^2_b. The net A obtained from A^1 by substituting all the elements D^1_i and N^1_j with B^2, or, it is the same, obtained from A^2 by substituting all the elements N^2_i and D^2_j with B^1, will be denoted by $B^1 \cup B^2$. The state of A in wich the values of the internal variables and of the output variables of the elements of B^1 (B^2) are equal to the values of such variables in S^1_a (S^2_b) is denoted by $S^1_a \cup S^2_b$.

Theorem 1. Let A^1 and A^2 be two connectible nets with respect to S^1_a and S^2_b. If A^1 and A^2 are self-regulating and persistent with respect to S^1_a and S^2_b, respectively, then $A = B^1 \cup B^2$ is self-regulating and persistent with respect to $S_c = S^1_a \cup S^2_b$.

Proof. Starting from S_c, the net A can be regarded as formed by B^1 (B^2) connected to r (s) Virtual Delay and s (r) Virtual Not.

Then A differs from A^1 (A^2) only in the substitution of Delay and Not elements by means of the corresponding virtual elements. Therefore, every element of B^1 (B^2) is well-driven and all its output variables are persistent in A with respect to S_c (Statement 3). Then A is self-regulating and persistent with respect to S_c.



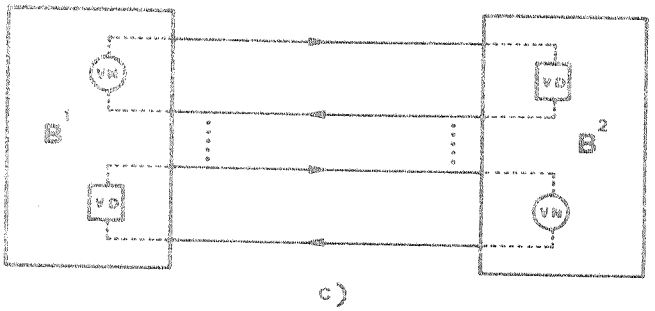
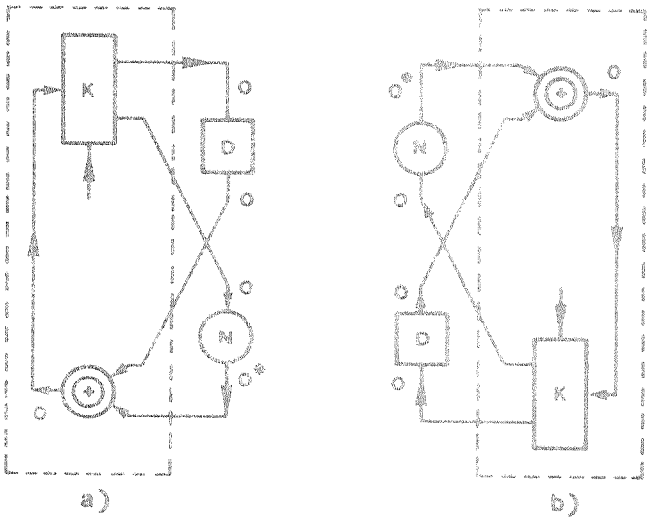


Fig. 7. a) Net A^1
b) Net A^2
c) Net $A=B^1 \cup B^2$

The nets given in Figs. 8a), 8b) and in Figs 9a), 9b), satisfies the hypotheses of Theorem 1. The nets in Fig. 8c) and 9c) then satisfy the theorem theses. Note that Theorem 1 can not be generalized to include the liveness property. In fact the net in Fig. 8c) is not live, with respect to the state shown in the figure, even if the nets in Figs 8a) and 8b) are live with respect to the states in which the nets are connected. A sufficient condition that assures the preservation of the liveness property is stated by the following Theorem.

Theorem 2. Let A^1 and A^2 be two connectible nets with respect to S_a^1 and S_b^2, and let $\alpha+\beta=1$. If A^1 and A^2 are self-regulating, persistent and live with respect to S_a^1 and S_b^2, respectively, then $A = B^1 \cup B^2$ is self-regulating, persistent and live with respect to $S_c = S_a^1 \cup S_b^2$.

Proof. Due to the Theorem 1, A is self regulating and persistent with respect to S_c. Let S_d be a state such that S_d is equal to S_c or S_d is a successive state to S_c, and let S_e^1 (S_f^2) be a successive state of S_a^1 (S_b^2) such that the value of each internal and output variable of every element of B^1 (B^2) is equal in S_e^1 (in S_f^2) and in S_d. Let Z_w^h be an output variable of an element of B^1 (B^2). Consider the net A^1 (A^2). As A^1 (A^2) is live with respect to S_a^1 (S_b^2), then there exists at least one combination of the parameter values Φ^1 (Φ^2) for which Z_w^h becomes excited in a finite time, with A^1 (A^2) starting from S_e^1 (S_f^2). Consider the



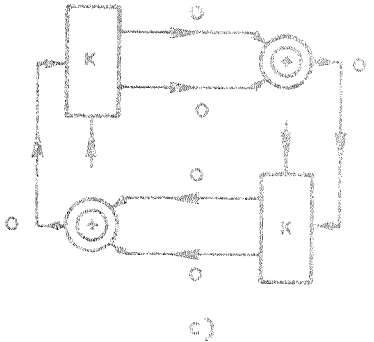
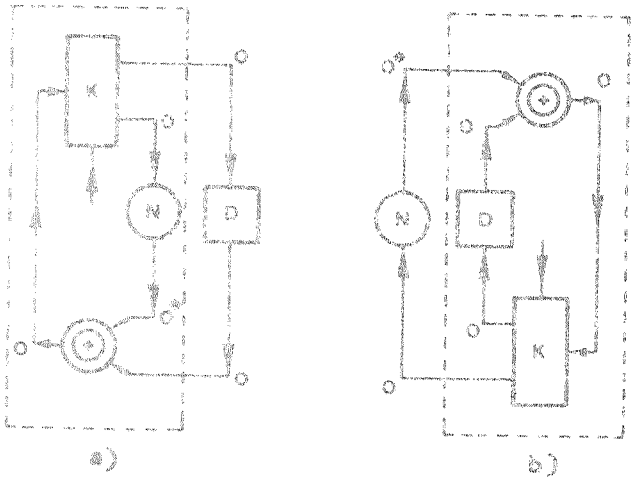


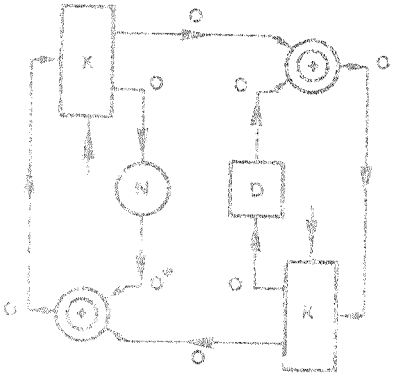
Fig. 8.

net A^2 (A^1). As A^2 (A^1) is live with respect to S_b^2 (S_a^1), then there exists at least one combination of the parameter values Φ_{eq}^2 (Φ_{eq}^1) for which B^2 (B^1) behaves as an element. Consider the net A. The variable Z_w^h becomes excited in a finite time, with A starting from S_d, if the parameter value combination is Φ^1, Φ_{eq}^2 (Φ^2, Φ_{eq}^1). Then A is live with respect to S_c.

The nets given in Figs 9a) and 9b) satisfy also the hypotheses of Theorem 2. Then the net in Fig. 9c) satisfies the theorem theses.



a) b)



c)

Fig. 9.

CONCLUSIVE REMARKS

In this paper asynchronous sistems constituted by asynchronous circuits are considered. An abstract model of an asynchronous circuit is given in order to analyze some system properties, such as self-regulation, persistence and liveness. Conditions are given that allow us to obtain a larger system starting from two smaller ones, preserving the above properties. The interconnection of several systems can be accomplished iteratively, by interconnecting two systems at a time.

The considered systems do not include circuits that perform an arbitration function. In fact, it can be verified that such systems result non self-regulating. Investigations about non self-regulating systems are made in [6].

Some other properties, such as determinacy of self-regulating and non self-regulating systems are under investigation

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