Nanowire-based architectures for the detection of THz radiation

Miriam S. Vitiello[a], Alessandro Pitanti[a], Frederic Teppe[b], Dominique Coquillat[b], Leonardo Viti[a],
Daniele Ercolani[a], Lucia Sorba[a], Wojciech Knap[b], and Alessandro Tredicucci[a]
[a] NEST, Istituto Nanoscienze – CNR and Scuola Normale Superiore, Piazza San Silvestro 12, 56127 Pisa (Italy)
[b] Université Montpellier2 – CNRS, Place E. Bataillon, 34950 Montpellier (France)

***Abstract*—Self-assembled nanowires represent a new interesting technology to be explored in order to increase the cutoff frequency of electronic THz detectors. They can be developed in field effect transistor (FET) and diode geometries exploiting non-linearities of either the transconductance or the currentvoltage characteristic as detection mechanism.**

I. Introduction And Background

ONE-DIMENSIONAL (1D) nanowires are at the forefront of studies on future electronics, although issues like massive parallelization, doping control, surface effects, and compatibility with silicon industrial requirements are still open challenges[1]. On the other hand, significant progress is being recently made in atomic to nanometer scale control of materials morphology, size, and composition, including the growth of axial, radial, and branched nanowirebased heterostructures[2].

Nanowires can be easily removed from the host substrate and placed on top of a new functional one for individual contacting, even in relatively large numbers, with a simple planar technology very suitable for low capacitance circuits. Therefore, they represent, in principle, an ideal building block for implementing rectifying diodes or plasma-wave detectors that could be well operated into the Terahertz, thanks to their typical attofarad–order capacitance. Surprisingly, though, despite the strong effort in developing these nanostructures for a new generation of complementary metal-oxide semiconductors (CMOS), memory and/or photonic devices, their potential as Terahertz radiation sensors has not been explored so far.

In this paper we first investigate three-terminal nanowire FETs using lateral gating for operation as plasma wave THz detectors through the non-linear transconductance response[3]. These are realized in InAs material to take advantage of the low effective mass and better mobilities achievable in this compound. The narrow bandgap and degenerate Fermi-level pinning further allows for easy formation of excellent ohmic contacts. Beyond the low capacitance advantage expected of nanowire FETs, 1D systems are also predicted to show better responsivities due to the fact that only one longitudinal plasmon mode can couple to the oscillating radiation field. In this first generation of devices we already demonstrate excellent room-temperature operation at 300 GHz and above.

We then consider how two-terminal diodes can be implemented within nanowires, displaying strongly non-linear current-voltage characteristics for the rectification of the incoming THz radiation. In particular we focus on broken-gap InAs/InSb n-type heterojunctions, in which majority carriers dominate transport, ensuring negligible influence of slow carrier recombination. We also discuss how Schottky devices can be practically implemented within individual thin Si wires, with junctions diameters below 10 nm for extremely low capacitance[4].

The concept of nanowire junctions can also be combined with lateral gating to achieve tunable barriers, which can be useful to engineer the non-linearity to be as close as possible to zero bias, in order to decrease the device noise, or to enhance the transconductance non-linearity in plasma-wave FET detectors. Finally we show the electric manipulation of electronic levels in InAs/InP nanowires[5] and discuss the potential for a THz detector in the Coulomb blockade regime at elevated temperatures.

II. Results

In order to fabricate our FET-based nanowire detectors 1.5 μm long InAs nanowires having a 30 nm diameter, were grown bottom-up on InAs(111)B substrates in a Chemical Beam Epitaxy (CBE) system. A 0.5 nm thick Au film was first deposited by thermal evaporation on the InAs wafer and subsequently annealed at 520°C in order to remove the surface oxide and produce the necessary catalytic Au nanoparticles by thermal de-wetting. Se-doping in the 10^{16} cm^{-3} is used to control the charge density, optimizing source-drain and contact resistance, while ensuring sharp pinch-off in the transconductance.

The nanowires were then mechanically transferred to a 350 μm thick Si substrate (afterwards thinned to about 120 μm) with a 500 nm SiO_2 insulating surface layer, and individually contacted using a combination of optical and ebeam lithography. Surface oxides must be removed and the InAs contact areas have to be passivated before contact metal deposition to prevent re-oxidation, a processing step really crucial for an optimal electrical behavior of the devices, due to the high surface- to-volume ratio of the nanowires. Ohmic contacts have been then realized, taking care of making negligible the potential barrier with InAs using a metal layer whose work function is smaller than the electron affinity of the semiconductor. In the case of InAs, a Ti(10nm)/Au(90nm) proved suitable.

Different detector designs have been realized by varying the geometry of the contact patterns and/or the mounting configuration. Specifically, to increase the asymmetry and therefore the responsivity, we designed as source and gate

electrodes low shunt-capacitance antenna structures to funnel the radiation into the strongly sub-wavelength detecting element (see fig. 1). A set of devices exploiting different antenna geometries have been realized: i) broad band bow-tie antennas with arm lengths in the range 100-250 µm, ii) wide band log-periodic circular-toothed structures, with an outer diameter of 650 µm, iii) control structures with the antenna arms between source and drain.

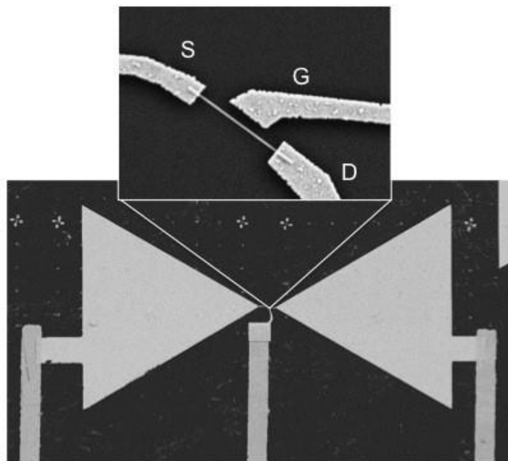

Fig. 1. SEM picture of a fabricated nanowire FET detector with bow-tie antennas. The blow-up shows the InAs nanowire element with the source, drain, and gate electrodes.

In all cases the gate electrode was lithographically designed to be 80-100 nm away from the InAs nanowire, with a channel length in the range 300-500 nm. Each sample was finally glued on a dual-inline package and wire bonded. In a few devices a Silicon hyper-hemispherical lens having a 6 mm diameter was mounted on the back of the Si substrate so that the GHz beam is properly focused on the nanowire after crossing the Si/SiO_2 layers.

The electrical characterization was performed connecting the drain contact to a current amplifier that converts the current into a voltage signal amplified by a factor of about 10^4 V/A. An ohmic behavior was observed at room temperature, while sweeping the V_{sd} voltage applied to the nanowire from 0.025eV to 0.025eV and while varying the gate voltage from -10V to 10V. At high gate voltage > 7 V), the resistance R_d was in the range of a few K and increased up to about 30 k in the subthreshold region, i.e. at gate voltages V_g lower than the voltage pinch off value V_t. Photoresponse experiments were performed by using an electronic 292 GHz source based on frequency multipliers. The radiation was collimated and focused by off-axis parabolic mirrors and mechanically chopped at 333 Hz, with the photo-induced drain current measured after the amplifier with a lock-in technique. Experiments were performed at zero source-drain bias with the source grounded.

Fig. 2 shows the room temperature responsivity values measured on a device with bow-tie antenna while the 292 GHz beam impinges on the substrate through the silicon lens. Note the difference of more than one order of magnitude, depending on the polarization direction, indicating the correct operation of the antenna geometry. As predicted for plasma wave detectors, the highest responsivity is achieved near the pinchoff voltage. Furthermore, no signal could be detected in the control devices ruling out any bolometric effects. As expected, log-periodic antennas in general yielded better performance than bow-tie, and devices with a Si lens showed an improved collection efficiency of more than one order of magnitude. The noise performance was evaluated using a spectrum analyzer and, in the best devices, noise equivalent powers already lower than 10^{-11} W/Hz$^{1/2}$ could be obtained.

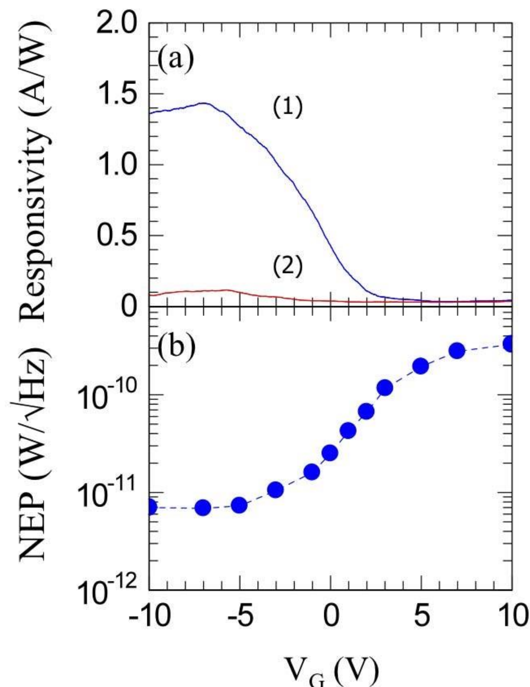

Fig. 2. (a) FET detector responsivity at ~ 300 GHz as a function of applied gate bias. Line (1) refers to the electric field of the incoming radiation polarized parallel to the antenna axis, while in (2) it is orthogonal. (b) Noise equivalent power as a function of gate bias as deduced from the responsivity and the detector noise measured in the absence of radiation with a spectrum analyzer.

InAs/InP nanowire quantum dots can also be grown to realize single-electron Coulomb-blockade transistors (SETs), showing extremely steep source-drain conductance variation with applied gate voltage up to liquid nitrogen, which could lead to huge THz responsivities.

In order instead to realize a two-terminal THz nanowire diode, a structure with a proper asymmetric junction within the wire itself is needed. We make use of a sharp axial heterojunction, achieved by faceting two n-type materials, namely InAs and InSb, whose band lineup is of type-III (broken gap). It is interesting to note that, while InAs/InSb bulk heterostructures are difficult to grow due to the large lattice constant mismatch (~ 6%), the feasibility of heterostructured nanowires indeed has been demonstrated in the last few years. Only the precursor of the group V element has to be switched during growth, with the possibility of growing very long nanowires without the need of any insertion layer and, when InSb is grown on an underlying InAs segment, of obtaining a sharp interface between the two materials. Moreover, the majority carriers are the same in both semiconductors (n-type), granting good ohmic contacts of two-terminal devices in a single lithographic step. This property is also appealing for high-speed operation as minority carriers are not expected to contribute significantly to transport, thereby avoiding issues

related to slow recombination times. The broken gap alignment, while not necessary, ensures that a strong charge-induced band bending, in our case of the order of the InSb gap, takes place, resulting in a relevant depletion region compensated by charge accumulation on the other side of the interface. A triangular barrier is formed, which leads to the transport asymmetry, analogously to the known behavior of the Schottky barrier at a metal semiconductor interface. Growth and fabrication proceeded along the lines already described for FETs and a scheme of the diode electrical measurements is reported in Fig. 3 together with a SEM picture of a typical device.

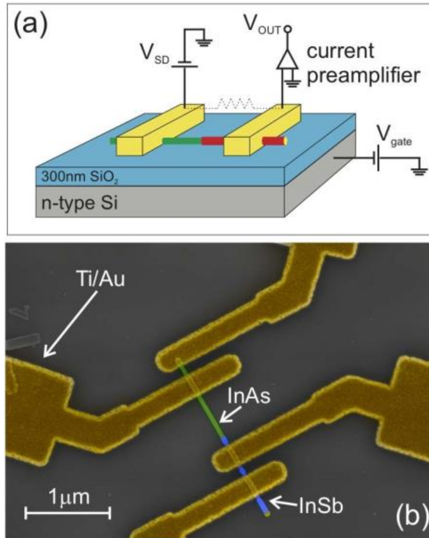

Fig. 3. (a) Schematic of an InAs/InSb nanowire device and sketch of the experimental circuit realized to probe the device transport properties. (b) SEM image of a contacted nanowire. The colors are artificially added to enhance the picture clarity.

A tuning element for the transport is offered by the possibility to grow a thin (3-5 nm) InP barrier in between InAs and InSb. Fig. 4 displays the room temperature current voltage characteristics of diodes with and without InP barriers. A nice diode-like behavior is observed with low-bias transport dominated by the thermionic contribution; devices with the InP barrier then show a much-improved rectification. Estimates of the device responsivity as detectors can be obtained by ratioing the curves second- and first-order derivatives, giving values of the order of few A/W. Real detector devices with appropriate antennas are being developed, but this also requires optimization of the doping to reduce the series resistance and to carefully tune the bias operating point near zero.

Alternatively, single-crystalline Si nanowires with uniform diameters down to 3 nm can been grown by the vapor liquid solid growth mechanism and nanowire segments transformed into metallic silicides in a thermally assisted solid-state reaction; atomically abrupt metal to Si Schottky junctions can thus be formed. The junction area is accordingly defined by the nanowire diameter. Typical diode characteristics are current densities surpassing $1x10^6$ A/cm^2 at 1 V bias and subfemtoFarad capacitances. Through external gating, charge carrier injection can be tuned between thermionic emission and quantum mechanical tunneling with high efficiency; by this method, the diode ideality factor can be externally adjusted.

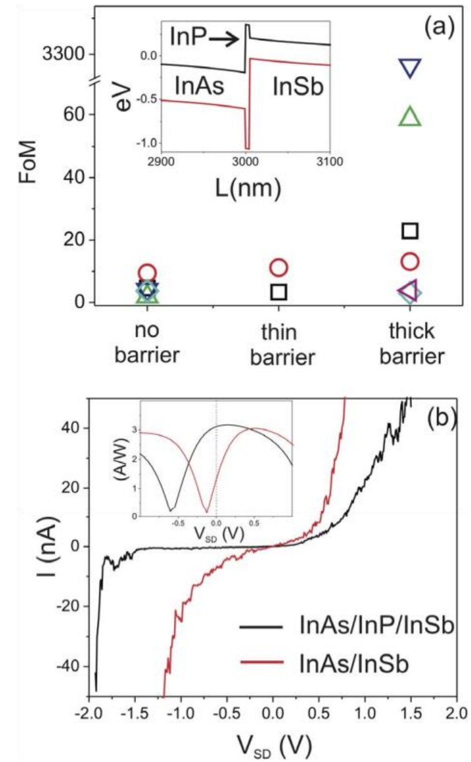

Fig. 4. (a) Figure-of-merit (ratio between on- and off-current at 0.5 V bias) for InAs/InSb and InAs/InP/InSb nanowires, where thin (2.5nm) and thick (5nm) InP insertions have been considered. Inset: qualitative band alignment of the heterostructure. (b) Room temperature rectification comparison for devices with and without InP (thick barrier). Inset: second to first order current derivative ratio for the device with and without InP.

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