Die-Attach Influence on Thermal/Electrical Parameters of GaN RF Device

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***Abstract*—This paper presents a comprehensive study on the relation between die-attach and thermal/electrical parameters of GaN RF devices. This correlation is investigated through Multiphysics simulations and experimental data. Particularly, thermal analysis is performed by means of Quantum Focus Instrument (QFI) Infrascope able to detect the surface temperature of the device. Then, 3-D finite element method thermal simulations are performed to support the observed heat distribution. A strong association between drain current drift and temperature escalation is demonstrated by comparing two devices with significantly different die-attaches. Particularly, we observe an increase in the drain current with increasing self-heating effects, conversely to what generally expected for thermal derating. However, this correlation is then explained thanks to the analysis of threshold voltage shift with temperature that supports the experimental evidence.**

***Index Terms*—GaN HEMTs, IR, thermal analysis, 3-D finite element method (FEM) thermal simulation.**

I. Introduction

GALLIUM Nitride (GaN) technology has emerged as a promising candidate for high-frequency, high-power electronic applications due to its superior material properties such as high electron mobility, high breakdown voltage, and thermal conductivity [1], [2]. In the realm of radio frequency (RF) devices, GaN-based transistors have shown remarkable performance, offering higher efficiency and power density compared to traditional semiconductor technologies like Silicon (Si) [3]. However, the operation at high power densities typically yields temperature increase due to Self-Heating Effects (SHE) that could significantly impact the performance and reliability of GaN RF devices.

Various methods and studies have been conducted to understand and address these aspects [4], [5], [6], [7]. In this scope, die-attach serves as a crucial interface between the GaN transistor chip and the package substrate, ensuring efficient thermal management and electrical connectivity [8]. Accordingly, the die-attach material and process parameters play a significant role in determining the overall electrical characteristics and thermal behavior of GaN RF devices [9], potentially affecting their performances and long-term reliability. Specifically, the characteristics that exhibit this temperature-dependent behavior not only make the device unreliable but also impair its performance in terms of gain, power, and efficiency. These parameters are crucial for developing a best-in-class power amplifier (PA).

Despite previous literature already addressed the impact of die attach on efficiency losses in RF GaN devices [10], a comprehensive investigation into the die-attach influence on both thermal and electrical parameters has not been reported so far. Our objective is not to determine the absolute peak temperature, for which micro-Raman or thermoreflectance methods are more accurate, but rather to obtain a reliable estimate of the average temperature and its distribution across the device. This information is crucial for understanding the thermal-electrical interplay, particularly how different die-attach materials affect self-heating and electrical behavior under operating conditions.

For this reason, in this paper, we aim to study the effect of two different die-attach on two identical devices, highlighting the role of the conductive paste in altering the thermal behavior and thus the electrical characteristics of the devices.

Particularly, to establish a correlation between electrical performance degradation and device overheating, infrared (IR) measurements were conducted to determine the surface temperature of the devices during operation [11], [12]. This data is fundamental for understanding the thermal behavior of GaN RF devices and its impact on electrical performance degradation.

Understanding the intricate interplay of die-attach properties, specifically thermal boundary resistance and thermal conductivity, with electrical performance is essential for optimizing GaN RF device design and fabrication processes. For this reason, it is important to perform thermal Multiphysics simulation to verify and validate the results coming from the experimental analysis.

The paper is organized as follows. Section II provides an initial presentation of the geometric and structural characteristics of the Devices Under Test (DUTs). Additionally, the I_D-V_D curves of the two DUTs are reported to highlight

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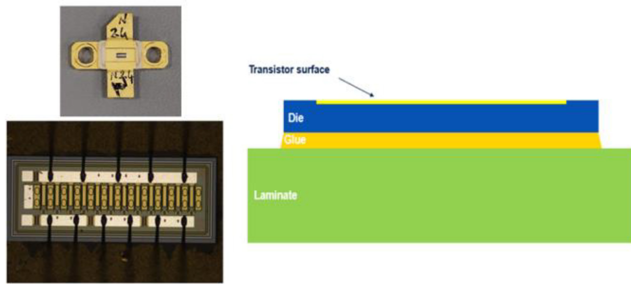

Fig. 1. Device tested, microscope image and cross-section. Two different glues are being used for die-attach.

the electrical difference between the samples. Section III thoroughly describes the IR measurement technique and how the measurement setup was used to thermally characterize the packaged devices under consideration, along with the thermal results obtained. Section IV reports the data obtained with Multiphysics simulations performed with Comsol [13]. In Section V, we present the comparison between the experimental and simulation results and the analysis of the threshold voltage shift with temperature is used to explain the electrical behavior experienced by devices with different die-attach. Finally, the conclusions are drawn in the last section.

II. Devices Tested and Electrical Characterization

Devices Under Test (DUTs) are AlGaN/GaN HEMT grown on Silicon substrate. GaN Buffer was Carbon doped to increase the breakdown voltage [14], whereas normally-on operation is obtained by means of Schottky gate [15] on top of single AlGaN/GaN heterojunction. The two devices considered have the same geometrical and material properties except for the die-attach (i.e., glue), which is present between the back of the device and the package. Particularly, tested devices have an overall gate width of 24x250 μm, yielding a total periphery of about 6 mm. The gate length is lower than 0.5 μm, while the gate-drain and gate-source length are about 4 μm and 1 μm, respectively. In this work, the total length of the device, housed in a traditional M243 package, is approximately 2 mm. An IR measurement was performed on it, allowing us to obtain the temperature profile along the entire length of the device (see next section). As already mentioned, the only difference between the two samples is the glue and, more in detail, the glue's thermal conductivity. Indeed, according to datasheets, sample A uses a glue with 140 W/mK whereas sample B has a second glue of 1.8 W/mK at 121 °C [16], [17]. It's crucial to highlight that the thickness of the glues was maintained equal, ensuring that the difference in performance can be attributed to the thermal conductivity properties of the two die attaches. Particularly, in both cases the die-attach thickness is slightly lower than 20 μm, but equal between each other. The adhesive thickness measurement was obtained through 3D spatial analysis using the Sensofar S Neox confocal interferometric system. The analysis was performed at 20x magnification, enabling a thorough examination of both the device and adhesive thickness.

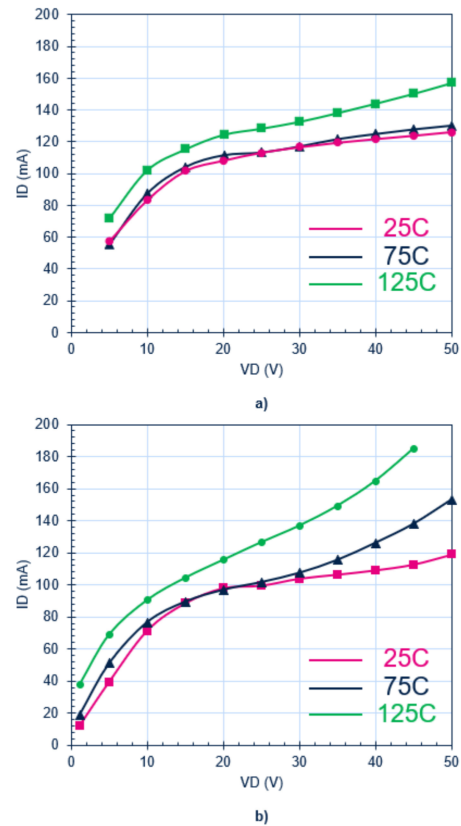

Fig. 2. Output characteristics I_D-V_D of two identical devices with different conductive glues: a) Sample A with high thermal conductivity glue, b) Sample B with lower thermal conductivity glue.

Figure 1 depicts the assembled device that will undergo thermal mapping acquisition, an image of the various gate fingers and device constitution under the microscope, and finally, a cross-section detailing the package and the layer of adhesive required for perfect adherence. First, the two samples are electrically characterized on thermal chuck to analyze the drain current versus drain voltage (I_D-V_D) behavior at different temperatures. As we can see in Fig. 2, the I_D-V_D are obtained by sweeping the drain voltage with 5 V steps, starting from 50 V to 5 V. The gate voltage is kept constant (sample A: V_{GS}=−1.838 V and sample B: V_{GS}=−1.7528 V) for all the three temperatures (25 °C, 75 °C and 125 °C) imposed by the thermal chuck. To find this value, we have performed a first measurement, after an initial stabilization phase, in which we set the drain voltage at V_{DS}=50 V and, by increasing the gate voltage, we reach 120 mA of drain current, which means 20 mA/mm for our devices at a chuck temperature of 25 °C. This value of current is very important to guarantee that the operation region for the two devices is the same. Found this value of gate voltage, we keep it constant for all the other measurements on said device. The output characteristics show immediately a significant difference between the two samples: Sample A shows a flatter behavior until 75 °C, while an I_D ramp-up starts to be observed at 125 °C as T increases. These two different behaviors are already signature of an important fact: the die-attach strongly affects the electrical characteristics (e.g., the I_D-V_D) of the devices under test at working operation

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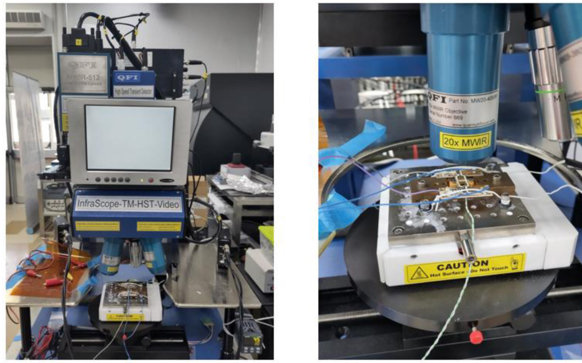

Fig. 3. InfraScopeTM Temperature Mapping Microscope and arrangement utilized to perform thermal characterization on GaN devices.

condition. In the next section, a thermal analysis is performed to highlight the reason for this experimental evidence.

III. IR Measurements

To further correlate the current drift (i.e., I_D ramp-up) to a thermal issue, thermal measurements were needed. Among the large variety of methods available to this end, we have chosen to make IR measurement through the QFI instrumentation. This choice was led by the opportunity to have, in this way, the temperature profile over the whole device length. This is a fundamental aspect to understand how heat is distributed through the device.

The IR measurement setup is organized as follows. The device enclosed within the package is firmly secured in place using two screws strategically positioned on the fins of the device. These screws serve dual purposes: they fasten the device to the copper plate located beneath it, which facilitates heating to the desired initial temperature, and they establish contact with the necessary contact card for device polarization. Moreover, a thermocouple positioned at the center of the copper plate in direct contact with the M243 package back side through a light layer of thermal conductive past continuously monitors the actual temperature at the back of the device, ensuring precise temperature measurement. Finally, voltage and current generators, in conjunction with multimeters, are utilized to finely adjust the measurement conditions.

Additionally, the ocular of the thermal imaging camera is carefully positioned on top of the decapsulated package devices, providing a clear view for thermal analysis. To enhance accuracy, the QFI temperature mapping software employs automated emissivity correction algorithms, resulting in the generation of a comprehensive temperature map. In Fig. 3, it is possible to appreciate the arranged bench for the measure.

Thanks to this instrumentation, it is possible to acquire thermal maps using the InSb camera at 5X magnification. After this first measure, which permits to see the variation of the temperature over all the device and then to understand which is the hottest area, we change the camera (20X magnification) by putting ourselves in that position, since we are interested to find the highest temperature at which these devices lead themselves to. Moreover, the camera with 20X magnification performs a more accurate and resolute measure of the temperature.

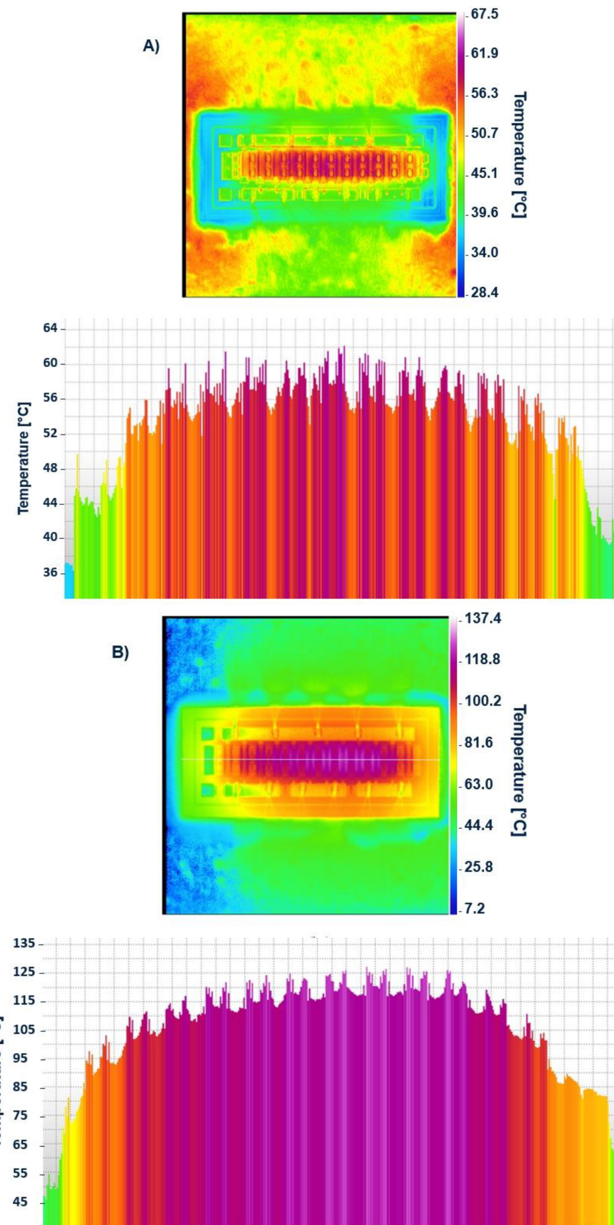

Fig. 4. Comparison of the IR thermography temperature maps and profiles temperature of two different devices with different conductive pastes, both operating at 6W. Thermal maps are realized with an InSb camera at 5X magnification, with identical conditions for the two samples, except for the gate voltage: Tbase-plate=25°C, V_{DS}=50V, I_D=120mA/mm and A) Sample A with $V_{GS=}$−1.838V, B) Sample B with V_{GS}=−1.7528V.

From Figure 4, we observe the dynamic evolution of the temperature profile within the device. As anticipated, the highest temperature concentrations manifest at the center due to the device's limited heat dissipation capabilities. Conversely, as we progress towards the external gate fingers, temperatures decrease gradually, thanks to lateral as well as vertical heat dissipation. Upon closer examination of two identical devices, differing only on the glue used to attach them with the package substrate, a stark contrast in peak temperature levels

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TABLE I
THERMAL CONDUCTIVITIES OF DIFFERENT LAYERS

Layer	Material	κ [W/m·K]
Contacts	Aluminum	235
Passivation	SiN	3[a]
Barrier	AlGaN	10[b]
Buffer	GaN	$160\times(300/T[K])^{1.4}$ [c]
Substrate	Silicon	$148\times(300/T[K])^{1.28}$ [d]
Flange	CuW	170
Die attach (case A)	Glue A High conductivity	120 (measured by Raman)
Die attach (case B)	Glue B Low conductivity	1.8 @120°C (from datasheet)

a [H. Ftouni, C. Blanc, D. Tainoff, A. D. Fefferman, M. Defoort, K. J. Lulla, J. Richard, E. Collin, O. Bourgeois “Thermal conductivity of silicon nitride membranes is not sensitive to stress”, Phys. Rev. B 92, 125439, Sep. 2015] ,

b [A Filatova-Zalewska et al., “Anisotropic thermal conductivity of AlGaN/GaN superlattices”, Nanotechnology 32, 2021],

c [A. Sarua, H. Ji, K. P. Hilton, D. J. Wallis, M. J. Uren, T. Martin, and M. Kuball, “Thermal boundary resistance between GaN and substrate in AlGaN/GaN electronic devices”m IEEE Trans. Elec. Dev. vol. 54, no. 12, dec. 2007],

d [C. J. Glassbrenner, G. A. Slack, “Thermal Conductivity of Silicon and Germanium from 3°K to the Melting Point”, Phys. Rev. 134, A1058, may 1964].

becomes evident. Specifically, sample A registers a maximum temperature of 63.8 °C (based on data acquired using the highest resolution camera available), whereas sample B peaks at 121 °C when subjected to identical testing conditions. This disparity underscores the significant impact of the conductive paste on thermal performance.

IV. THERMAL SIMULATIONS

In order to verify and validate the results coming from IR analysis, some thermal simulations are carried out. Comsol Multiphysics is used for the 3-D finite element method (FEM) thermal simulation of the device under test. The model includes the die, die-attach and package flange. Table I contains thermal conductivities of each layer in the device/package stage. Joule heating is applied in the model as a heat emission surface load at the AlGaN/GaN interface, representing the high electric field region in the (2-Dimensional Electron Gas) 2-DEG. TCAD simulation is used to determine the Joule heating spatial distribution [18]. The system is considered isolated and the symmetry conditions are applied [19]. The two-dimensional device simulator used is ATLAS by Silvaco Inc. [22].

The thermal contribution is calculated turn-on the module GIGA, which extends ATLAS for lattice heat flow and for the dependence of material and transport parameters on the lattice temperature. For GaN-compound material, a temperature dependent thermal conductivity is considered based on table I. The heat capacitances are 3.0135 J/cm3/K and 2.37761 J/cm3/K for GaN and AlN, respectively [22]. The

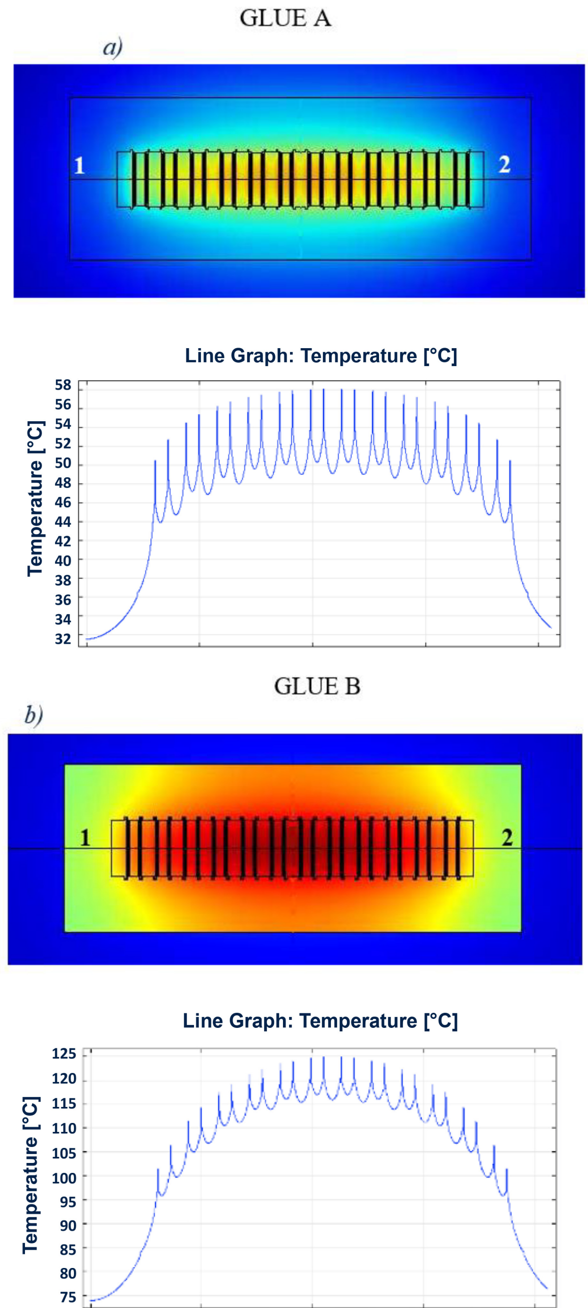

Fig. 5. Thermal simulation with the two different glues, at 6W and Tcase=25°C. a) Cutplane at the top of the device and transversal cutline along AB direction when the device is attached with a glue with high thermal conductivity instead case b) Cutplane and cutiline in the case of the glue with low thermal conductivity.

Silicon substrate final thickness was also included in the simulation set-up. Thermo-electrical simulation was performed at 1W/mm with the following biasing conditions V_{DS}=50V, I_D=20 mA/mm.

Different dissipated powers are simulated in order to reproduce the experimental data and, for each dissipated power, T_{case} (temperature at the bottom of the device) is swept from 25 °C to 150 °C. These simulations have been carried out for glue A and glue B, both with thickness of 20 um. In Figure 5 are reported the results coming from simulations in the same

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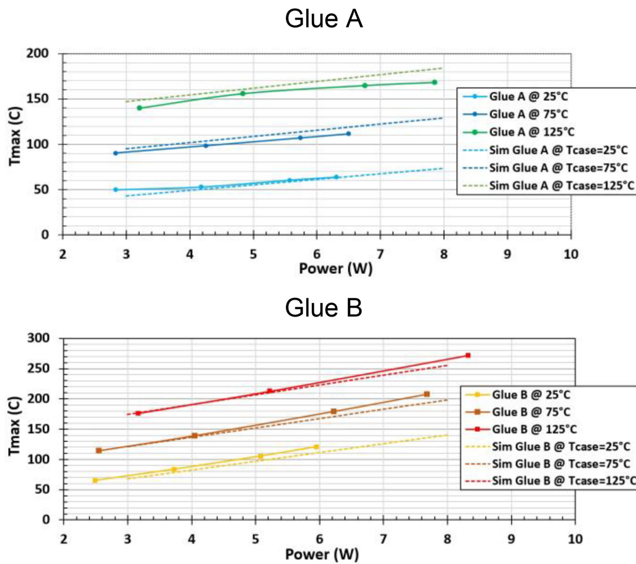

Fig. 6. Comparison of maximum surface temperatures obtained by IR thermography by increasing drain voltage and operating power and the correspondent thermal simulations (dashed lines). Higher values are obtained die attach B, with lower thermal conductivity.

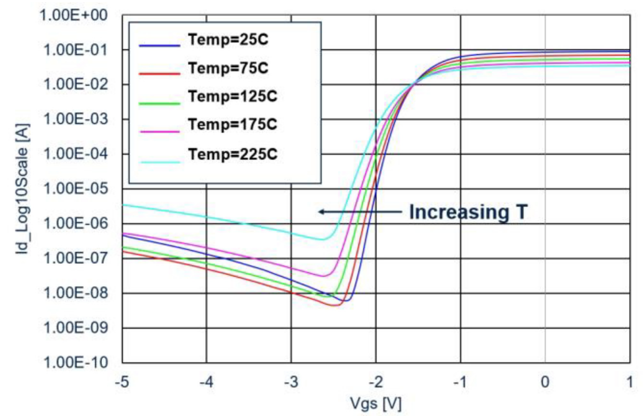

Fig. 7. I_D-V_{GS} normalized characteristics (logarithmic scale) of tested devices. One can see how the threshold voltage decreases while increasing the base-plate temperature and thus a higher drain current.

condition as Figure 4. As we can see in Figure 5 either from cut-planes that from cutlines, of both samples, the results obtained by Multiphysics simulation are in accordance with the IR analysis. Particularly, higher maximum temperature is detected with Glue B with respect to Glue A.

V. Results and Discussion

Figure 6 illustrates the significant difference in behavior between the two devices, notably showcasing the temperature trend relative to the power dissipation. The power range fluctuates between 2 W and 9 W, corresponding to operating conditions ranging from 0 V to 50 V drain voltage with a constant gate voltage. Initially, V_{GS} is set to ensure standard operating conditions (temp=25 °C, V_{DS}=50 V, I_D=120 mA). Subsequently, V_{GS} remains constant for all following measurements conducted at varying temperatures.

The graph shows three distinct curves for each device, each corresponding to the base plate temperatures during testing. It is evident from the data that device B consistently reaches significantly higher temperatures compared to device A. These results are confirmed by simulations (dotted lines) performed in the same condition of the IR measurements. The discrepancy in temperatures can be attributed to inadequate heat dissipation, primarily caused by the die attach, despite both devices being identical in other aspects. As power dissipation increases, the lower heat dissipation capabilities of device B become more pronounced when compared to device A. These results underline the critical importance of optimizing heat dissipation mechanisms in the context of GaN RF devices, to optimize electrical and reliability performances in radio frequency applications.

In the latter segment of our investigation, we directed our attention towards a possible explanation for the observed current drift phenomenon in Device B (see Figure 2). This involved delving into the intricate interplay between temperature fluctuations and electrical behavior. The observed correlation between temperature and current dynamics can be comprehensively expounded through the complex mechanism of threshold voltage modulation induced by thermal effects [20]. As the device operates and encounters varying thermal environments, the dissipation of power increases, resulting in localized self-heating within the device structure. This self-heating phenomenon is especially exacerbated by the suboptimal thermal conductivity properties of the adhesive material used in the device-packaging interface. Consequently, this thermal energy influx is the cause of a gradual alteration in the threshold voltage.

The empirical findings presented in Figure 7 serve as a tangible manifestation of this thermal-induced threshold voltage shift. At an ambient temperature of 25 °C, the measured threshold voltage stands at −2.2 V; however, as the temperature is increased to 225 °C, an observable decrease in the threshold voltage to −2.6 V is documented. This negative voltage shift underscores the complex sensitivity of device performance to thermal stimuli, thereby supporting the established correlation between temperature and electrical behavior. This effect can be better summarized as follows. The device is biased at constant gate voltage V_{GS}, which results in a given overdrive voltage (V_{OV}=V_{GS}-V_{TH}) at 25 °C. As temperature increases, the threshold voltage drops, thus increasing the overdrive from the previously mentioned V_{OV}.

This variation in V_{OV} significantly affects the drain current since the chosen V_{GS} is close to the point at which the transconductance (g_m) peaks [21].

Accordingly, a negative threshold voltage drift (i.e., overdrive increase) in this V_{GS} range causes a strong rise in the current for device B, where the thermal rise and the consequent decrease in V_{TH} are more pronounced.

VI. Conclusion

Within this study, AlGaN/GaN High Electron Mobility Transistors (HEMTs) on Si substrate have been subjected to thorough investigation from both thermal and electrical perspectives. Specifically, by monitoring the surface temperature

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of a packaged device, we have successfully delineated a compelling correlation between temperature escalation, induced by device overheating under standard operational conditions, and the resultant current flow within the device. Notably, this observed current drift phenomenon can be attributed to a negative shift in the threshold voltage, thereby facilitating enhanced device conduction and subsequent increase of drain current.

The study has been made possible through the utilization of advanced instrumentation, namely the Quantum Focus Instrument (QFI) instrumentation. Leveraging the capabilities of QFI instrumentation, we have been able to conduct a comprehensive thermal analysis of the devices under study.

This investigation underscores the fundamental role of temperature management in dictating the operational stability and performance reliability of AlGaN/GaN HEMTs. By clarifying the relationship between temperature fluctuations and electrical behavior, this study not only enhances our fundamental understanding of semiconductor device dynamics but also points out the need to optimize the die-attach properties for achieving good device performance and longevity in real-world applications.

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