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Extraction of Defects Properties in Dielectric Materials From I-V Curve Hysteresis

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Abstract-Atomic defects in high-k materials affect the performance, reliability, variability, and scaling potential of electronic devices. Their characterization is thus of paramount importance, and methods exploiting electrical measurements are highly demanded. In this work we present a novel method for extracting the defect properties from I-V curve hysteresis measured at low electric field in thick metal-insulator-metal (MIM) stacks. The I-V curve hysteresis allows detecting the defects located near the electrode-insulator interfaces and aligned with the stack Fermi level, and extracting their properties. The defects are profiled cross-correlating the information provided by the low-field current hysteresis and the high-field steady-state current. This technique can be applied to MIM stacks fabricated in Back-End-of-Line for capacitors, embedded memories and thin film transistors.

Index Terms—Atomic defects, charge trapping, defects characterization, high-k dielectric, metal-insulator-metal stack

I. INTRODUCTION

THE electrical response of dielectric materials is greatly affected by the atomic defects due to lattice distortion, interfaces, grain boundaries, amorphous phase of materials and impurities. Defects affect the devices performance (e.g. leakage current, random telegraph noise) [1], [2], reliability [3]–[5] (e.g. time to breakdown, bias temperature instability), variability [6], [7], and scaling [8]. In this scenario, understanding the defects properties (i.e. the spatial density, atomic structure, and energy distribution in the band gap) affecting the material and device electrical response is crucial. Unfortunately, there are no established methods for extracting the defects properties in metal-insulator-metal (MIM) stacks in the Back-End-of-Line (BEoL), as techniques commonly used to characterize FET stacks (V_{TH} shift [9], gm degradation [10], and charge pumping [11]) cannot be directly applied to MIM stacks.

In this letter, we present a new method to extract the defect properties from the I-V curves hysteresis measured at low voltage/field in MIM stacks. This technique can be applied to characterize MIM stacks fabricated in BEoL for radio frequency (RF), storage, and dynamic random-access memory (DRAM) capacitors, embedded memories, and thin film transistors (TFT).



Fig. 1. Experimental results (symbols) and simulations (solid lines) of the transient I-V characteristics of (a) a TaN/10nm a-Al₂O₃/TaN MIM stack, and (b) a TaN/10nm HfO₂/TaN and a TaN/20nm HfO₂/TaN MIM stacks. The input voltages were double staircase voltage sweeps for both polarities. The arrows show the current evolution during the sweeps. The curves are plotted in a log-plot with sign, which allows highlighting the current hysteresis in the low-field region, characterized by the current amplitude I_H and the upper voltage limit V_H.

II. SAMPLES AND EXPERIMENTS

In this study, we consider TaN/high-k dielectric/TaN MIM stacks fabricated on n++-Si wafers (1-3.10-3 Ω ·cm) without native oxide, using amorphous alumina (a-Al₂O₃) and hafnia (HfO₂) as high-k material. First, 10nm Ta/20nm TaN bilaver was sputtered at room temperature and used as bottom electrode. Then, the dielectric film was deposited by atomic layer deposition at 300 °C in a Savannah reactor (Cambridge Nanotech) using trimethylaluminum and Bis(methyln5-cyclopentadienyl)methoxymethylhafnium as metal precursors for a-Al2O3 and HfO2 respectively, and water water as oxidizing agent [12], [13]. Finally, 20nm TaN/30nm W bilayer was deposited by sputtering and patterned by optical lithography and lift-off process to form the top electrode $(8 \cdot 10^{-1})^{-1}$ ⁴ cm² area), followed by a post-deposition thermal treatment in N₂ ambient for 20 min at 300 °C. The current-voltage characteristic was measured using an HP4140B pA meter / DC voltage source. The voltage stimuli were double-sweep stepwise voltage ramps with a 0.05 V voltage step. The measurement delay time was set to 2 s and the integration time was set to "Long", resulting in a 4.56 s maximum step length.

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Fig. 2. (a) Band diagram of a TaN/high-k dielectric/TaN MIM stack with two uniform defect distributions, accounting for the defects near the top and the bottom electrodes, characterized by a thermal ionization energy distribution with mean $E_{TH mean}$, spread $E_{TH spread}$, and aligned with the stack E_F , defect densities DD_{TOP} and DD_{BOT} , respectively, and thickness t_{TOP} and t_{BOT} , respectively; (b) charge trapping dynamics after a positive voltage step (V_{STEP} >0) with a positive voltage applied to the top electrode (V_{TOP} >0): charges are trapped/emitted to/from defects near the bottom/top, resulting in a positive transient current; (c) charge trapping dynamics after a negative voltage step (V_{STEP} <0) with a positive transient current; trapped/emitted to from defects near the bottom/top, resulting in a positive transient current; (c) charge trapping dynamics after a negative voltage step (V_{TOP} >0): charges are emitted/trapped from/to defects near the bottom/top, resulting in a negative transient current. These transient currents are independent of the stack voltage polarity, allowing for the emergence of the observed low-field current hysteresis. The arrows depitct the electron capture/emission processes.

III. EXTRACTION OF DEFECT PROPERTIES FROM LEAKAGE CURRENT MODELING

The leakage current in MIM stacks originates from electron tunneling [14], [15]. While for extremely thin stacks the charge transport is dominated by the direct tunneling, Trap-Assisted Tunneling (TAT) mechanism are relevant for thicker stacks. Indeed, defects support the charge transport and the multiphonon TAT model, accounting for lattice relaxation and electron-phonon coupling, was proposed to reproduce the I-V curves [16]. In thicker stacks defects can also trap electrons, changing the stack electrostatics and complicating the electrical data interpretation.

Transient I-V curves measured on TaN/10nm a-Al₂O₃/TaN, TaN/10nm HfO₂/TaN and TaN/20nm HfO₂/TaN stacks by applying double staircase voltage sweeps are shown in Fig. 1. The currents plotted in log-plots with sign allows highlighting the current hysteresis at low electric field, characterized by the current amplitude I_H and the upper voltage limit V_H. It is worth noting that such hysteretic behavior is often overlooked, as single voltage sweep measurements are typically considered.

The low-field current hysteresis is ascribed to charge trapping (emission) to (from) defects located near electrode interfaces [1], [17], [18]. This occurs when the defect thermal ionization energy (E_{TH}) is aligned with the stack Fermi level (E_F) as in Fig. 2a. Considering a positive double staircase voltage sweep applied to the top electrode ($V_{TOP}>0V$), during the rising part of the sweep (Fig. 2b, $V_{STEP}>0V$) defects with E_{TH} below (above) the cathode (anode) Fermi energy capture (emit) tunneling electrons, resulting in a positive transient current. In the falling part of the sweep (Fig. 2c, $V_{STEP}<0V$), the process is reversed: the electrons previously captured near the cathode are re-emitted as the defects energy exceed the cathode Fermi energy, and electrons are re-captured near the anode as the defects energy fall below the anode Fermi energy, resulting



Simulations of a TaN/10nm a-Al₂O₃/TaN MIM stack with Fia. 3. $DD_{TOP}=DD_{BOT}$, showing the effects of the defect distributions properties. (a) I-V curves at different E_{TH mean}-Φ_B (E_{TH spread}=2eV, DD_{TOT}=2·10¹⁸cm⁻ $^{3}eV^{-1}$); (b) Extracted I_H (at 1V) and V_H at different E_{TH mean}- Φ_{B} , showing the emergence of a significant low-field hysteresis for $E_{TH mean}$ - Φ_B =0eV and a weak dependence of the hysteresis limit; (c) I-V curves at different $E_{TH spread}$ ($E_{TH mean}$ - Φ_B =0eV, DD_{TOT} =2·10¹⁸cm⁻³eV⁻¹); (d) Extracted I_H (at 1V) and V_H at different $E_{TH spread}$, showing a strong dependence of the hysteresis limit on E_{TH spread}. (e) I-V curves at different DD_{TOT} (E_{TH mean}- $\Phi_B=0eV$, $E_{TH spread}=2eV$); (f) Extracted I_H (at 1V) and V_H at different DD_{TOT}, showing a larger hysteresis amplitude in correspondence of a higher DD_{TOT}. At high DD_{TOT} (e.g. DD_{TOT}= $2 \cdot 10^{19}$ cm 3 eV $^{-1}$), the hysteresis is limited by the onset of a steady-state conduction, facilitated by the defects. The materials parameters used in the simulations are summarized in Table I.

in a net negative transient current. The same holds true for a negative voltage sweep, generating either a positive or negative transient current for V_{STEP} >0V and V_{STEP} <0V, respectively. Thus, the current hysteretic behavior shown in Fig. 1 originates from the transient charge trapping/emission currents at the MIM interfaces. In the high-field current (i.e. above V_H), no hysteresis is observed due to the higher electron tunneling probability through the whole stack, which makes the steady state current (traversing the MIM stack) dominating over the transient charge trapping/emission current (at the MIM interfaces). Interestingly, the high-field currents shown in Fig. 1 are asymmetric in both the a-Al₂O₃ and the HfO₂ stacks.

The low-field current hysteresis has been investigated with the support of GINESTRA[®] simulation software [19]–[24], which self-consistently accounts for the electrostatics, the charge trapping/emission dynamics to/from defects in the dielectric, the charge transport through the stack by the different conduction mechanisms relevant in dielectrics (i.e. direct

TABLE I	
MATERIALS PARAMETER	25

Electrodes		TaN		
WF	Work Function (eV)	4.55		
High-k oxides		a-Al ₂ O ₃	HfO ₂	
BG	Band gap (eV)	6.4	5.8	
χ	Electron affinity (eV)	2	2.5	
m _T	Electron tunneling	0.5 m ₀	$0.25 m_0$	
	effective mass			
k	Permittivity	9	14	
E _{PH}	Phonon energy (eV)	0.05	0.07	
E _{TH mean}	Thermal ionization	2.55	1.8	
	energy mean (eV)			
E _{TH spread}	Thermal ionization	2	1.5	
	energy spread (eV)			
E _{REL}	Relaxation energy (eV)	0.5	1.19	
DD _{TOP}	Top distribution	$4.5 \cdot 10^{18}$	$0.15 \cdot 10^{18}$	
	defect density (cm ⁻³ eV ⁻¹)			
DDBOT	Bottom distribution	$0.5 \cdot 10^{18}$	$4 \cdot 10^{18}$	
	defect density (cm ⁻³ eV ⁻¹)			
t _{TOP}	Top distribution	5	6 (10 nm stack)	
	thickness (nm)		4 (20 nm stack)	
t _{BOT}	Bottom distribution	5	4 (10 nm stack)	
	thickness (nm)		16 (20 nm stack)	

tunneling, conduction/valence band carrier drift, and multiphonon TAT), along with the respective temperature effects. The low-field current hysteresis is reproduced considering two defect distributions, DD_{TOP} with thickness t_{TOP} and DD_{BOT} with thickness t_{BOT} , accounting for the defects near the top and the bottom electrodes, respectively (Fig. 2a). The effects of the defect distributions parameters (i.e. $E_{TH mean}$, $E_{TH spread}$, DD_{TOP} , and DD_{BOT}) are shown in Fig.3 considering, for simplicity, a TaN/10nm a-Al₂O₃/TaN stack with a uniform defect distribution (i.e. DD_{TOP} =DD_{BOT}) at positive voltages (the same applies for negative voltages). The following discussion applies to any dielectric, such as the HfO₂ (not included for brevity).

As illustrated in Fig. 3a-b, the $E_{TH}-E_F$ alignment strongly affects the current hysteresis magnitude, providing results similar to the measurements of Fig. 1 when E_{TH} mean= Φ_B . Interestingly, the hysteresis upper voltage limit increases with $E_{TH}-E_F$. Both I_H and V_H correlate to $E_{TH}-E_F$, thus providing information on the defects energy alignment.

Simulations shows that the current hysteresis depends on the defect energy distribution spread $E_{TH spread}$. As shown in Fig. 3cd, a single defect energy E_{TH} level cannot account for the wide current hysteresis shown in Fig. 1. V_{H} increases with $E_{TH spread}$ up to 2eV, saturating for higher defect energy spread, so that it can be used to identify $E_{TH spread}$. I_H is not sensitive to $E_{TH spread}$.

The hysteresis current amplitude depends linearly on $DD_{TOT}=DD_{TOP}+DD_{BOT}$, Figs. 3e-f. It is worth noting that this holds true for either a uniform or a non-uniform distribution (i.e. $DD_{TOP}\neq DD_{BOT}$). Increasing either DD_{TOP} or DD_{BOT} offers more trapping/emission sites at each voltage step, thus increasing I_H irrespectively of the specific defect distribution. Conversely, the high-field steady-state current, if mediated by the defects (e.g. TAT), is expected to be affected by the defect distribution non-uniformity, leading to an asymmetric IV characteristics. Consistently, a higher DD_{TOT} reduces the V_H due to the earlier onset of a steady-state charge transport (e.g. TAT), also mediated by the defects.

Simulations at different dielectric permittivity and at different dielectric thickness (not included for brevity), shown no effect on $I_{\rm H}$. The dielectric permittivity shown also no effect

on $V_{\rm H}$. Finally, the dielectric thickness trivially affects $V_{\rm H}$ due to the related electric field scaling, which can be easily taken into account when extracting the dielectric defects properties.

In summary, I_H and V_H are strongly correlated to the defects properties, while being mostly independent from the dielectric macroscopic properties, enabling the defects profiling.

IV. PROFILING DEFECT PROPERTIES IN HIGH-K DIELECTRICS

The I-V curves shown in Fig. 1 have been analyzed by exploiting (I_H and V_H)-($E_{TH mean}$, $E_{TH spread}$, DD_{TOT}) correlation to extract a-Al₂O₃ and HfO₂ defects properties as described in the previous sections. The information provided by the low-field hysteresis is then cross-correlated with the information provided by the high-field steady-state current, allowing fitting the parameters DD_{BOT}, DD_{TOP}, t_{TOP}, and t_{BOT}. The accuracy of the extracted defect properties was verified using GINESTRA[®].

First, in agreement with Figs. 3(b,d), the almost constant hysteresis amplitude I_H shown at low-field in Fig. 1 suggests the presence of defects distributed near the electrodes, with ETH mean aligned with the device E_F, and with a significant energy spread E_{TH spread} that can be estimated exploiting its relationship with V_H (Fig. 3d). Low-field hysteresis simulations allowed estimating an E_{TH spread} in the 1.5-3 eV range and in the 1-3 eV range for the a-Al₂O₃ and HfO₂ stacks, respectively. Finally, the linear relationship between I_H and DD_{TOT} (Fig 3e-f) allowed estimating a DD_{TOT} of $5 \cdot 10^{18}$ cm⁻³eV⁻¹ and $4.15 \cdot 10^{18}$ cm⁻³eV⁻¹ for the a-Al₂O₃ and HfO₂ stacks, respectively. A non-uniform defect distribution is then considered to account for the highfield I-V curves asymmetry. The values of ETH mean, ETH spread, identified through the above reasoning were then refined using full I-V curve simulations, while fitting DD_{BOT}, DD_{TOP}, t_{TOP}, and t_{BOT} under the constraint provided by the extracted DD_{TOT}. The extracted parameters are summarized in Table I.

The simulations of the MIM stack (Fig. 1), performed considering the extracted defects parameters, well compare with the reported experimental results. The extracted defects parameters of a-Al₂O₃ are in good agreement with ab-initio calculation [25], and compatible with oxygen vacancies and aluminum interstitials. Both defect typologies are also compatible with experimental results of exhaustive photo-depopulation spectroscopy (EPDS) of a-Al₂O₃ [26] and simulations of charge-trap memory devices [27]. The defect parameters extracted from the HfO₂ stacks are compatible with oxygen vacancies, as good agreement is found with values previously reported from both ab-initio calculations [28], [29] and leakage currents fitting [24], [16], [30]. This confirms the effectiveness of the presented extraction technique, based on the information provided by the low-field I-V curve hysteresis.

V. CONCLUSIONS

We presented a methodology for extracting the properties of defects in MIM stacks. The proposed method, exploiting the information provided by the low-field I-V curve hysteresis, allows for an accurate and consistent identification of the defects properties. We applied the presented methodology to a-Al₂O₃-based and HfO₂-based MIM stacks, profiling their defects and finding good agreement with ab-initio simulations and different experimental results.

REFERENCES

- Z. Xu *et al.*, "A Study of Relaxation Current in High-k Dielectric Stacks," *IEEE Trans. Electron Devices*, vol. 51, no. 3, pp. 402–408, Mar. 2004, doi: 10.1109/TED.2003.822343.
- [2] F. M. Puglisi, L. Larcher, A. Padovani, and P. Pavan, "A Complete Statistical Investigation of RTN in HfO₂-Based RRAM in High Resistive State," *IEEE Trans. Electron Devices*, vol. 62, no. 8, pp. 2606–2613, Aug. 2015, doi: 10.1109/TED.2015.2439812.
- [3] G. Bersuker *et al.*, "Effect of Pre-Existing Defects on Reliability Assessment of High-K Gate Dielectrics," *Microelectron. Reliab.*, vol. 44, no. 9–11, pp. 1509–1512, Sep. 2004, doi: 10.1016/j.microrel.2004.07.048.
- [4] G. Ribes et al., "Review on high-k dielectrics reliability issues," *IEEE Trans. Device Mater. Reliab.*, vol. 5, no. 1, pp. 5–19, Mar. 2005, doi: 10.1109/TDMR.2005.845236.
- [5] A. Padovani, D. Z. Gao, A. L. Shluger, and L. Larcher, "A microscopic mechanism of dielectric breakdown in SiO2 films: An insight from multi-scale modeling," *J. Appl. Phys.*, vol. 121, no. 15, 2017, doi: 10.1063/1.4979915.
- [6] A. Veloso *et al.*, "Integration Challenges and Options of Replacement High-/Metal Gate Technology for (Sub-)22nm Technology Nodes," *ECS Trans.*, vol. 52, no. 1, pp. 385–390, Mar. 2013, doi: 10.1149/05201.0385ecst.
- [7] C. Couso, M. Porti, J. Martin-Martinez, A. J. Garcia-Loureiro, N. Seoane, and M. Nafria, "Local Defect Density in Polycrystalline High-k Dielectrics: CAFM-Based Evaluation Methodology and Impact on MOSFET Variability," *IEEE Electron Device Lett.*, vol. 38, no. 5, pp. 637–640, May 2017, doi: 10.1109/LED.2017.2680545.
- [8] J. Robertson and R. M. Wallace, "High-K materials and metal gates for CMOS applications," *Mater. Sci. Eng. R Reports*, vol. 88, pp. 1– 41, Feb. 2015, doi: 10.1016/j.mser.2014.11.001.
- [9] G. P. Lansbergen et al., "Threshold voltage drift (PBTI) in GaN D-MODE MISHEMTs: Characterization of fast trapping components," in 2014 IEEE International Reliability Physics Symposium, Jun. 2014, pp. 6C.4.1-6C.4.6, doi: 10.1109/IRPS.2014.6861111.
- [10] S. Johansson, J. Mo, and E. Lind, "Characterization of border traps in III-V MOSFETs using an RF transconductance method," *Eur. Solid-State Device Res. Conf.*, vol. 60, no. 2, pp. 53–56, 2013, doi: 10.1109/ESSDERC.2013.6818817.
- [11] R. E. Paulsen and M. H. White, "Theory and application of charge pumping for the characterization of Si-SiO2 interface and nearinterface oxide traps," *IEEE Trans. Electron Devices*, vol. 41, no. 7, pp. 1213–1216, Jul. 1994, doi: 10.1109/16.293349.
- [12] E. Cianci, A. Molle, A. Lamperti, C. Wiemer, S. Spiga, and M. Fanciulli, "Phase Stabilization of Al:HfO 2 Grown on In x Ga 1– x As Substrates (x = 0, 0.15, 0.53) via Trimethylaluminum-Based Atomic Layer Deposition," ACS Appl. Mater. Interfaces, vol. 6, no. 5, pp. 3455–3461, Mar. 2014, doi: 10.1021/am405617q.
- [13] S. Spiga, F. Driussi, G. Congedo, C. Wiemer, A. Lamperti, and E. Cianci, "Sub-1 nm Equivalent Oxide Thickness Al-HfO 2 Trapping Layer with Excellent Thermal Stability and Retention for Nonvolatile Memory," ACS Appl. Nano Mater., vol. 1, no. 9, pp. 4633–4641, Sep. 2018, doi: 10.1021/acsanm.8b00918.
- [14] F. Chiu, "A Review on Conduction Mechanisms in Dielectric Films," Adv. Mater. Sci. Eng., vol. 2014, pp. 1–18, 2014, doi: 10.1155/2014/578168.
- [15] A. Paskaleva, D. Spassov, and D. Dankovic, "Consideration of conduction mechanisms in high-k dielectric stacks as a tool to study electrically active defects," *Facta Univ. - Ser. Electron. Energ.*, vol. 30, no. 4, pp. 511–548, 2017, doi: 10.2298/fuee1704511p.
- [16] L. Vandelli, A. Padovani, L. Larcher, R. G. Southwick, W. B. Knowlton, and G. Bersuker, "A Physical Model of the Temperature Dependence of the Current Through SiO2/HfO2 Stacks," *IEEE Trans. Electron Devices*, vol. 58, no. 9, pp. 2878–2887, Sep. 2011, doi: 10.1109/TED.2011.2158825.
- [17] R. Moazzami, C. Hu, Reza Moazzami, and Chenming Hu, "Stressinduced current in thin silicon dioxide films," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, vol. 1992-Decem, no. c, pp. 139– 142, 1992, doi: 10.1109/IEDM.1992.307327.
- [18] D. Bisi et al., "On trapping mechanisms at oxide-traps in Al2O3/GaN metal-oxide-semiconductor capacitors," *Appl. Phys. Lett.*, vol. 108, no. 11, 2016, doi: 10.1063/1.4944466.
- [19] "Applied Materials GinestraTM," [Online]. Available:

http://www.appliedmaterials.com/products/applied-mdlx-ginestrasimulation-software.

- [20] L. Larcher, A. Padovani, F. M. Puglisi, and P. Pavan, "Extracting Atomic Defect Properties From Leakage Current Temperature Dependence," *IEEE Trans. Electron Devices*, vol. 65, no. 12, pp. 5475–5480, 2018, doi: 10.1109/TED.2018.2874513.
- [21] A. Padovani *et al.*, "A Sensitivity Map-Based Approach to Profile Defects in MIM Capacitors From I-V, C–V, and G–V Measurements," *IEEE Trans. Electron Devices*, vol. 66, no. 4, pp. 1892–1898, Apr. 2019, doi: 10.1109/TED.2019.2900030.
- [22] A. Padovani, J. Woo, H. Hwang, and L. Larcher, "Understanding and Optimization of Pulsed SET Operation in HfO x -Based RRAM Devices for Neuromorphic Computing Applications," *IEEE Electron Device Lett.*, vol. 39, no. 5, pp. 672–675, May 2018, doi: 10.1109/LED.2018.2821707.
- [23] B. Dianat, A. Padovani, and L. Larcher, "Multiscale modeling of CeO2/La2O3 stacks for material/defect characterization," in 2020 IEEE 33rd International Conference on Microelectronic Test Structures (ICMTS), May 2020, pp. 1–3, doi: 10.1109/ICMTS48187.2020.9107922.
- [24] P. La Torraca, F. M. Puglisi, A. Padovani, and L. Larcher, "Multiscale Modeling for Application-Oriented Optimization of Resistive Random-Access Memory," *Materials (Basel).*, vol. 12, no. 21, p. 3461, Oct. 2019, doi: 10.3390/ma12213461.
- [25] O. A. Dicks, J. Cottom, A. L. Shluger, and V. V. Afanas'Ev, "The origin of negative charging in amorphous Al 2 O 3 films: The role of native defects," *Nanotechnology*, vol. 30, no. 20, 2019, doi: 10.1088/1361-6528/ab0450.
- [26] V. V. Afanas'ev, W. C. Wang, F. Cerbu, O. Madia, M. Houssa, and A. Stesmans, "Spectroscopy of Deep Gap States in High-k Insulators," *ECS Trans.*, vol. 64, no. 8, pp. 17–22, Aug. 2014, doi: 10.1149/06408.0017ecst.
- [27] A. Padovani, L. Larcher, V. Della Marca, P. Pavan, H. Park, and G. Bersuker, "Charge trapping in alumina and its impact on the operation of metal-alumina-nitride-oxide-silicon memories: Experiments and simulations," *J. Appl. Phys.*, vol. 110, no. 1, p. 014505, Jul. 2011, doi: 10.1063/1.3602999.
- [28] K. Xiong, J. Robertson, M. C. Gibson, and S. J. Clark, "Defect energy levels in HfO2 high-dielectric-constant gate oxide," *Appl. Phys. Lett.*, vol. 87, no. 18, p. 183505, Oct. 2005, doi: 10.1063/1.2119425.
- [29] P. Broqvist, A. Alkauskas, J. Godet, and A. Pasquarello, "First principles investigation of defect energy levels at semiconductoroxide interfaces: Oxygen vacancies and hydrogen interstitials in the Si–SiO2–HfO2 stack," J. Appl. Phys., vol. 105, no. 6, p. 061603, Mar. 2009, doi: 10.1063/1.3055347.
- [30] S. Cimino *et al.*, "A study of the leakage current in TiN/HfO2/TiN capacitors," *Microelectron. Eng.*, vol. 95, pp. 71–73, Jul. 2012, doi: 10.1016/j.mee.2011.03.009.