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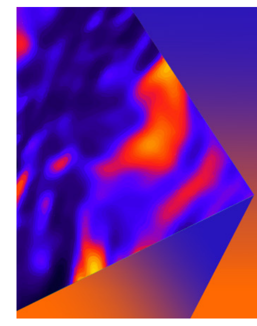

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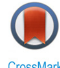
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ABSTRACT

Recently, the possibility to tune the critical current of conventional metallic superconductors via electrostatic gating was shown in wires, Josephson weak-links, and superconductor-normal metal–superconductor junctions. Here, we exploit such a technique to demonstrate a gate-controlled vanadium-based Dayem nano-bridge operated as a *half-wave* rectifier at 3 K. Our devices exploit the gate-driven modulation of the critical current of the Josephson junction and the resulting steep variation of its normal-state resistance, to convert an AC signal applied to the gate electrode into a DC one across the junction. All-metallic superconducting gated rectifiers could provide the enabling technology to realize tunable photon detectors and diodes useful for superconducting electronics circuitry.

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In the last few years, the possibility to suppress the critical current in conventional Bardeen–Cooper–Schrieffer (BCS) superconducting wires,[1] Dayem bridge (DB) Josephson junctions (JJs),[2–5] and superconductor-normal metal–superconductor weak-links[6] via electrostatic gating was demonstrated.[7] Such a technique is at the basis of a class of innovative all-metallic superconducting Josephson transistors, where a gate electrode is used to modulate down to full suppression the critical current of a superconducting channel, in analogy to what occurs for the current in standard gated semiconductor transistors. Furthermore, the impact of the electrostatic gating on the macroscopic phase and on the phase slip dynamics was proved in superconducting quantum interference devices (SQUIDs)[8] and in gated titanium DBs, respectively.[9] So far, the microscopic origin of the gating effect in metallic superconductors is unclear, and the debate in the search of a satisfactory explanation for the aforementioned phenomenology has just started.[4,10,11] Electrostatic-field-driven surface-orbital polarization was proposed as the knob to control both the amplitude and the phase of gated superconductors.[4,11] Furthermore, it was conjectured about the role of a tiny field-emission gate-superconductor current.[12,13] Yet, several technological implementations based on gated superconducting transistors for both classical and quantum computation architectures were proposed[7] until now and promise new paradigms to realize innovative superconducting circuits. These are expected to benefit from operation frequencies close to those typical of rapid single flux quantum devices (up to ∼750 GHz),[14] but in a *voltage-driven* fashion, which would provide a direct and convenient interface with complementary metal-oxide technology (CMOS).

Here, we demonstrate a vanadium (V) Josephson half-wave rectifier based on a scheme recently proposed,[5] which exploits the strong non-linearity of the resistance (R) of a gated superconducting nanotransistor vs gate voltage (V_G). Such a device might form the rectifying core of a photon sensor operating at high frequencies, relevant, for instance, for cosmological applications[15] or could be exploited as a comparator[16] to be used in all-superconducting digital electronic circuits.[7] The potentially high operation frequency, the ease of fabrication, and the simple geometry of our nanodevices make them attractive as effective alternatives to conventional all-semiconductor[17] and semiconductor–superconductor hybrid[18–23] field-effect-transistor-based technologies.[24–28] Below, we focus on the manipulation of the dissipative response of the V-based Josephson weak-link via the application of a voltage to a gate capacitively coupled to the junction and show its time-resolved response to periodic square-wave and sinusoidal signals applied to the gate, thereby leading to electric rectification.

Our device consists of a planar 60-nm-tick, 160-nm-long, 90-nm-wide V Dayem bridge JJ with a 70-nm-apart, 120-nm-wide side-gate aligned to the constriction. The device fabrication was

performed on a silicon oxide substrate by single-step electron beam lithography followed by vanadium deposition performed at a rate of 0.36 nm/s in an ultra-high vacuum electron-beam evaporator with a base pressure of $\sim 10^{-11}$ Torr.[29–35] Figure 1(a) shows the false color scanning electron micrograph of a representative V JJ transistor along with the 4-wire biasing scheme used for the low-temperature current vs voltage (I–V) characterization of the devices performed in a filtered cryogen-free ^{3}He–^{4}He dilution refrigerator.

For temperatures below ∼3.5 K, the V JJ is superconducting and exhibits, at 2 K, a critical current I_C of ∼1.42 mA, a retrapping current $I_R \sim 380\,\mu$A, and a normal-state resistance R_N of around ∼110 Ω. The forward and backward current I vs V characteristics for temperatures T ranging from 2.0 K to 3.8 K are shown in Fig. 1(b), where the full evolution of I_C as a function of T is highlighted by the gray area. The hysteretic behavior of the curves stems from quasiparticle overheating when the junction switches from the superconducting to the normal state.[36,37] Moreover, the additional features present on the I–V characteristics at higher current are likely to be related to the switching of the DB banks to the normal state. The decay of both I_C and I_R with the temperature is shown in Fig. 1(c), where the black dashed line represents a fit of the I_C vs T characteristic performed with Bardeen's equation: $I_C(T) = I_C^0[1-(\frac{T}{T_C})^2]^{\frac{3}{2}}$, where I_C^0 is the zero-temperature critical current and T_C is the DB critical temperature. The fitting procedure yielded $I_C^0 = (2.2 \pm 0.1)$ mA and $T_C^{fit} = (3.62 \pm 0.07)$ K. The latter value is in agreement with the experimental critical temperature determined from the 4-wire lock-in measurement of the junction resistance vs bath temperature T, as shown in the inset of Fig. 1(b).

The preliminary characterization of the gating effect on I_C and R was carried out by acquiring the forward and backward I–V characteristics of a representative vanadium DB as a function of the voltage applied to the gate electrode, V_G. Figure 2(a) displays the $I_C(V_G)$ characteristics extracted from I–V acquired at several bath temperatures. The suppression of I_C occurs for both positive and negative values of V_G ($V_G \rightarrow -V_G$), and the gating effect persists up to ∼3.3 K, i. e., $\sim 0.9T_C$. We note that the sharper suppression of I_C observed for positive values of V_G seems to be in contrast to a possible contribution to the critical current suppression driven by cold field-emission of electrons. Indeed, electron extraction from the gate (occurring at negative gate bias values) is expected to be more effective than that from the DB (occurring at positive gate bias values) owing to the substantial asymmetry of the device geometry.[13]

Let us now describe further the transport properties of the transistor by focusing on the behavior of the device resistance R under the action of the electric field. The steep modulation of the critical current yields, at constant current bias I_B, an analogous modulation of the resistance of the device. Figure 2(b) displays the evolution of R as a function of gate voltage V_G for several values of bias current I_B, which was always set below the retrapping current so that no hysteretic

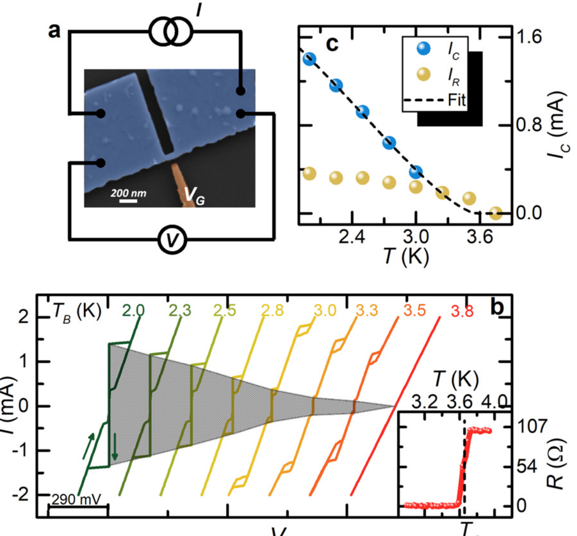

FIG. 1. (a) False-color scanning electron micrograph of a typical gate-controlled vanadium JJ nanotransistor. The DB constriction (light blue) is current biased, and the voltage drop is measured in a 4-wire configuration. The electrostatic field is applied via the gate electrode (orange). (b) Back and forth current I vs voltage V characteristics of a representative device measured at different bath temperatures from 2.0 K to 3.8 K. The curves are horizontally offset for clarity. The inset shows the 4-wire lock-in measurement (with biasing current $I \simeq 15$ nA) of the R vs T characteristic of the junction. The superconducting transition occurs at $T_C \simeq 3.6$ K. (c) Evolution of the critical current I_C (light blue dots) and retrapping current I_R (yellow dots) vs bath temperature T. The black dashed line represents the best fit of $I_C(T)$ with Bardeen's theory, which yields $I_C^0 = (2.2 \pm 0.1)$ mA and $T_C^{fit} = (3.62 \pm 0.07)$ K as fitting parameters.

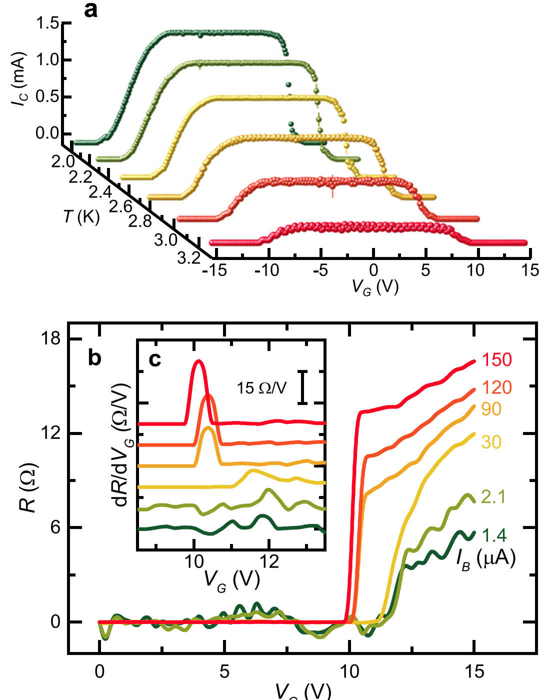

FIG. 2. (a) I_C vs V_G characteristics for different temperatures ranging from 2.0 to 3.3 K. Data were computed averaging 25 acquisitions of the switching current. The error bars represent the standard deviation of the ensemble of measurements. (b) Resistance $R = V/I_B$ vs gate voltage V_G for different values of bias current I_B from 1.4 to 150 μA. (c) Transresistance $\frac{dR}{dV_G}$ vs gate voltage V_G for the same bias currents of panel (b). Measurements of panels (b) and (c) were carried out at $T_B = 3.0$ K.

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behavior was expected from the device. We note that R remains almost equal to 0 for V_G values such that $I_C(V_G) > I_B$. Then, for higher gate voltage, the resistance jumps to finite values due to the gate-driven superconducting-to-normal state transition of the device. Finally, R increases with V_G, probably owing to the enlargement of the normal-state region within the junction.[2] In particular, for $I_B > 30\ \mu$A, R exhibits a linear dependence on V_G. Moreover, the steepness of the resistance jump also depends on I_B, as customarily described by the figure of merit of the resistance derivative with respect to the gate voltage (dR/dV_G), which is shown in Fig. 2(c). The amplitude of the differential resistance peaks, corresponding to the transition to the normal state, increases with I_B reaching the maximum value of $\sim 30\Omega/$ V at $I_B = 150\ \mu$A. Furthermore, the peak center shifts toward lower V_G values as the bias current is increased.

The strong non-linearity typical of the $R(V_G)$ characteristics, provided by the transition to the dissipative regime, could be conveniently exploited to implement a superconducting *half-wave* rectifier converting an AC signal applied to the gate into a DC one across the DB. Such a mechanism has been recently proposed for Nb gate-controlled transistors,[5] where the rectification properties of a DB device have been analyzed by a standard lock-in technique, which does not provide information neither on the time-resolved behavior of the devices nor on the shape of the output signal. These features could allow us to realize, for instance, a radiation detector in which the AC electric field collected by an antenna coupled to the gate electrode would be rectified, thereby leading to an amplified non-zero average signal. The gain of such a device can be defined as the ratio $g = V_{out}/V_{in}$, where V_{in} and V_{out} are the peak-to-peak amplitudes of the signal applied to the gate and the voltage drop across the DB, respectively. The quantity g can be calculated through the relation $g = R(V_G)I_B\tau/\sigma$, where $R(V_G)I_B = V_{out}$ is the product of the gate-dependent DB resistance R and the current bias I_B, while $\sigma/\tau = V_{in}$ is given by the ratio of the typical width (σ) of the switching current probability distribution for gate-driven superconducting field-effect transistors[9] and the transconductance $\tau = dI_C/dV_G$.[7] For V-based devices, g is expected to reach values as high as ~ 7 with a typical power dissipation of ~ 40 nW. Our V DB nanotransistor shows gain performance similar to cryogenic semiconductor devices[38,39] with a reduction in power consumption of about *three* orders of magnitude. Noteworthily, a series of N rectifiers can be realized by feeding the gate electrode of the nth rectifier with the output voltage of the $(n-1)$th one, resulting in a total gain equal to g^N.

In the following, we shall focus on the time-resolved investigation of the response of V Josephson transistors to AC square-wave and sinusoidal gate signals. The measurement setup, comprising an input/output analog-to-digital/digital-to-analog converter (ADC/DAC) board for the generation and the acquisition of time-resolved alternate current and voltage signals, is depicted in Fig. 3(a). The voltage drop $V(t)$ across the current-biased DB was measured as a function of a time-dependent gate voltage $V_G(t)$. In this configuration, when $I_C[V_G(t)] < I_B$, the junction is in the *normal* state and a finite voltage drop is built across the DB (*high-state*). By contrast, when $I_C(V_G(t)) > I_B$, the DB is *superconducting* and $V \sim 0$ (*low-state*). The response of the device to a transistor–transistor-logic (TTL)-like square-wave excitation was probed by feeding the gate with a signal consisting of a $V_{DC} = 10$ V DC bias added to a $V_{AC} = 5$ V square-wave signal with frequencies up to ~ 50 Hz, as shown in Fig. 3(c). The voltage drop in the *high* and *low states* for some representative values of I_B is shown in Fig. 3(d) as pairs of points of the same color superimposed on the I–V characteristics. Such curves are taken at selected values of V_G. As displayed in Fig. 3(d), the voltage drop across the junction preserves the shape of the input signal. In this regard, we emphasize that in our experiments, the maximum operation frequency is limited by the low-pass filtering stages of the electrical lines of our setup. A lower bound to the operation frequency of the V gate-controllable rectifiers might arise in the $10^8 - 10^{10}$ Hz range due to the typical electron–phonon relaxation rates at these bath temperatures.[40] Furthermore, the frequency defined by $2\Delta/h \sim 265$ GHz, where Δ is the superconducting gap energy and h Planck's constant, is likely to provide the ultimate operation limit.[41] The latter value is

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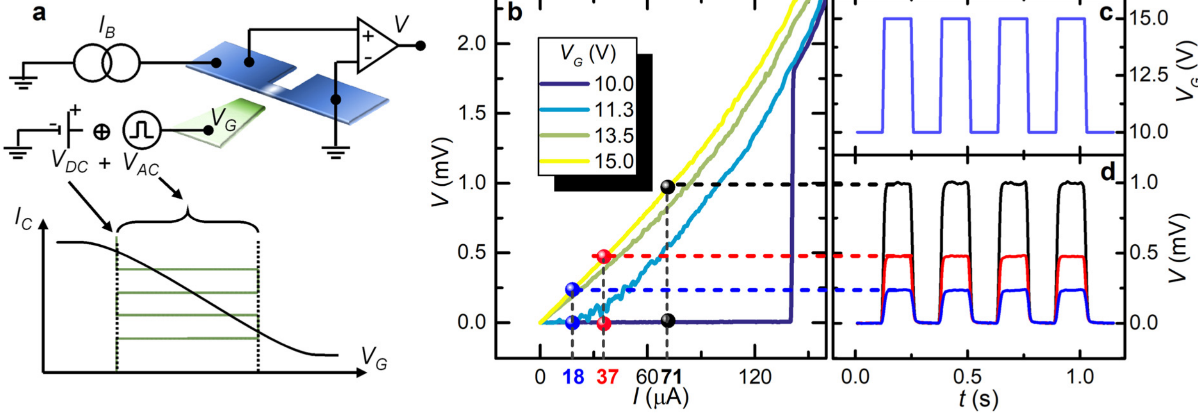

FIG. 3. (a) Scheme of time-resolved measurements of the 4-wire voltage drop $V(t)$ across the junction at constant current bias I_B vs DC (black dotted line) + AC (square-wave green line) gate voltage. The gate polarization signal is compared with the I_C vs V_G curve to highlight the dynamic working range of the system. (b) Voltage V vs current I characteristics for selected values of gate voltage V_G. The dot pairs show the working points of the system for different values of the bias current $I_B = 18$, 37, 71 μA. (c) Evolution of the gate voltage vs time. The signal was obtained by summing a DC voltage $V_{DC} = 10$ V and an AC square-wave voltage with amplitude $V_{AC} = 5$ V. (d) Time-resolved voltage drop across the DB for selected values of the current bias. Dashed lines show the corresponding working points in panel (b). These measurements were performed at $T_B = 3$ K.

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comparable to state-of-the-art hybrid and CMOS field-effect transistors;[17,42,43] nonetheless, we stress that at the present time, the timescale of gate-driven superconducting phase transition is still totally unknown and is worth to be investigated through specifically designed experiments.

The response of the DB to a sinusoidal gate voltage excitation was measured by applying to the gate an AC sine signal V_{AC} with peak-to-peak amplitudes ranging from 1 to 3.5 V added to a V_{DC} = 11 V DC voltage bias. This results in a periodic sinusoidal oscillation of the critical current I_C above and below I_B, producing a gate-driven periodic modulation of the device resistance. The voltage drop across the DB as a function of I_B and V_G is displayed in Fig. 4(a). We note that by choosing I_B and V_{DC}, it is possible to set a working point for the rectifier, which determines the intensity and the shape of the resulting output voltage signal through the evolution of the super-to-normal switching point [red dashed line in Fig. 4(a)] and through the dependence of the device resistance on the gate voltage (also see Ref. 2). Indeed, the system lies in the zero voltage state for $I_C(V_G(t)) > I_B$, and a voltage drop across the junction occurs when $I_C(V_G(t)) \simeq I_B$. For higher values of V_G, i.e., when $I_C(V_G(t)) < I_B$, the voltage drop increases due to the gate-driven evolution of the DB resistance, which eventually will saturate at the asymptotic value of the normal-state resistance. Figure 4(c) shows the voltage drop of the DB as a function of time, in response to the gate signal reported in Fig. 4(b). To clarify the response of the system to such excitation, we highlight in Figs. 4(a) and 4(b) three points corresponding to the minimum of the $V_G(t)$ signal (light green dot), the switching point (red dot), and the maximum of $V_G(t)$ (dark green dot). The value of the biasing current was set to $I_B = 72\mu$A in order to take advantage of both the sharp normal-to-superconductor transition and the linear relation between R and V_G for $I_B > I_C$. The latter feature allows us to preserve the sinusoidal shape in the output voltage when the JJ is in the resistive state, as shown in Figs. 4(c)–4(e) for different values of V_{AC}. Indeed, although the output signal resembles that of a conventional half-wave rectifier,[43] it is worth emphasizing that, in our systems, it is possible to tune the rectification threshold V_G^* by changing both I_B and V_{DC}.

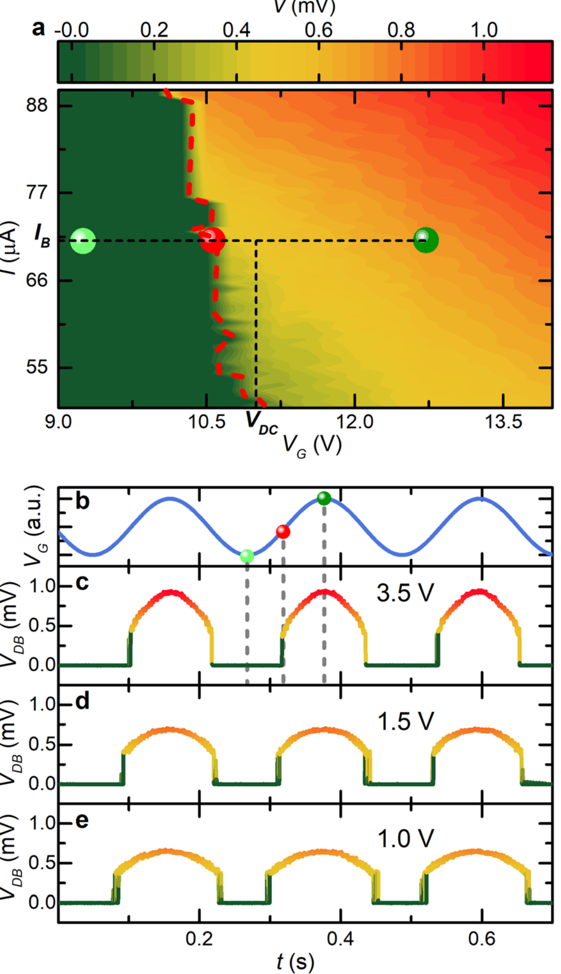

FIG. 4. (a). Density plot of the voltage drop across the junction as a function of the gate voltage (x axis) and current bias (y axis). From left to right, the three points represent the minimum zero resistance gate voltage value (light green), the transition between the superconducting and the normal state (red), and the maximum of both gate voltage and voltage drop (dark green). The dashed red curve highlights the critical current I_C as a function of the gate voltage V_G. (b) Time evolution of the gate voltage. The signal was obtained adding a DC voltage V_{DC} = 11 V and an AC sine wave voltage V_{AC}. The three dots highlight the working points described in panel (a). [(c)–(e)] Time-resolved voltage drop across the DB for V_{AC} = 3.5, 1.5, 1.0 V, respectively. The colormap is the same as panel (a). All these measurements were carried out at T_B = 3 K.

In summary, we have demonstrated a half-wave rectifier based on a gated vanadium Dayem nano-bridge Josephson transistor operating at 3 K. We showed the time-resolved response of our device to square-wave and sinusoidal gate signals, demonstrating the ability to convert an AC excitation into a DC one, and with a gain, which is expected to obtain a value close to 7 at a power consumption of ~40 nW. The performance of the V DB represents a major improvement in energy efficiency compared to conventional cryogenic semiconductor technology.[38,39] V-based gate-controllable Josephson rectifiers could represent a breakthrough and a possible enabling technology to implement innovative all-metallic superconducting photon detectors[44–46] based on gating as well as electric diodes suitable for superconducting digital[41] and quantum electronics[47,48] circuitry.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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