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Towards vertical Schottky diodes on bulk cubic silicon carbide (3C-SiC)

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Abstract

In this paper, we demonstrate the feasibility of fabricating vertical Schottky diodes on bulk cubic silicon carbide (3C-SiC) material obtained by combining sublimation epitaxy and chemical vapor deposition, starting from 4°-off axis 4H-SiC. First, the good quality of the epilayers grown with this method was demonstrated by morphological and structural analyses. Then, fabricated vertical Pt/3C-SiC Schottky diodes exhibited an ideality factor of 1.21 and a barrier height of 0.6eV, as determined by thermionic emission model. The temperature dependent forward current analysis indicated the formation of an inhomogeneous barrier, which has been related with the presence of conductive surface defects, detected by nanoscale local current measurements. On the other hand, the reverse leakage current could be described by thermionic field emission model including image force lowering. These findings demonstrate the viability of the proposed approach for bulk 3C-SiC growth for device fabrication. The material quality and the feasibility of fabricating vertical diodes based on 3C-SiC with a low barrier pave the way for the application of this polytype for medium-voltage power devices.

Keywords: 3C-SiC, Pt Schottky contacts, I-V, C-AFM

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1. Introduction

Silicon carbide (SiC) possesses excellent physical and electronic properties, which make this semiconductor the optimal choice for power electronic devices [1]. It can be found in nature in a large variety of polytypes [2]. Among them, the hexagonal 4H-SiC material is today available in large diameter wafers of good crystalline quality [3] and is the only polytype used for the fabrication of commercial devices, e.g., Junction Barrier Schottky (JBS) diodes and Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) [4,5].

On the other hand, the cubic polytype (3C-SiC) has been often indicated as a promising alternative for MOSFET technology, due to a lower density of traps at the SiO_2/3C-SiC interface with respect to SiO_2/4H-SiC system [6,7]. This peculiarity can result in high channel mobility values in 3C-SiC MOSFETs [8,9,10]. However, the crystal quality of 3C-SiC strongly depends on the rather demanding growth conditions, thus leading to a variety of implications on the structural and electronic properties of the material [11,12].

Heteroepitaxial layers of 3C-SiC grown on silicon (Si) are characterized by a high density of structural defects, generated by the large lattice and thermal expansion coefficient mismatch. Among them, stacking faults (SF) and anti-phase-boundaries (APBs) can have a detrimental impact on the performances of both Schottky- and MOS-based devices [13,14]. On the other hand, while using hexagonal SiC substrates can provide a more favorable condition (in-plane lattice mismatch ~0.08% for 3C/4H), controlling the initial nucleation of 3C-SiC domains onto on-axis hexagonal SiC substrates is particularly difficult. Hence, *Jokubavicius et al.* [15] recently developed a growth idea based on sublimation epitaxy of 3C-SiC onto 4°-off axis hexagonal substrates, which enabled obtaining a significantly lower defects density, compared to the 3C-SiC crystals grown onto on-axis substrates.

Besides the aforementioned crystal growth issues, different technological impediments associated to fabrication processing steps for power devices (contacts, selective doping, gate oxides, etc.) still limit the introduction of 3C-SiC in power electronics [16]. As an example, one of the main technological challenges in the processing of 3C-SiC-based electronic devices is the achievement of Schottky contacts with almost ideal characteristics and acceptable leakage current level. Hence, in the last three decades many works studied the properties of Schottky contacts on n-type 3C-SiC layers, mostly grown on Si substrates, using high work-function materials (e.g., Au or Pt) [17,18,19,20,21,22,23,24,25,26,27]. First, *Eriksson et al.* [25] proposed a quantitative explanation of the limiting role of material defects on the functionality of Schottky barriers on 3C-SiC layer grown onto on-axis 4H-SiC, indicating the route towards ideal rectifying contacts. More recently, *Giannazzo*

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et al. [13] elucidated more clearly the specific role of APBs as the main responsible of the reverse bias leakage current. In addition, in that work a preferential current conduction has been observed in forward bias on both APBs and SFs [13].

Noteworthy, most of these papers were related to 3C-SiC grown onto foreign substrates (Si or 4H-SiC). In fact, the lack of good quality bulk 3C-SiC layers has hindered the development of functional vertical devices based on 3C-SiC. Only recently, *Li et al.* [28] preliminarily demonstrated the feasibility of p-n junctions on free standing 3C-SiC, obtained by chemical vapour deposition (CVD) of thick 3C-SiC layers onto Si(100) substrates, followed by melting and removal of the Si substrate.

In this work, we demonstrate the feasibility of fabricating vertical Schottky diodes on bulk 3C-SiC material, obtained by an innovative method combining sublimation epitaxy and chemical vapor deposition, starting from a 4°-off axis 4H-SiC substrate. By the cross correlation of different analyses, the degree of the Pt/3C-SiC Schottky barrier inhomogeneity in the fabricated diodes could be assessed and associated with the nanoscale electrical properties of the material. A comparison with the behavior of Pt/4H-SiC Schottky barrier reported in literature is also shown. In this view, the perspectives of bulk 3C-SiC for medium-voltage vertical power devices are discussed.

2. Experimental details

The initial 3C-SiC material was grown on the C-face of 4°-off-oriented 4H-SiC conductive substrates using fast sublimation epitaxy (FSE). More in detail, the growth of 3C-SiC was done in inductively heated graphite crucible. Inside the crucible, the raw materials for the growth were stacked in a sandwich-like arrangement in the following order: Ta foil at the bottom followed by polycrystalline SiC plate, graphite spacer and the 4H-SiC substrate. The design of the crucible and the arrangement of raw materials provide very high temperature gradient (~15-17 ^{o}C/mm) between the polycrystalline SiC plate and the 4H-SiC substrate and enables conditions for growth of bulk material [29]. The growth was performed in vacuum (10^{-4} mbar) at growth temperature varying from 1800 to 1950 °C. The choice of growing on C-face is based on the experimental findings that the crystalline quality is superior (less grain boundaries) as compared to growth on Si-face [30]. After sublimation epitaxy process, the 4H-SiC template was removed by grinding, leaving behind a free-standing 3C-SiC substrate with a thickness of about 800 μm and a background electron concentration in the range of 10^{17}cm^{-3}. This relatively high background electron concentration is due to the preferred nitrogen incorporation on the C-face [31]. Hence, the grown 3C-SiC material keeps the initial miscut and C-face front surface. The front side of such substrates was then subjected to chemo-mechanical-

polishing (CMP) with StepSiC process developed by NOVASiC [32]. As a result, a scratch-free, low roughness epi-ready surface was obtained, as will be discussed in the next section.

In order to achieve low, well-controlled carrier concentration, a 15 μm thick homoepitaxial 3C-SiC layer was grown by chemical vapor deposition (CVD) in a "home-made", low-pressure, horizontal, resistively-heated hot-wall CVD system with rotating sample holder, which is described in detail elsewhere [33]. Standard chemistry was used: silane (SiH_4) and propane (C_3H_8) as Si and C precursors, hydrogen (H_2) as carrier gas and nitrogen (N_2) as source of n-type doping [33]. Previous trials of C-face growth in our setup indicated that, at any growth temperature, the growth rate has to be considerably reduced with respect to Si-face in order to avoid poly-crystalline deposition. Furthermore, for hexagonal SiC polytypes, it is well-known that nitrogen (n-type dopant) incorporation on C-face is much stronger than on Si-face [31,34]. Also the residual (unintentional) n-type doping on C-face is stronger [34]. Finally, in our growth setup, we observed a higher dispersion of nitrogen doping profile. Hence, similar effects are expected for 3C-SiC growth. Consequently, high C/Si ratio (2.3), high-temperature (1800°C) and limited growth rate (below 20μm/h) conditions were adjusted to ensure high structural quality, prevent excessive nitrogen incorporation and achieve a target doping of $N_D=1\times10^{16}$ cm^{-3}. The growth pressure was fixed at 100 mbar. Five samples have been grown, with the CVD conditions given in table 1.

CVD run	**Sample name**	**Growth Temperature (°C)**	**Growth Rate (μm/h)**	**Epilayer Thickness (μm)**	**Nominal Doping (cm^{-3})**
Epi_01	CH-45	1800	14	11	4.0×10^{16}
Epi_02	CH-22	1800	13	14	9.8×10^{15}
Epi_03	CH-42	1700	16	17	n.a.
Epi_04	CH-46	1800	19	20	1.1×10^{16}
Epi_05	CH-50	1700	8	16	1.8×10^{16}

Table 1: CVD growth conditions used for the 3C-SiC epitaxial layers.

As one can see in table 1, two growth runs were performed at lower temperature (1700°C). However, at that temperature, the growth rate had to be further reduced, down to 8μm/h (sample #CH-50), since the deposition at 16μm/h resulted in formation of a polycrystalline layer (sample #CH-42).

Fig. 1 schematically shows the sequence of the processes performed to obtain the final bulk and CVD 3C-SiC epitaxial material.

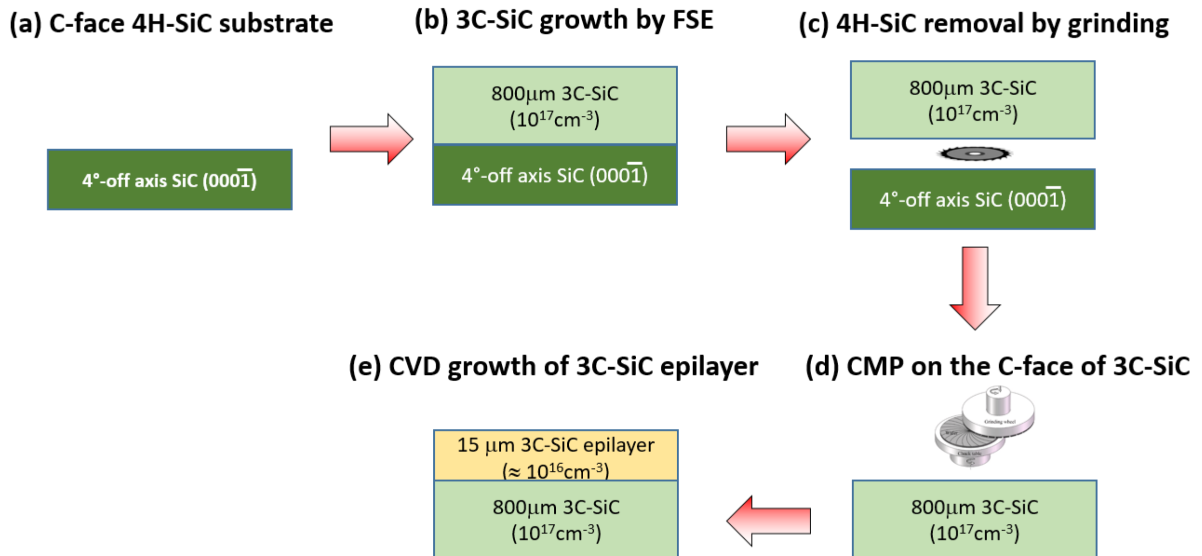

Fig. 1: Schematic of the processes sequence performed in order to obtain the 3C-SiC bulk epitaxial material for vertical Schottky diodes fabrication. In brackets electron concentration of the layers is indicated.: (a) starting C-face 4H-SiC substrate, (b) growth of a thick 3C-SiC layer by fast sublimation epitaxy (FSE), (c) removal of the 4H-SiC substrate, (d) chemical mechanical polishing (CMP) of the C-face of the 3C-SiC substrate to prepare the final epitaxial growth, (e) chemical vapor deposition (CVD) growth of the epitaxial layer.

To have a better insight in layer characteristics, the CVD runs were performed simultaneously on 3C-SiC substrates and C-face 4H-SiC control substrates.

Polished 3C-SiC substrates and as-grown 3C-SiC epitaxial samples were inspected by optical microscopy and atomic force microscopy (AFM) to assess the surface morphology. Standard X-Ray diffraction (XRD) analyses were performed to probe the crystalline quality of the grown material.
To demonstrate the material potential, vertical Schottky diodes were fabricated by synthetizing at 950°C nickel silicide ohmic contact as back- side electrode [35,36] and defining circular Pt Schottky contacts on the front epitaxial layer by optical lithography and metal lift-off [26]. The ohmic contact annealing process was carried out in nitrogen atmosphere in a Jipelec JetFirst 150 furnace.

Current voltage (I-V) and capacitance voltage (C-V) measurements were carried out to extract the electrical properties of the Pt/3C-SiC Schottky barrier, using a Microtech Cascade probe station and a Keysight B1505 parameter analyzer, varying the temperature between 25 and 150 °C.

3C-SiC epitaxial samples were also characterized at nanoscale by conductive atomic force microscopy (C-AFM), using a Bruker Dimension 3100 microscope. Diamond coated Si tips, ensuring high mechanical and electrical stability of the nano-contact on 3C-SiC surface, were used for these analyses.

3. Results and Discussion

3.1 Morphological and structural properties of the 3C-SiC material

The surface aspect of the 3C-SiC substrate and as-grown 3C-SiC epilayer are compared in Fig.2, showing both optical microscopy and AFM images of a representative sample (#CH22). As one can see, CMP prepared surface is featureless, scratch-free and extremely smooth, with a Root Mean Square roughness value RMS=1Å on a 5×5µm² scan area. AFM scans on larger areas of 20×20 μm^2 or 50×50 μm^2 (not shown) gave RMS values of 0.8 nm and 1.4 nm, respectively. The three vertical features, marked by crosses in Fig. 1a, are associated to the inclusions of hexagonal polytype, as will be discussed later based on XRD analysis. Moreover, some preferentially "line-shaped" defects can be observed in the optical images. These features are kind of groves, associated to the presence of double position boundaries (DPBs) that form during the 3C-SiC growth, and are preferentially oriented parallel to the miscut direction of the 4°-off-axis 4H-SiC substrate [15,29].

As one can see, the high-temperature CVD process reveals several substrate related features: lines along the off-cut axis (vertical on images) and at 60° with respect to that direction, as well as local buried defects. The surface remains smooth, and neither steps nor step-bunching formation is observed. On a larger AFM scan area (20×20µm²) the measured roughness is increased to RMS=3nm, due to the relief of "vertical" lines. However, between the lines, the RMS was in the Angstrom range. Consequently, no additional CMP was necessary before further sample processing.

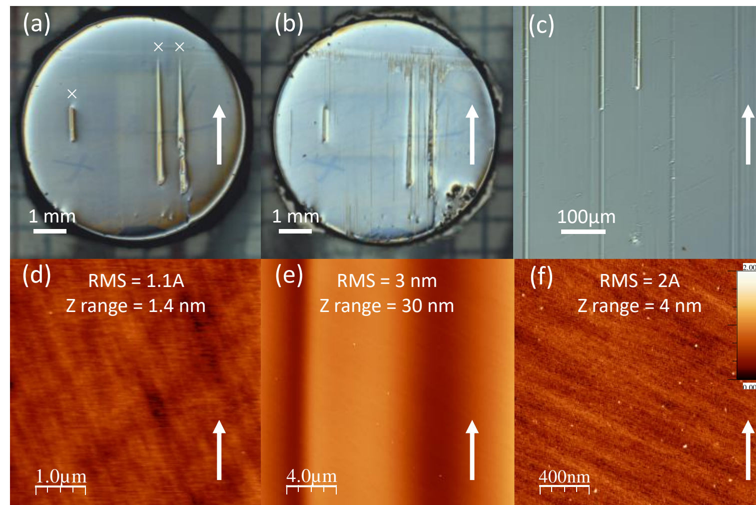

Fig. 2: Optical microscopy image (x5 objective) of sublimation grown 3C-SiC substrate (a) and as-grown epilayer (b)Three vertical features, marked by crosses, are the inclusions of hexagonal polytype; (c) detail (x20 objective). AFM scans of 3C-SiC substrate (d) and as grown CVD epilayer (e and f). Arrows indicate the direction of the off-cut axis.

X-ray diffraction (XRD) measurements were performed on different samples described in Table 1 (#CH22, #CH45, #CH46, # CH50), focusing on the properties of basal plane reflection. As can be

seen in Fig. 3a, in all cases the 2θ-ω scans (with analyzer) reveal double-peak structure of this reflection. The first peak at 2θ=35.60° can be associated to the 4H-SiC(004) reflection, whose intensity is correlated with the presence of residual 4H-SiC domains within the sample. The second peak, at 2θ=35.65° is related to 3C-SiC (111). The splitting indicates that the Si-C bilayer thickness measured along the c-axis in 3C-SiC (2.516 Å) is slightly lower than in 4H-SiC inclusion (2.520 Å). Similar splitting between 3C-SiC(111) and 4H-SiC(004) 2θ-ω peaks was previously observed for 3C-SiC epilayers on 4H-SiC substrate [37]. The 3C-SiC lattice parameter along the out of plane [111] direction is thus 7.549 Å. For perfectly relaxed 3C-SiC crystal (lattice constant 4.3602 Å [38], one should obtain 7.552 Å. The reduction of out of plane lattice parameter may be associated with increase of in-plane lattice dimensions, i.e. with tensile stress of 3C-SiC material. However, XRD measurement of asymmetric reflections are necessary to verify this hypothesis.

The full width at half maximum (FWHM) of the 3C-SiC(111) rocking curves (Fig. 3b) is in the range 70-160 arcsec, depending on the sample, which indicates a high structural quality of the 3C-SiC material. For all the grown samples, the values measured before and after CVD growth were the same. Hence, the low FWHM reflects the excellent substrate characteristics and does not indicate additional features to the quality of the epilayers.

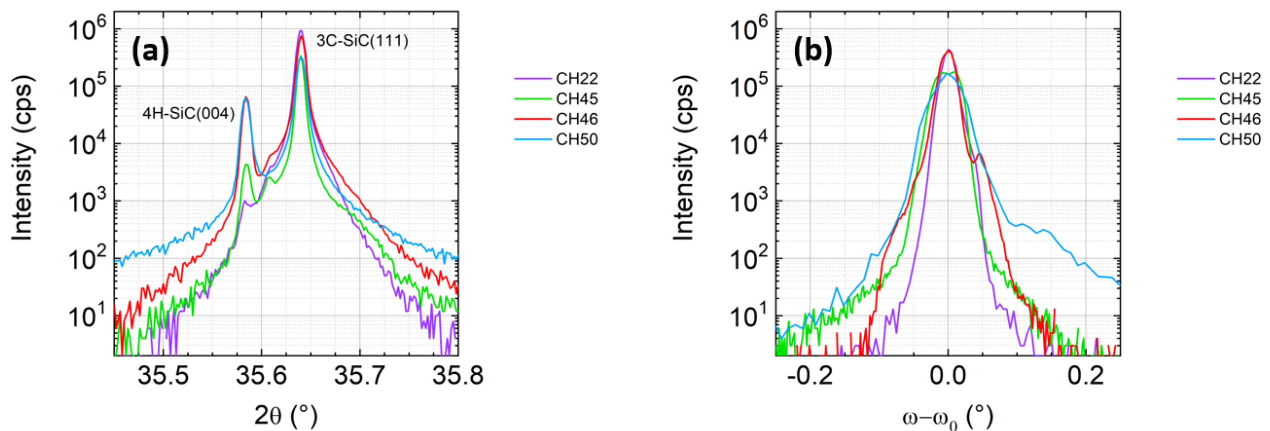

Fig. 3: (a) 2θ-ω XRD scans of basal plane reflection. Data from various samples are centered on 3C-SiC(111) peak. 4H-SiC(004) peak related to inclusions is more or less visible on the samples. (b) ω scans of 3C-SiC(111) peak on the same samples.

Among the grown samples, #CH22 was selected for device fabrication and nanoscale electrical analyses, since it exhibited the best features in XRD analysis (i.e. almost absence of residual 4H-SiC peak and the lowest FWHM). The results are described in sections 3.2 and 3.3.

3.2 Fabrication and characterization of vertical Pt/3C-SiC Schottky diodes

Vertical Pt/3C-SiC Schottky diodes were fabricated to get further insights on the electronic quality of the material for potential devices applications. Fig. 4a and 4b reports a schematic of the fabricated diodes, together with an optical microscopy image of the devices, respectively.

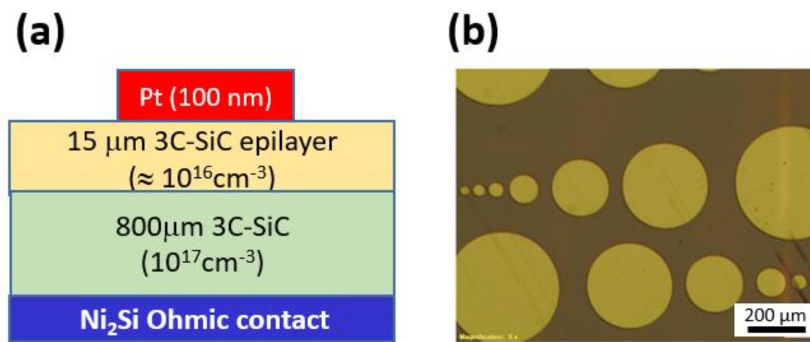

Fig.4: Schematic cross section (a) and optical microcopy image (b) of the fabricated vertical Pt/3C-SiC Schottky diodes.

Fig. 5 shows, in a semi log plot, the forward and reverse I-V characteristics of the fabricated Pt/3C-SiC Schottky diodes acquired at room temperature. The forward I-V characteristic of the diode, shown in Fig. 5a, could be described by the Thermionic Emission (TE) model [39]. Accordingly, in the linear region the forward current density J can be expressed as:

$$J = J_S \left[exp\left(\frac{qV_F}{nkT}\right) - 1 \right] \approx J_S \, exp\left(\frac{qV_F}{nkT}\right) \qquad \text{Eq. 1}$$

with

$$J_S = A^* T^2 \, exp\left(-\frac{q\Phi_B}{kT}\right) \qquad \text{Eq. 2}$$

where A^* is the Richardson constant, T is the measurement temperature, k is the Boltzmann constant, Φ_B and *n* are the Schottky barrier height and the ideality factor, respectively.

From the linear fit of the forward bias characteristic, an ideality factor of n=1.21 and a barrier height of Φ_B=0.60 eV could be determined using the TE model.

It must be pointed out that significantly higher barrier height values (the range 1.39-1.81 eV) are reported at room temperature for Pt Schottky contacts formed on the hexagonal 4H-SiC polytype [40,41,42]. This large difference can be associated to the electron affinity difference of about 1eV between these two polytypes [12,16].

On the other hand, the reverse characteristic shows a leakage current density of 1.5×10^{-2} A/cm^2 at a reverse bias of -10 V and a rectification ratio close to 10^5 at the applied voltage of +/-1 V. At reverse bias (-1V) the leakage current density is one order of magnitude lower (1.5×10^{-3} A/cm^2). Under similar bias conditions, a wide range of leakage current density values are reported in literature for simple silicon Schottky diodes, i.e. varying from 6.4×10^{-5} up to 1 A/cm^2 [43,44,45,46,47,48].

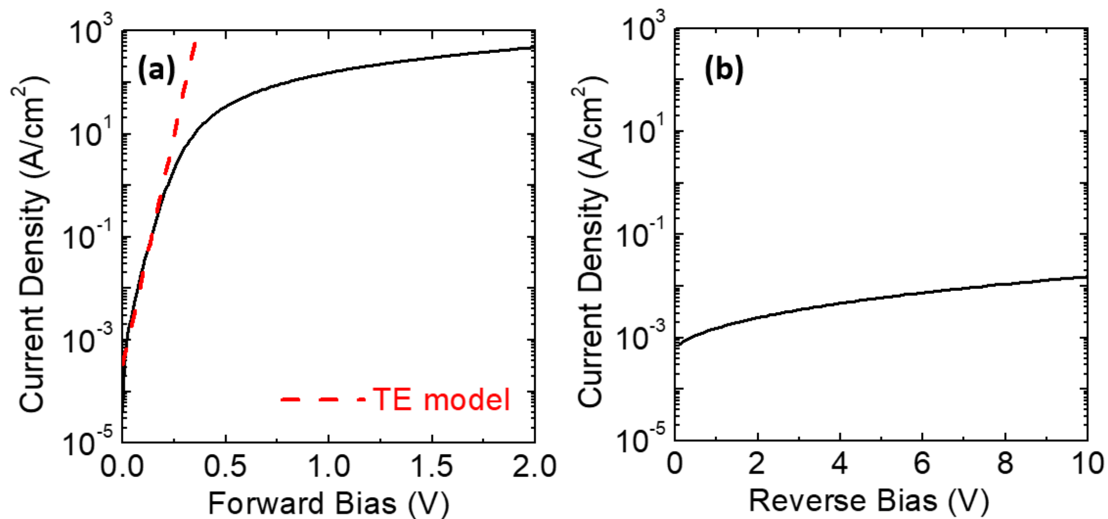

Fig.5: Forward (a) and Reverse (b) I-V characteristics of the fabricated Pt/3C-SiC Schottky diode. The dashed line in (a) is the linear fit obtained using the TE model.

The C-V curves and the corresponding 1/C^2 vs V plot are reported in Fig. 6a and Fig. 6b. From the linear fit of the 1/C^2 plot, it is possible to extract the value of the doping concentration of the epilayer [39]. In particular, in our case we found a value of of N_D=1.54×10^{16} cm^{-3}, which is very close to the nominal doping level targeted in the CVD process (see table 1). Noteworthy, the value of the barrier height determined by the C-V analysis was 0.83 eV, i.e. higher than the value extracted by I-V. This latter, is an indication of the formation of an inhomogeneous barrier. In fact, the I-V measurements

are typically affected by the presence of preferential leakage current paths with lower barrier height. Since the C-V measurements are carried out under reverse bias, the potential at lower barrier regions is pinched-off by the neighbors regions, thus resulting into a higher experimental barrier height value with respect to that extracted by I-V [49,50].

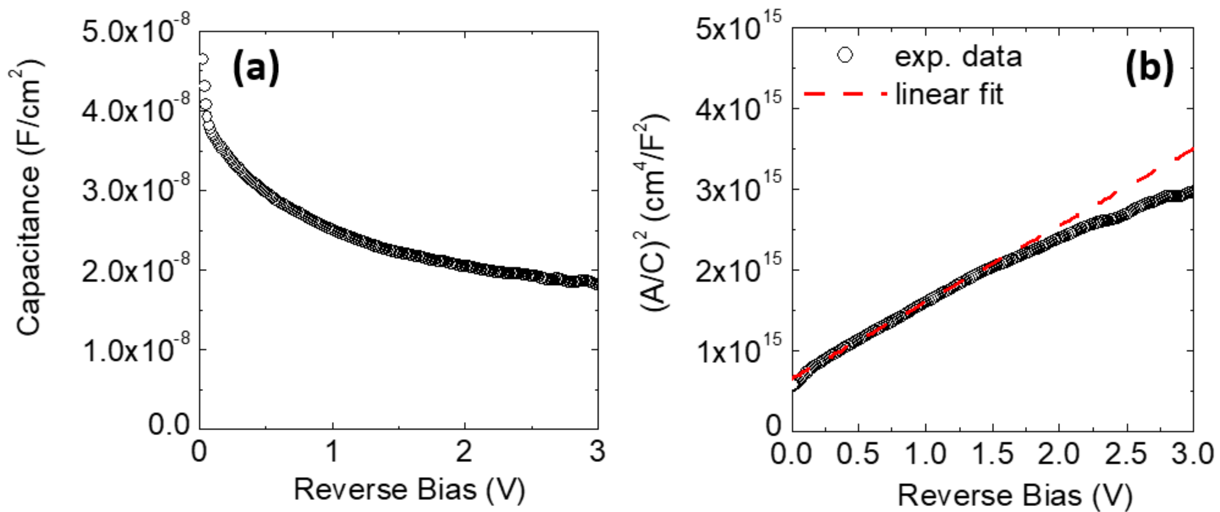

Fig. 6: (a) C-V curve acquired on the fabricated Pt/3C-SiC Schottky diode. (b) Plot of $1/C^2$ as a function of the reverse bias. The linear fit is also reported.

To learn more on the conduction mechanisms and homogeneity degree of the Schottky barrier height, the I-V characteristics of the diode have been acquired both under forward and reverse bias at different temperatures.

Fig. 7a displays the I-V characteristics in forward bias, measured in the temperature range between 25 °C and 150 °C. As can be seen, for moderate bias values, the forward current density increases with increasing the measurement temperature. For each temperature, the ideality factor and the Schottky barrier height have been extracted from the fit of the forward I-V curves, by using the thermionic emission (TE) model. As shown in Fig. 7b, the ideality factor decreases from 1.21 at 25°C down to 1.06 at 150°C. At the same time, the barrier height increases from 0.60 eV (25°C) to 0.68 eV (150°C). A similar trend with the temperature of these two parameters has been already observed in Schottky diodes on the hexagonal polytype 4H-SiC [51,52].

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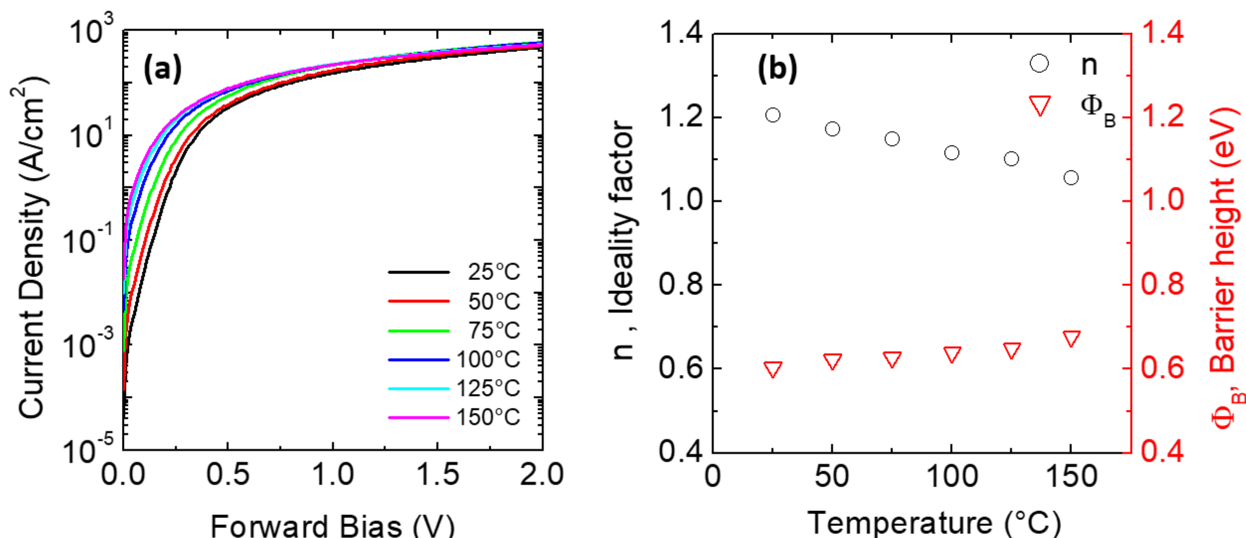

Fig. 7: (a) Forward I-V characteristics of the fabricated Pt/3C-SiC Schottky diode acquired at different measurement temperatures (in the range 25-150 °C); (b) Temperature dependence of the ideality factor and barrier height, extracted from the forward I-V characteristics of the Pt/3C-SiC Schottky diode.

Fig. 8a reports a plot of the barrier height as a function of the ideality factor, which clearly shows a linear correlation between these two parameters. This behavior is typically observed in inhomogeneous Schottky barriers [51,53]. In particular, from the observed trend, it was possible to extrapolate the value of the barrier (Φ_B^0) expected for an ideal contact (at n=1), i.e. $\Phi_B^0 = 0.70$ eV. In inhomogeneous barriers, multiple regions of different barrier heights exist at the metal/semiconductor interface. According to Tung's model, these systems can be seen as a distribution of low-barrier "patches" immersed inside a region with a uniform higher-barrier height [54]. The extrapolated barrier Φ_B^0 in Fig. 7a can be identified with the ideal homogeneous barrier embedding the regions with lower barrier height [53]. Then, at higher temperatures, the uniform barrier will dominate the current transport, while decreasing the temperatures the lower barriers become more relevant. This scenario explains well the temperature dependence of the barrier observed in Fig. 8a.

For the sake of comparison, the correlation between the barrier height and ideality factor observed by *Huang et al.* [41] for Pt Schottky barrier on the hexagonal polytype 4H-SiC is also displayed in the inset of Fig. 8a. In this case a value of Φ_B^0=1.87 eV could be extrapolated at n=1, which is much higher than that found in 3C-SiC for the reason discussed above. To have a more quantitative indication on the inhomogeneity degree of the barrier and the deviation from the ideal behavior, it is useful to report a plot of *nkT* as a function of *kT*, as displayed in Fig. 8b. As can be seen, at low temperature the experimental data for our Pt/3C-SiC diode lie almost parallel to the straight line describing the ideal behavior (n=1). Then, at the highest temperatures, the data tend to gradually

approach the ideal behavior. Such a temperature dependence of the ideality factor occurring in inhomogeneous barriers is often regarded as T_0 anomaly [55], i.e. the ideality factor can be approximately expressed as $n=1+T_0/T$. In the case of Pt/3C-SiC barrier, a value of T_0=62K could be determined. As can be noted in the inset of Fig. 8b, the literature value of T_0 for Pt Schottky contacts on 4H-SiC is significantly lower (T_0=32K) [41], which denotes still a better interface quality obtainable in the case of the mature hexagonal 4H-SiC polytype.

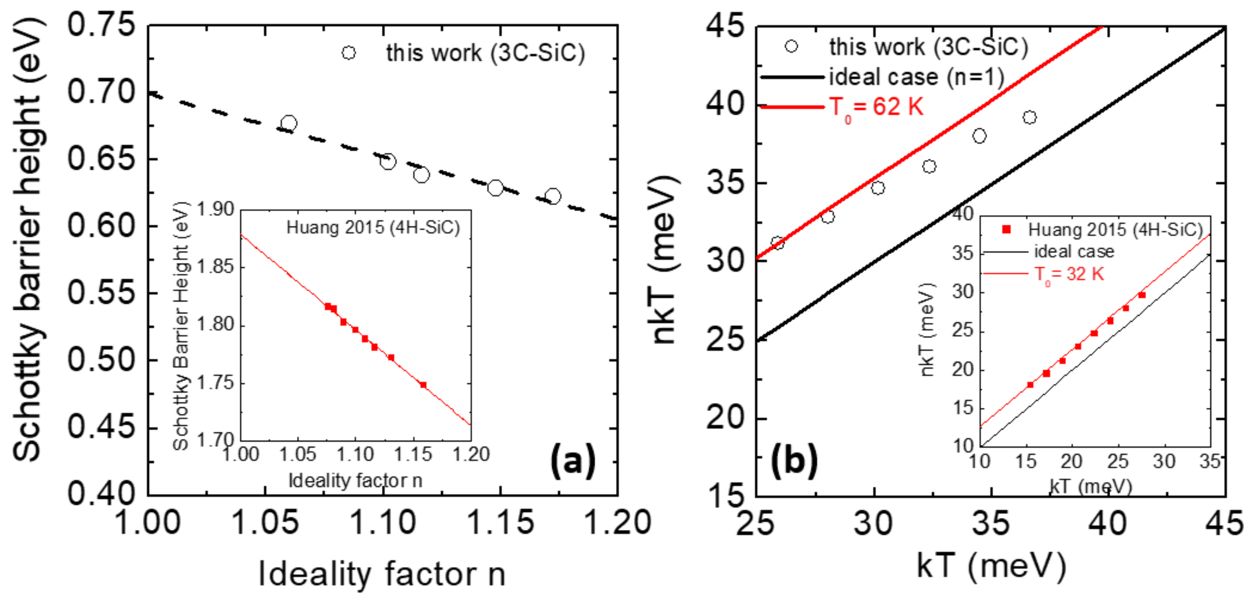

Fig. 8: (a) Correlation plot of the barrier height as a function of the ideality factor. The dashed line is a linear fit of the data, from which a value of Φ_B^0=0.70eV could be extrapolated at n=1. (b) Plot of nkT as a function of kT, showing the deviation from the ideal behavior and the T_0 anomaly (with T_0=62K). The insets show analogous plots obtained for the case of the Pt/4H-SiC Schottky barrier using literature data. In this case, the values of Φ_B^0=1.87eV and T_0=32K could be determined. These insets were reproduced with permission using the data from Ref. [41]. Copyright 2015 IOP Publishing.

Finally, the study of the Pt/3C-SiC Schottky contact behavior was completed by analyzing the temperature dependence of the reverse I–V characteristics of the diodes. Fig. 9 reports the reverse I-V characteristics of the diodes acquired at different temperatures. In the same graph, the fits of the experimental curves obtained using the thermionic field emission (TFE) model, including the image force lowering effect [56] and assuming the value of the doping concentration obtained by the C-V analysis ($N_D=1.54\times10^{16}$ cm^{-3}). Indeed, according to the TFE model, under reverse bias, the current density can be expressed as [56]:

$$J_{TFE} = A^*T^2\sqrt{\frac{q\pi E_{00}}{kT}}\sqrt{V_R + \frac{q\overline{\overline{\Phi_B}}}{cosh\left(\frac{qE_{00}}{kT}\right)^2}} \, exp\left(-\frac{q\overline{\overline{\Phi_B}}}{E_0}\right) exp\left(\frac{qV_R}{kT} - \frac{qV_R}{E_0}\right) \quad \text{Eq. 3}$$

with $E_0 = E_{00}\, coth\left(\frac{E_{00}}{kT}\right)$, $E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N_D}{m^*\,\epsilon}}$ and where m^* and ε are the electron effective mass and the dielectric constant of the semiconductor, respectively.

In Eq. 3, the image force lowering effect has been taken into account, by considering the following expression for the barrier height $\overline{\overline{\Phi_B}}$ [39]:

$$\overline{\overline{\Phi_B}} = \Phi_B - \left[\frac{q^3N_D}{8\pi^2\varepsilon^3}(V_{bi} - V_R)\right]^{\frac{1}{4}} \quad \text{Eq. 4}$$

As can be seen, the reverse curves simulated with the TFE show an excellent agreement with the experimental ones in the whole temperature range, considering an increasing barrier height with the temperature. In this case, however, the values of the barrier height leading to good TFE fits of the experimental curves are slightly higher than those extracted by the TE model in forward bias. These findings are coherent with previous works on 4H-SiC Schottky contacts, which indicated that the presence of interface inhomogeneity can enhance the tunneling contribution under reverse bias and lead to the occurrence of a TFE mechanism [57,58]

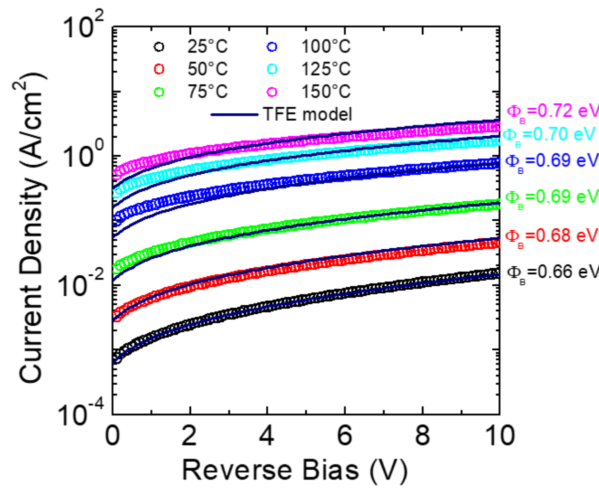

Fig. 9: Reverse *I-V characteristics of the fabricated Pt/3C-SiC Schottky diode acquired at different measurement temperatures (in the range 25-150 °C). The fits of the curves obtained with the TFE model are also reported.*

3.3 Nanoscale electrical properties of the 3C-SiC epilayer

The nanoscale electrical properties of the material have been assessed by means of local electrical measurements performed by C-AFM. Fig. 10a and 10b show the correlation between the C-AFM

morphology and the current maps collected on the 3C-SiC bare surface on a 50×50 μm^2 scanned area. During the scan, a positive bias (V_{tip}= + 0.5 V) was applied between the diamond tip and the sample's backside, while the locally injected current at the tip/3C-SiC nano-contact was collected by a high sensitivity current sensor connected to the tip.

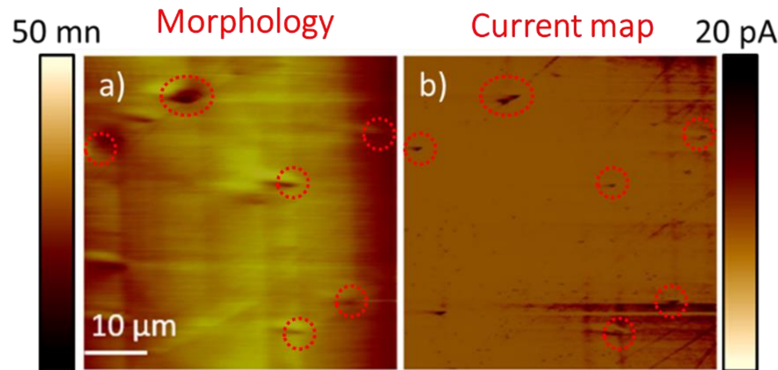

Fig. 10. (a) AFM map of the surface morphology and (b) current map acquired by C-AFM on the bare surface of the free standing 3C-SiC, obtained by applying a V_{tip} = + 0.5 V

The current map in Fig. 10b generally exhibits a uniform contrast, with the presence of some conductive points (indicated by red circles in the figure), correlated to pits in the surface morphology. These features are approximately 2-5 nm deep and about 1-2 μm in size. From the C-AFM image, it can be estimated that these defects cover approximately 1/50 of the sample surface. Such "point-like" conductive features, visible in the two-dimensional current map, are likely to be associated to uni-dimensional crystalline defects (e.g. threading dislocations) running through the epitaxial layer and connecting the 3C-SiC surface to the doped substrate. Performing a statistical analysis on several C-AFM current maps, the areal density of these conductive defects was estimated to be in the order of about 3×10^5 cm^{-2}. It must be pointed out that the 3C-SiC layers grown on Si substrates are often characterized by the presence of both uni-dimensional and bi-dimensional crystallographic defects [13], such as SFs and APBs, having a detrimental effect on both the Schottky barrier and the metal-oxide-semiconductor robustness [13,14]. Noteworthy, in the present case, SF and APB could not be detected within the typical scan areas probed by the C-AFM (comparable to the size of the fabricated Pt/3C-SiC Schottky contacts), differently than in previous C-AFM investigation performed on 3C-SiC grown on Si, where typical areal densities of SF of ~5×10^6 cm^{-2} and of APB of ~2×10^5 cm^{-2} were observed [13]. As a matter of fact, lateral Pt Schottky diodes fabricated on those 3C-SiC layers grown on Si [13,14,36] exhibited leakage current density values at -10 V higher than 1.5×10^{-1} A/cm^2, i.e. higher than those measured in the present study in bulk 3C-SiC (see Fig. 5b). The lowered density of conductive defects in the bulk 3C-SiC layers confirms the excellent quality of the material, which can

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be then very promising for the realization of functional vertical devices. In this context, past works reported on the possibility to electrically passivate near-surface defects in 3C-SiC layer by appropriated thermal oxidation or UV-light annealing processes [59,60]. However, while it is reasonable that these processes can be beneficial also for the passivation of the conductive defects observed in our bulk 3C-SiC material, dedicated experiments are needed to demonstrate the feasibility of these approaches.

4. Conclusion

In conclusion, fast sublimation growth of 3C-SiC on 4°-off-axis 4H-SiC substrates was used in this work to produce a template for bulk 3C-SiC epilayers growth of good crystalline quality and smooth morphology. On these bulk 3C-SiC epitaxial samples, Pt Schottky diodes have been fabricated and characterized, in order to get both fundamental insights on the metal/3C-SiC system, demonstrating at the same time the possibility to obtain functioning vertical devices on the cubic SiC polytype. The fabricated Pt/3C-SiC diodes showed an ideality factor of 1.21 and a barrier height of 0.6eV. The temperature dependence of the electrical characteristics indicated the formation of an inhomogeneous barrier. The barrier inhomogeneity revealed by the macroscopic electrical behavior has been associated to the presence of conductive defects on the surface detected by nanoscale local current measurements, whose density however is much lower that than typically observed in 3C-SiC layers grown on Si. On the other hand, the reverse leakage current could be well described by thermionic field emission model including image force lowering.

The improved material quality and the feasibility of fabricating vertical diodes based on 3C-SiC with a low Schottky barrier open interesting perspectives for the possible applications of the cubic polytype for medium-voltage power devices. In fact, the lower barrier of Pt on 3C-SiC with respect to 4H-SiC polytype can be exploited for the fabrication of Schottky-based devices with low turn-on voltage and, hence, lower power consumption. However, the future application of bulk 3C-SiC in power devices remains strictly related to a further reduction of the defect density of the material and to the employment of an optimized device design to minimize the reverse leakage current.

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