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Development of the power supply of HEPD-02 instrument on board CSES-02 satellite

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Abstract: The High Energy Particle Detector HEPD-02 is primarily devoted to observe fluxes of cosmic-ray electrons, protons and light nuclei, with kinetic energies in the range from less than 10 MeV to few hundreds MeV, either incoming or trapped in the terrestrial magnetosphere. HEPD-02 will be hosted on board the China Seismo-Electromagnetic Satellite CSES-02. The CSES mission, coordinated

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by China National Space Administration (CNSA) and Italian Space Agency (ASI), aims at developing a series of satellites for the study of the near-Earth environment, by means of electromagnetic, ionospheric, magnetospheric and cosmic-ray observations. HEPD-02 is a state-of-the-art instrument for measurement of energy and arrival direction and for identification of incoming cosmic particles; it is formed by a tower of superimposed plastic and crystal scintillator layers, read-out by photo-multiplier tubes (PMTs), with a direction detector composed of monolithic active pixel sensors.

This paper describes the design, structure and operation of the power supply component of HEPD-02, which comprises a low-voltage unit for power distribution to other sub-systems and a high-voltage unit for generation of PMT bias. The HEPD-02 power supply features specific and optimized design solutions matching the demanding requirements for employment on board the CSES-02 satellite: it is conceived to guarantee at least 6 years of continuous operation, delivering stable voltages with low susceptibility to electromagnetic interference, in a harsh environment (characterized by relatively intense ionizing radiation, wide temperature excursions, absence of heat dissipation by air convection), after sustaining strong mechanical stresses at launch, at the same time complying with strict limits in mass, dimensions and available power.

KEYWORDS: On-board space electronics; Control systems; Instrument optimisation; Space instrumentation

2025 JINST 20 P06005

Contents

1 The HEPD-02 instrument **1**

2 Design criteria of the HEPD-02 power supply **3**

3 Low-voltage power supply **4**
3.1 LV-DCDC board 6
3.2 LV-CTRL board 9

4 High-voltage power supply **14**
4.1 HV-PS mechanical structure 15
4.2 HV-PS operation 17

5 Conclusions **19**

2025 JINST 20 P06005

1 The HEPD-02 instrument

The High-Energy Particle Detector HEPD-02 is one of the payloads that will equip the second China Seismo-Electromagnetic Satellite (CSES-02), designed to operate on a quasi-polar, Sun-synchronous, low-Earth orbit. The CSES scientific space program ([1]) foresees the development of a multi-satellite monitoring system and includes several missions scheduled for the next years. The first satellite (CSES-01) was launched in 2018, while the second one (CSES-02) is currently under development and expected to be launched in the first half of 2025.

The CSES space mission is dedicated to monitor the variations of electromagnetic fields, plasma parameters and particle fluxes in the near-Earth space, induced by natural sources and artificial emitters, in particular investigating possible correlations between such perturbations and the occurrence of high-magnitude seismic events. Other fundamental scientific targets are the study of space-weather phenomena ([2]) and cosmic-rays ([3]).

The HEPD-02 instrument ([4]) was developed by the Italian Limadou collaboration; it is aimed at measuring the fluxes of charged particles, either incoming or trapped in the terrestrial magnetosphere. Particle detection is entrusted to various layers of scintillator detectors and a pixel direction detector, optimized for high-efficiency identification of individual electrons and protons with kinetic energies in the range from 3 to 100 MeV and from 30 to 200 MeV, respectively, and allowing for measurement of energy and incoming direction. The design of HEPD-02 takes advantage of the previous experience gained with HEPD-01 ([5]) installed on-board CSES-01 satellite, leading to the introduction of several innovations and improvements in the new payload.

The HEPD-02 detectors (figure 1) are arranged in a tower along the instrument axis, which is normally pointing towards the zenith during orbital flight:

- TR1, TR2: two planes of Eljen EJ-200 plastic scintillator ([6]) for triggering data acquisition; they are segmented into mutually orthogonal bars and positioned on top and bottom of direction detector;

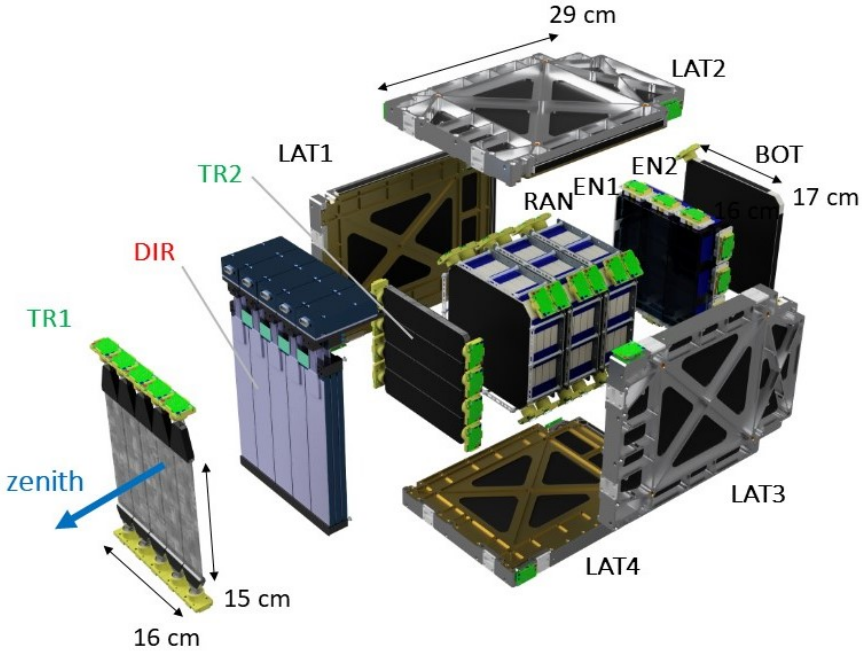

Figure 1. Exploded view of HEPD-02 detectors. PMT PCBs are outlined as green rectangles.

- DIR: direction detector ([7]), consisting of five independent turrets; each turret is made of three superimposed sensitive layers ("staves") of Monolithic Active Pixel Sensors (MAPS), with 5×2 sensors per stave;
- RAN: twelve EJ-200 planes ([6]) for incoming particle range assessment;
- EN1, EN2: two layers of LYSO scintillator ([6]), segmented into orthogonal bars, for energy measurement;
- LAT1, . . . , LAT4, BOT: five EJ-200 containment detector layers ([6]), surrounding the sides (LAT) and bottom (BOT) of the tower.

Overall the instrument contains 32 scintillator pieces (bars or planes), each one read-out with two Hamamatsu R9880-210 Photo-Multiplier Tubes (PMTs) placed at opposite ends. Each PMT is mounted on a dedicated high-voltage distribution PCB.

The instrument control and data acquisition is managed by specialized boards:

- data processing and control unit (DPCU), constituting the digital interface with CSES-02 satellite;
- trigger board ([8]), to read-out the PMT signals and generate the particle-crossing trigger signals;
- tracker data acquisition (TDAQ) board ([9]), to read-out the DIR pixel data.

The power supply is managed by two units, which make up the topic of the present paper:

- low-voltage power supply (LV-PS), distributing power from the satellite to all the HEPD-02 sub-systems;
- high-voltage power supply (HV-PS), dedicated to the generation of PMT bias voltages.

2025 JINST 20 P06005

2 Design criteria of the HEPD-02 power supply

The design work of the LV-PS and HV-PS units was carried out in such a way to match the general instrument requirements concerning reliability and operating conditions imposed by the orbital environment, structural requirements (mechanical and thermal robustness), physical limits (mass, dimensions), available power from satellite, expected working performance in terms of stability of supplied voltages and interference susceptibility. The ECSS (ESA) criteria were used as general guidelines, together with the experience gained with the development of HEPD-01 payload.

As regards reliability, the main requirement was to guarantee a fully operational life span of 6 years minimum, taking into account the expected aging, in particular from thermal stresses and environmental radiation (expected ~ 1 krad/year of absorbed dose during CSES-02 flight).

In order to comply with this requirement, space qualified electronic parts were selected for the most critical circuits (e.g. primary DC/DC voltage converters), when available and affordable, while other circuits employ parts with automotive or industrial qualification, that were successfully used for several years during previous low-Earth space missions, in particular HEPD-01.

For what concerns FPGAs, the Microsemi ProASIC 3 series was selected because of its configuration memory based on flash technology, showing relatively strong radiation tolerance. In fact, no susceptibility was observed for more than 20 krad of total ionizing dose. On the other hand, the cross-section for single-event effects (SEE) amounts to $\sim 10^{-4}$ cm^2/kbit, made up of recoverable events, with a negligible contribution from potentially dangerous latch-ups:[1] since the implemented LV-PS and HV-PS logics requires few kbits of flip-flops, and given the expected radiation environment along the CSES-02 orbit, the estimated SEE rate turns out to be $\sim 10^{-2}$/year, with no practical effect on operation.

Additionally, a cold redundancy architecture was adopted for LV-PS and HV-PS electronics, i.e. a given circuit is present in two physical copies, indicated as hot (or main) and cold (or spare): this solution substantially increases the overall reliability, at the expense of a limited additional design complexity related to the duplication of PCB areas and implementation of appropriate external connections with non-redundant circuitry.

Regarding the structural requirements, the main constraints guiding the design were:

- the need to keep weight within the allowed budget: 1.5 kg for LV-PS, 3.5 kg for HV-PS;
- the need to stand the expected mechanical stresses, in particular those applied to the assembled HEPD-02 instrument in the most demanding conditions, i.e. during qualification tests: sinusoidal sweep from 10 to 100 Hz with peak acceleration up to 12 G, sustained random loading (10 Hz to 2 kHz) with overall RMS value of 11.3 G, shock pulse (100 Hz to 4 kHz) with peak value up to 1000 G;
- the need to properly dissipate heat through the instrument base plate in vacuum environment (i.e. without air convection), considering that correct circuit operation must be guaranteed during the demanding qualification tests, with base plate temperature varied between -30°C and $+50$°C.

The conflicting requirements of limited weight and mechanical robustness, as well as efficient heat dissipation, were matched by employing high-performance space-grade aluminium alloy (EN AW

[1] Information on radiation susceptibility of ProASIC 3 series can be found on the vendor site: https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/proasic-3-fpgas.

2025 JINST 20 P06005

6082 T651) for both the LV-PS and the HV-PS support frames. For the same purposes, a relatively complex and expensive design and manufacturing process was adopted, with each frame obtained from a single solid block with no internal joints and shaped with multiple surface ribs to increase stiffness. Anchoring points towards surrounding mechanics further limit frame oscillations. This approach allowed to obtain acceptable local accelerations on electronic boards and negligible structural resonance effects, as verified both with simulations and during the above mentioned qualification tests of the HEPD-02 apparatus.

To satisfy the heat dissipation requirement, the thermal contact between electronic boards and surrounding frames was increased by implementing wide exposed copper bands on board surfaces, which are properly tightened to the underlying support frame in the assembled unit. Additionally, frame extrusions implement local thermal contact with the electronic parts producing most of the heat on each board. To avoid mechanical stresses on the plastic cases of the parts, the contact is mediated by soft pads characterized by low thermal resistance (Laird TFlex HD80000). A thermal simulation of the apparatus allowed to determine the expected variation of local temperature for each electronic part during operation. Each part was therefore chosen having a suitable operating temperature range, by applying wide safety margins in compliance with ECSS criteria. The correct circuit functionalities were finally verified with varying base plate temperature during the qualification tests.

As regards the requirements on stability of delivered voltages, all the employed primary and secondary voltage converters are characterized by wide enough range of accepted input voltages, in particular considering the allowed variability ($\pm 10\%$) of the satellite power bus voltage and appropriate safety factors to take into account temperature and aging drifts. Several solutions were implemented to guarantee low enough susceptibility to both conducted and radiated interference: an electromagnetic interference (EMI) filter is installed on LV-PS, downstream the satellite power bus; as much as mechanically feasible, all electronic boards and inter-connections are completely shielded by support frames and cable screens; an optimized grounding scheme was adopted to minimize interference conveyed by ground loops (see section 3).

A further specific requirement for high-voltage parts (HV-PS) was to guarantee the absence of discharges in the in-flight low-pressure environment ($P < 6.65$ mPa), also taking into account the possible contribution of material outgassing, which can locally produce more demanding pressure conditions (i.e. pressure can moderately increase, thus lowering the breakdown voltage as described by Paschen's curve). This requirement was matched by several design features, such as: employing low-outgassing materials, implementing appropriate geometric separation around high-voltage parts on board surfaces, filling the gaps with encapsulant material characterized by high dielectric strength, taking extreme care to avoid that residual substances may deposit on board surfaces during manufacturing and thus create low-resistance paths for discharges.

It is also worth mentioning a specific constraint for CSES satellites, namely to avoid extensive use of ferromagnetic materials, which may interfere with the magnetic measurements performed by other payloads. This requirement led to discard materials containing iron and nickel for mechanics and harness.

3 Low-voltage power supply

The low-voltage power supply unit (LV-PS) accomplishes the main task of converting the 29.5 V input voltage of satellite power bus into the 12 V primary voltage distributed to the HEPD-02 sub-systems

2025 JINST 20 P06005

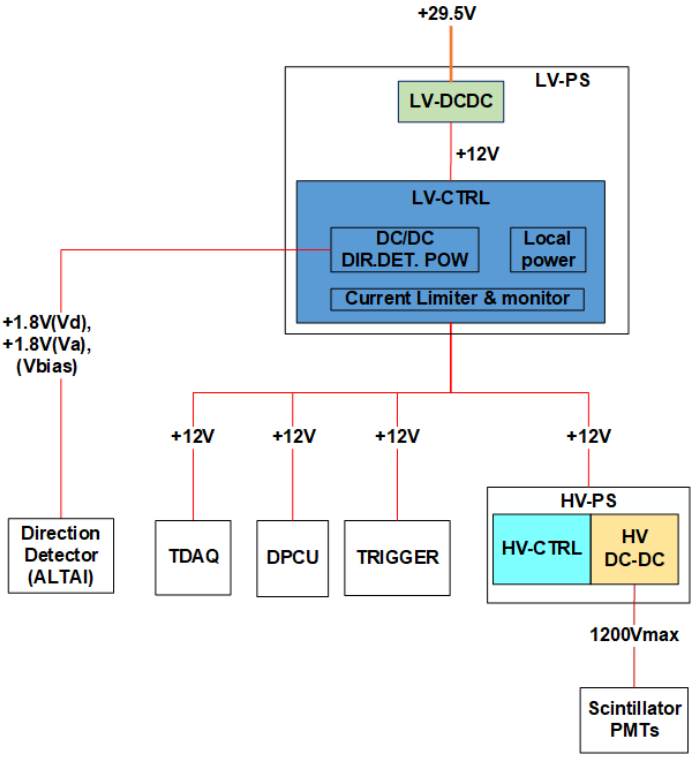

Figure 2. The HEPD-02 power distribution tree.

and into additional lower voltages, necessary for operating the direction detector (DIR), according to the power distribution tree shown in figure 2. Besides voltage conversion, the unit directly manages the low-level wired telecommand and telemetry interface with the satellite platform. During the initial phases of HEPD-02 switch-on, the LV-PS unit carries out the controlled power-on of the data processing and control unit (DPCU), while monitoring the correct start-up of DPCU, which subsequently takes control of the system for normal operation.

Compared to the LV-PS unit of HEPD-01 (described in [10]), most of the design was improved with new circuits and parts, in particular by implementing more performing fault protection circuits and continuous monitoring of the voltages and currents supplied to each load.

The LV-PS unit is composed of two electronic boards, defined as "low voltage DC/DC" (LV-DCDC) and "low voltage control" (LV-CTRL), housed in a compact mechanical structure formed by two interconnected aluminium-alloy frames. The two boards implement the separation of circuits with interfaces towards the satellite from those with interfaces towards the HEPD-02 sub-systems. According to this approach, the LV-DCDC board contains the interface with the satellite power bus, EMI filter, primary DC/DC voltage converter, the circuits for management of wired telecommands (TC) and telemetries (TM). On the other hand, the LV-CTRL board contains the FPGA for unit control, the circuits for distribution of 12 V primary voltage to sub-systems, the DC/DC voltage converters to supply power and bias lines to DIR, as well as the housekeeping circuits for the unit itself and for the power distribution tree.

In terms of layout, both electronic boards are divided into a common area for interface with external non-redundant electronics (satellite interface and DIR electronics), a hot and a cold area

2025 JINST 20 P06005

interfacing respectively with the main and spare circuits of HEPD-02 sub-systems (DPCU, Trigger board, TDAQ, HV-PS).

The grounding scheme implemented in HEPD-02 system and in particular in the LV-PS unit is shown in figure 3. It is designed to keep the satellite power bus ground, instrument signal ground and chassis ground lines electrically isolated from each other, apart from a single point outside HEPD-02, where they are physically connected, in such a way to minimize mutual interference injected via ground loops.

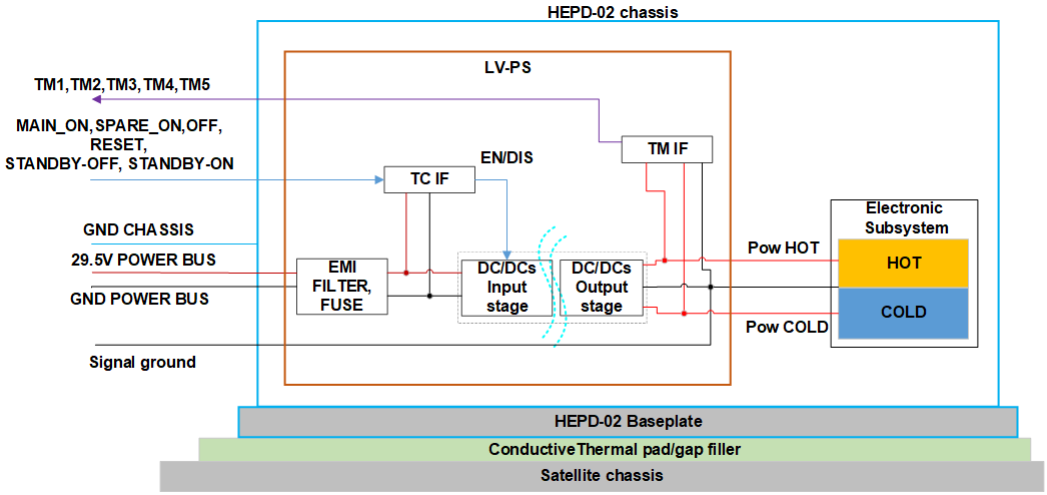

Figure 3. The HEPD-02 grounding scheme.

The LV-PS unit is completely enclosed in an aluminium-alloy container formed by two half-frames joined with screws (figure 4), with overall dimensions 29.8 cm × 24.3 cm × 4.0 cm. Internally, the LV-CTRL board is installed on the bottom half-frame, while the LV-DCDC board is subsequently connected on top of it, allowing for the insertion of appropriate inter-board spacer columns, which contribute to the assembly stiffness. Finally, the top half-frame is installed to close the unit. Three structural cages for EMI filter module and hot/cold primary DC/DC voltage converters are anchored to the LV-DCDC board (see figure 5); these cages are necessary to mechanically stabilize these bulky parts and to efficiently convey heat flow towards the frames.

3.1 LV-DCDC board

The LV-DCDC board architecture is represented as a block diagram in figure 6. It includes power management circuits, wired telecommands (TC) interfaces and wired telemetries (TM) interfaces. The board has four connectors: J1 for interfacing with the satellite (power, wired TC and TM signals), J2 for read-out of two PT1000 temperature sensors used to generate the corresponding TM signals, J3 and J4 for direct connection with the hot and cold sections of the LV-CTRL board.

The power management features a redundant Yunke MF3216 series fuse, for short-circuit protection of 29.5 V satellite power bus, followed by an EMI filter (ECRIM HFH100) and a fully redundant power circuit. This circuit contains an inrush current limiter made by discrete components (designed on the basis of the inrush requirements from satellite) and the primary DC/DC voltage converter (ECRIM HDCD(20-50)-12-60/SP), with banks of input/output filter capacitors appropriately sized according to the maximum current absorbed by the instrument. The fuse, filter and DC/DC

2025 JINST 20 P06005

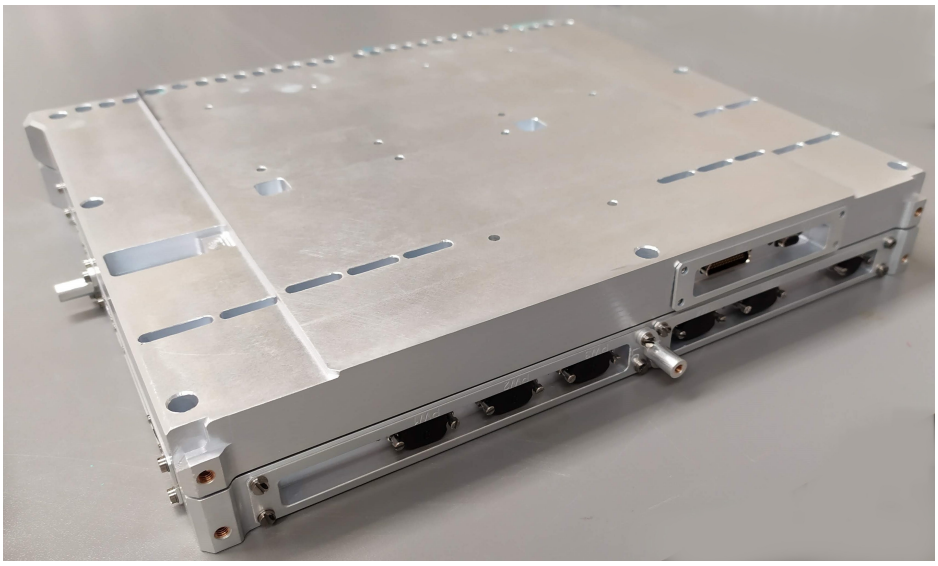

Figure 4. The LV-PS unit fully assembled. The overall dimensions of the unit are 29.8 cm × 24.3 cm × 4.0 cm.

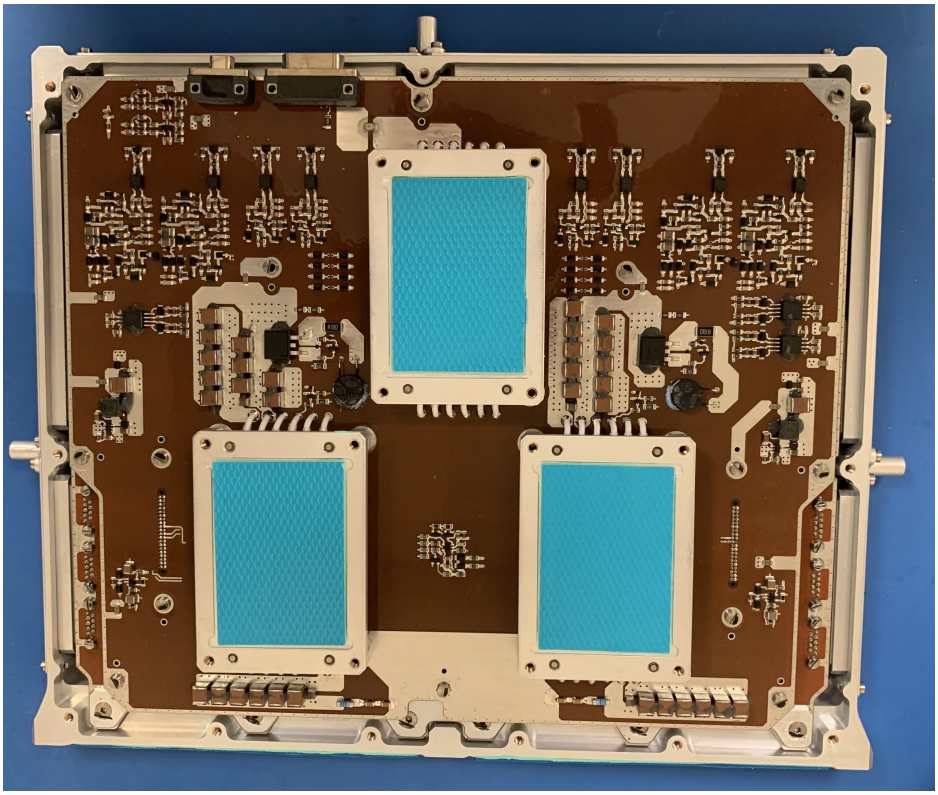

Figure 5. Partially assembled LV-PS unit, with the three structural cages mounted over EMI filter (top) and hot and cold primary DC/DC converters (bottom).

2025 JINST 20 P06005

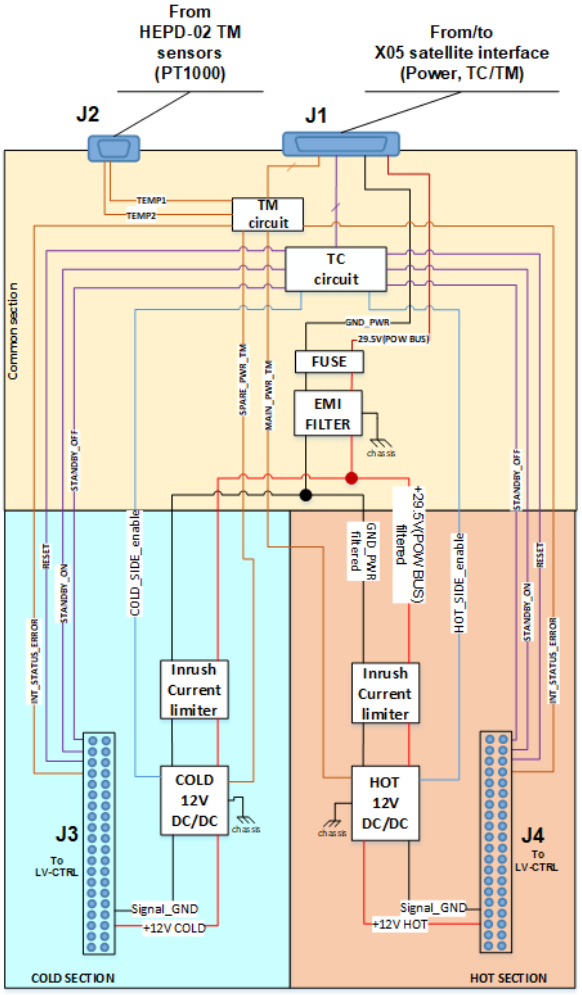

Figure 6. LV-DCDC board architecture.

converter are space qualified in compliance with China Academy of Space Technology (CAST) requirements stated in CAST standard "C".

The TM circuit generates the following 5 V signals towards the satellite, by using redundant circuits based on operational amplifiers:

- MAIN_PWR, SPARE_PWR: voltage proportional to the output of primary DC/DC converter, main (spare) side;
- TEMP1, TEMP2: temperatures measured through PT1000 sensors placed on the electronics crate (TEMP1) and on the detectors structure (TEMP2);
- INT_STATUS_ERROR: 3-level internal status error signal (no error, generic operation failure, critical switch-on failure).

The TC circuit (detailed in figure 7) processes two groups of input signals from the satellite:

- MAIN_ON, SPARE_ON and OFF, for switching-on/off the main and spare sides of HEPD-02;
- STAND_BY_ON, STAND_BY_OFF and RESET, to manage energy saving state and forced reset of the instrument.

2025 JINST 20 P06005

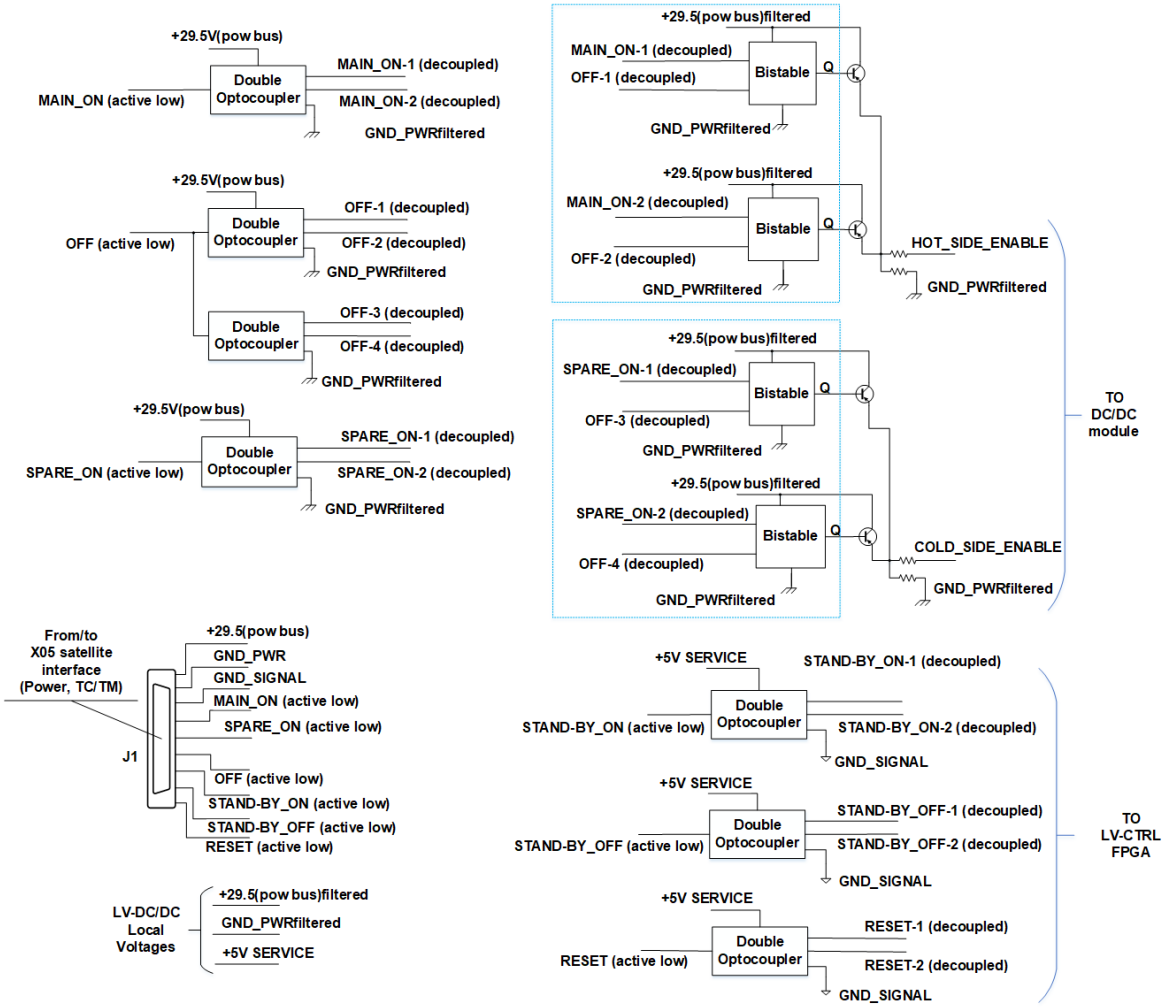

Figure 7. The TC circuit architecture.

The interface includes an optical decoupling stage of the signals coming from the satellite, in order to comply with the requirement of maximum decoupling of satellite power bus from internal circuits. For the first signal group, a digital logic stage follows, made with discrete components (mainly MOSFET), for latching the impulsive input signals and invert them to properly drive the primary DC/DC voltage converter. For the second group, the signals are sent to the LV-CTRL board to be processed by the FPGA. Both the decoupling and latching stages are redundant, with output signals logically ORed.

3.2 LV-CTRL board

The LV-CTRL board architecture is represented as a block diagram in figure 8.

Through direct interconnections with the LV-DCDC board, it receives the 12 V primary power and three TCs (STAND_BY_ON, STAND_BY_OFF and RESET) and sends back the TM signal INT_STATUS_ERROR. The hot and cold areas contain the circuits for unit control, communication with DPCU and distribution of power locally and to main/spare sub-systems. The common area implements the circuits for voltage conversion and distribution towards DIR (direction detector) with

2025 JINST 20 P06005

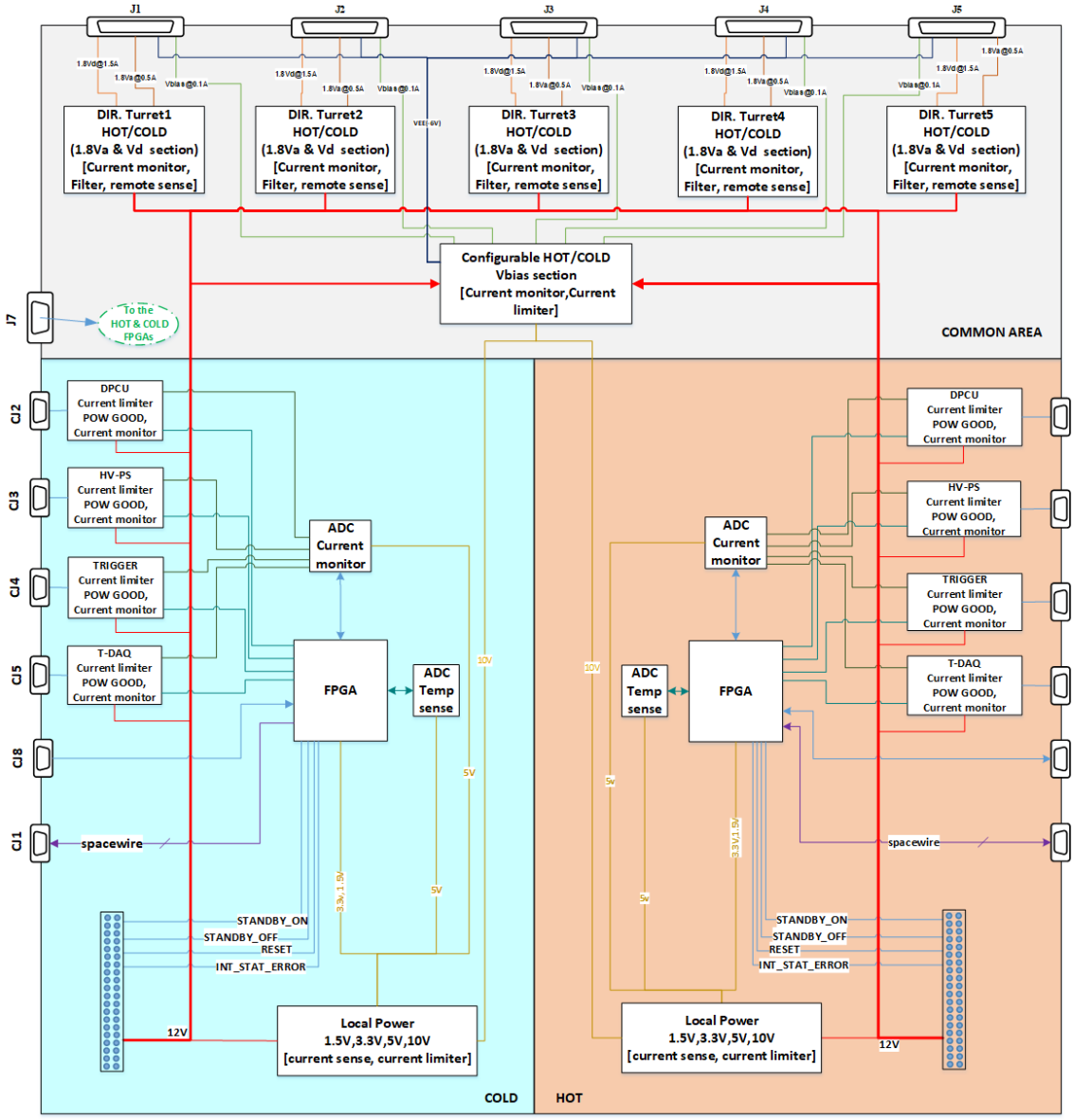

Figure 8. LV-CTRL board architecture.

one independent section for each of the five turrets. All branches of the power supply tree include fault protection, current sense, voltage and current sampling.

The control and communication functionality is implemented on an FPGA (ProAsic A3P600) with ancillary circuits necessary for correct operation and interfacing: a 48 MHz oscillator (ABRACON ASAAIG) as main clock signal, a power-on reset circuit (made with discrete components) to guarantee a clean start of the logics, a watchdog timer (Texas Instruments TPL5010) to assure automatic recovery of instrument operation in case of faults. The communication lines with DPCU are implemented according to the LVDS standard, employing the transceivers (Texas Instruments SN65LVDS31 and SN65LVDS32) which demonstrated excellent reliability on HEPD-01.

The logic structure implemented on LV-CTRL FPGA is shown as a block diagram in figure 9. The main functionalities are here listed and further detailed in the rest of the section:

2025 JINST 20 P06005

- slow control communication with DPCU, via full-duplex SpaceWire Lite interface (register file access) and additional single signals (RESET, SW_ERROR);
- UART debug interface (register file access);
- managing of initial power sequence and DPCU board start-up;
- watchdog timer control and emergency instrument power-down;
- SPI interface towards on-board ADCs for 1 Hz sampling of voltages, currents and temperatures;
- enabling of supply outputs to sub-systems and status monitoring of current limiters.

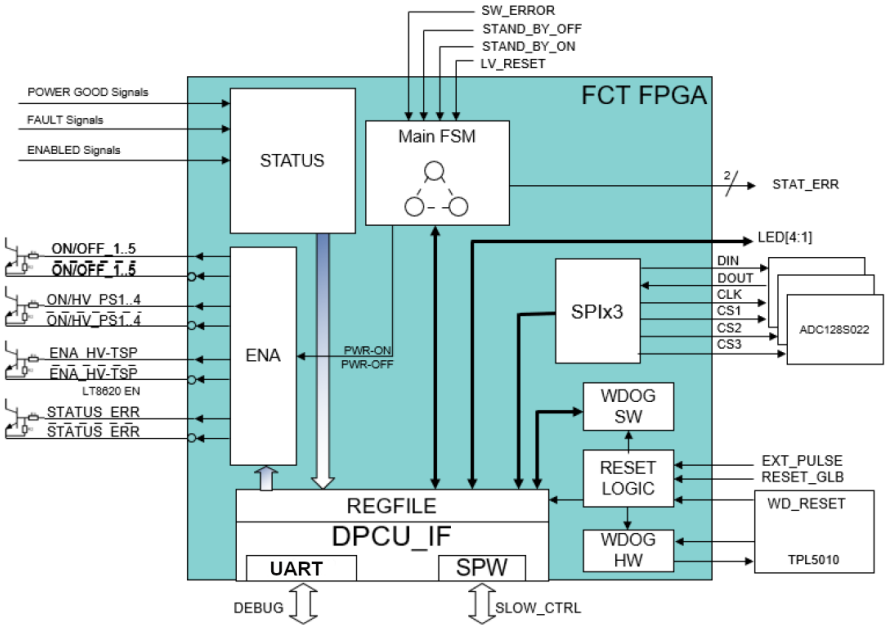

Figure 9. The LV-CTRL FPGA logic structure.

The SpaceWire Lite interface block allows the DPCU to read and write on the FPGA register file and thus control operation of LV-CTRL. The data/strobe coding and traffic management layer was implemented through the open-source licensed SpaceWire Lite core, already successfully used on HEPD-01. An additional block of code was created to implement the operations of writing, reading and burst reading on register file.

To allow debugging and characterization of operations on LV-PS, during development phases and even in the absence of the DPCU, a UART core was integrated and interfaced with the register file.

The LV-CTRL FPGA manages the initial power sequence when the 29.5 V satellite power bus is switched-on: after a predefined delay, it enables the power supply of DPCU and waits for DPCU to properly confirm its alive status, by writing on register file within the expected time interval. In the event of DPCU failing to do so, the switch-on sequence is repeated for a maximum number of times and, if not working, a critical error is indicated to the satellite by activating the INT_STATUS_ERROR wired TM.

After successful DPCU start-up, the watchdog timer is allowed to operate and expected to be reset by the DPCU every 5 s; in the event of DPCU failing to do so, the LV-CTRL FPGA manages

2025 JINST 20 P06005

a safe power-down of the whole instrument. Similarly, a controlled power-down of the instrument is operated following the detection of an anomaly or fault that cannot be directly controlled by the DPCU (for example, a persistent fault situation of the SpaceWire link).

3.2.1 Primary power distribution

As regards the controlled power distribution of primary 12 V supply to sub-systems, four architecturally identical sections were implemented respectively for DPCU, Trigger board, TDAQ and HV-PS unit, each one with specifically tuned design parameters. Each section (figure 10) features fault protection and current sense circuit.

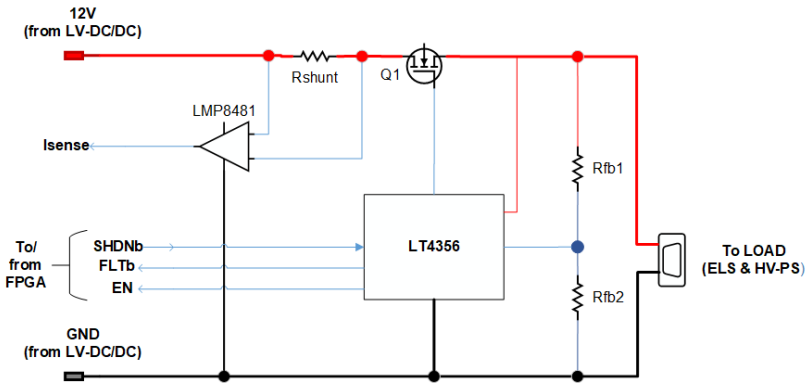

Figure 10. Block scheme of a primary power distribution section.

The fault protection circuit is based on the Linear Technology LT4356 current limiter: in case of input overvoltage or load overcurrent conditions, the LT4356 intervenes by opening the power MOS switch (Q1) and signalling the anomalous condition to the FPGA through a dedicated line (FLTb). An additional line (EN) allows to determine whether the fault condition is accompanied by a short-circut at the load. In turn the FPGA can react with a forced shutdown of the power section, by activating the corrisponding signal (SHDNb). The overcurrent fault thresholds for each of the four loads were set by taking into account the maximum possible absorption across the full operating voltage and temperature range.

The current sense circuit implements a shunt measurement with a precision current sense amplifier (Texas Instruments LMP8481), whose output is periodically sampled by an ADC (Texas Instruments ADC128S022).

The power for the LV-CTRL itself is generated from the primary 12 V supply, through two voltage conversion branches, as shown in figure 11: the upper branch generates 3.3 V and 1.5 V supplies, required by the FPGA I/Os and core respectively, while the lower branch generates 10 V and 5 V supplies, respectively for service (current sense amplifiers) and ADC circuits.

Each branch features a load fault protection and current sense circuit, designed as previously described (see figure 10). For the upper branch, this is followed by a voltage converter stage implemented with DC/DC converters, in order to minimize conversion losses. For the lower branch, given the low current absorption and the need to keep the power supply as clean as possible, the voltage conversion is implemented through low-dropout linear regulators (LDO).

2025 JINST 20 P06005

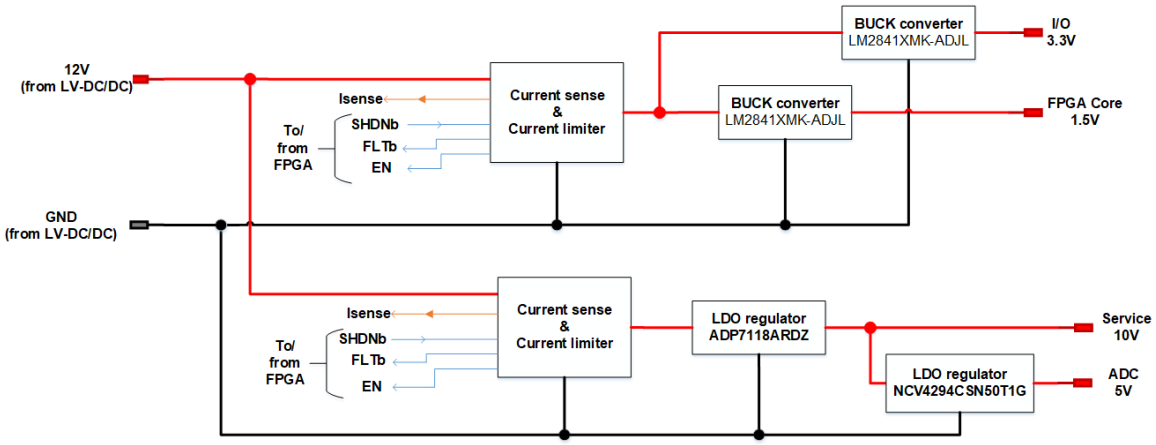

Figure 11. The LV-CTRL local power distribution.

3.2.2 Power distribution towards DIR

The power distribution for the five DIR turrets is obtained with redundant circuits implementing a configurable bias voltage source and five independent sections delivering 1.8 V supply for analog and digital turret electronics, starting from the 12 V primary voltage.

The bias voltage source (figure 12) is designed as the cascade of a fault protection and current sense circuit (same as shown in figure 10), a ±6 V supply generator and five independent bias generators with three selectable output values (−3 V, −1 V, −100 mV), obtained with a weighted voltage divider controlled by FPGA; the generators are made with discrete components, with the bias output stage formed by an operational amplifier followed by a first order low-pass filter.

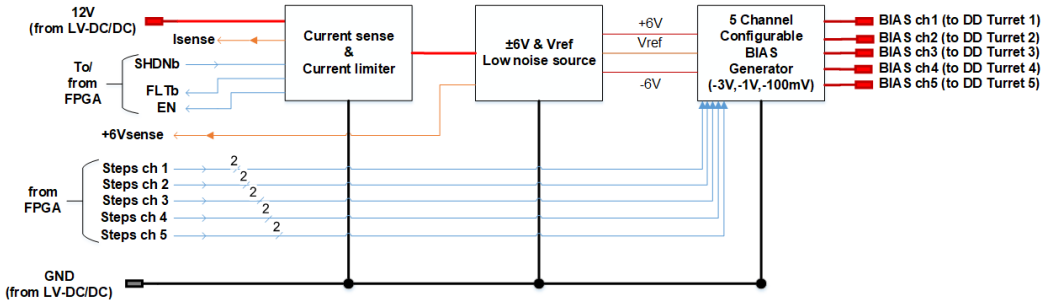

Figure 12. Architecture of the configurable hot (or cold) bias voltage source for DIR turrets.

The 1.8 V power supplies for digital and analog turret electronics are generated from a single DC/DC converter (figure 13); the analog line is obtained through a filter placed at the output of the DC/DC converter, in order to remove spurious harmonics and reject the common mode. The current is monitored by a sense amplifier sampled by ADC. In order to obtain a voltage as stable as possible locally at the DIR turret, a sense voltage circuit was implemented, working on a feedback line from the turret and compensating the effects of drops along the cable and absorption transients during times compatible with the circuit bandwidth. The unique feedback signal is shared by the hot and cold circuits through SPDT switches appropriately driven to isolate the currently active side (e.g. hot) from the powered-off one (e.g. cold).

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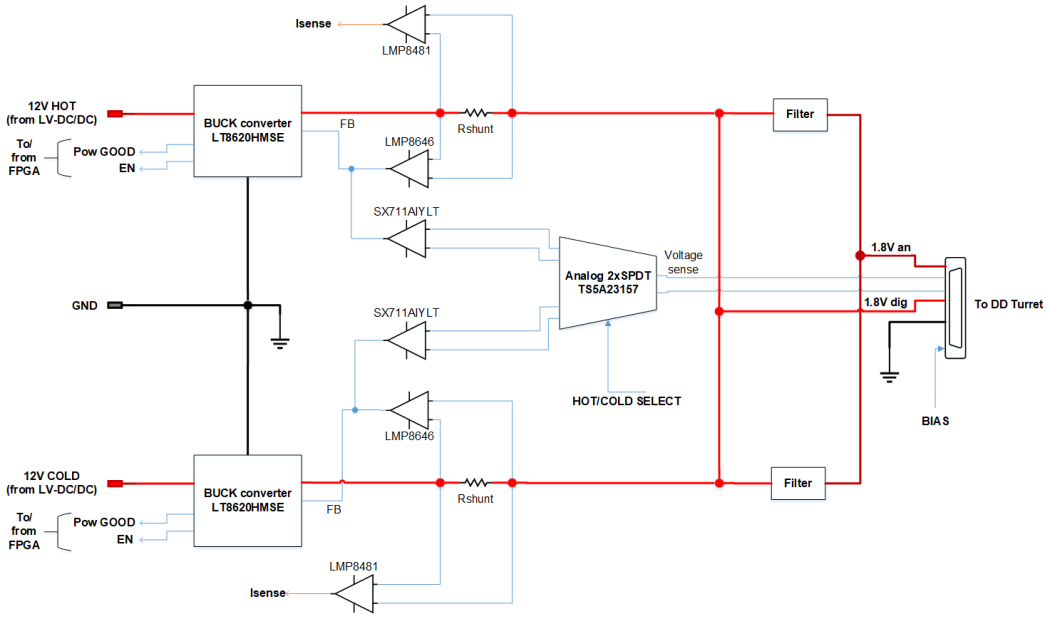

Figure 13. The redundant architecture delivering 1.8 V digital and analog power to a DIR turret.

4 High-voltage power supply

The high-voltage power supply unit (HV-PS, see figure 14) consists of a compact and stiff mechanical assembly with 16 hot/cold redundant "high-voltage DC/DC" (HV-DCDC) boards, delivering negative bias voltages up to 1000 V to the 64 PMTs which constitute the read-out of HEPD-02 scintillators. The unit is managed by a slow control section housed on a dedicated "HV control" (HV-CTRL) board with redundant circuits.

The HV-PS internal power distribution tree is housed on the HV-CTRL board, where the primary 12 V supply enters two branches: a 3.5 V DC/DC converter, followed by a set of low-dropout linear regulators, delivering low voltages towards the on-board circuits; a pair of linearly regulated 11.5 V supplies, each one supplying 8 of the 16 HV-DCDCs.

The HV-DCDC board (Aerospazio Tecnologie HV3) is a regulated high-voltage supply, capable of 1200 V output (either sign) and sustaining up to 500 µA output current, featuring very low ripple and noise (15 mV peak-to-peak), wide operating temperature range, low non-linearity ($\leq 0.5\%$) and temperature drift (≤ 100 ppm/°C). Its design is optimized for space applications and high-reliability, with very low internal power consumption (360 mW at maximum voltage), very compact size (7 cm × 5 cm × 2 cm), light weight (80 g) and circuit parts characterized by high radiation resistance. It has been tested at prototype level up to 30 krad total ionizing dose, without reporting any significant performance degradation. The board is equipped with a low-voltage monitoring output proportional to the HV level and with a foldback current limiter, capable of automatic restoration of normal operation in case of transient overcurrent conditions.

Each pair of hot/cold redundant HV-DCDC boards have their outputs short-circuited on a dedicated "HV splitter" (HSP) board, thus producing a single line that is distributed to a group of PMTs with similar gain and reading the same type of scintillator detector, therefore able to receive the same bias voltage. Given the different number of PMTs for each type of detector (TR1, TR2, RAN, EN, LAT

2025 JINST 20 P06005

and BOT), the number of PMTs in each bias group varies from 2 to 6. Series diodes on the hot and cold HV outputs allow to isolate the corresponding HV-DCDC circuitry when off.

The present design constitutes an evolution and improvement with respect to the HV-PS unit of HEPD-01 (described in [10]), with the numeric increase of HV-DCDCs (from 12 to 16), the introduction of HSP boards to implement hot/cold HV short-circuit directly inside the unit, a significantly better power efficiency, obtained with newly designed circuits matching the primary 12 V supply available in HEPD-02.

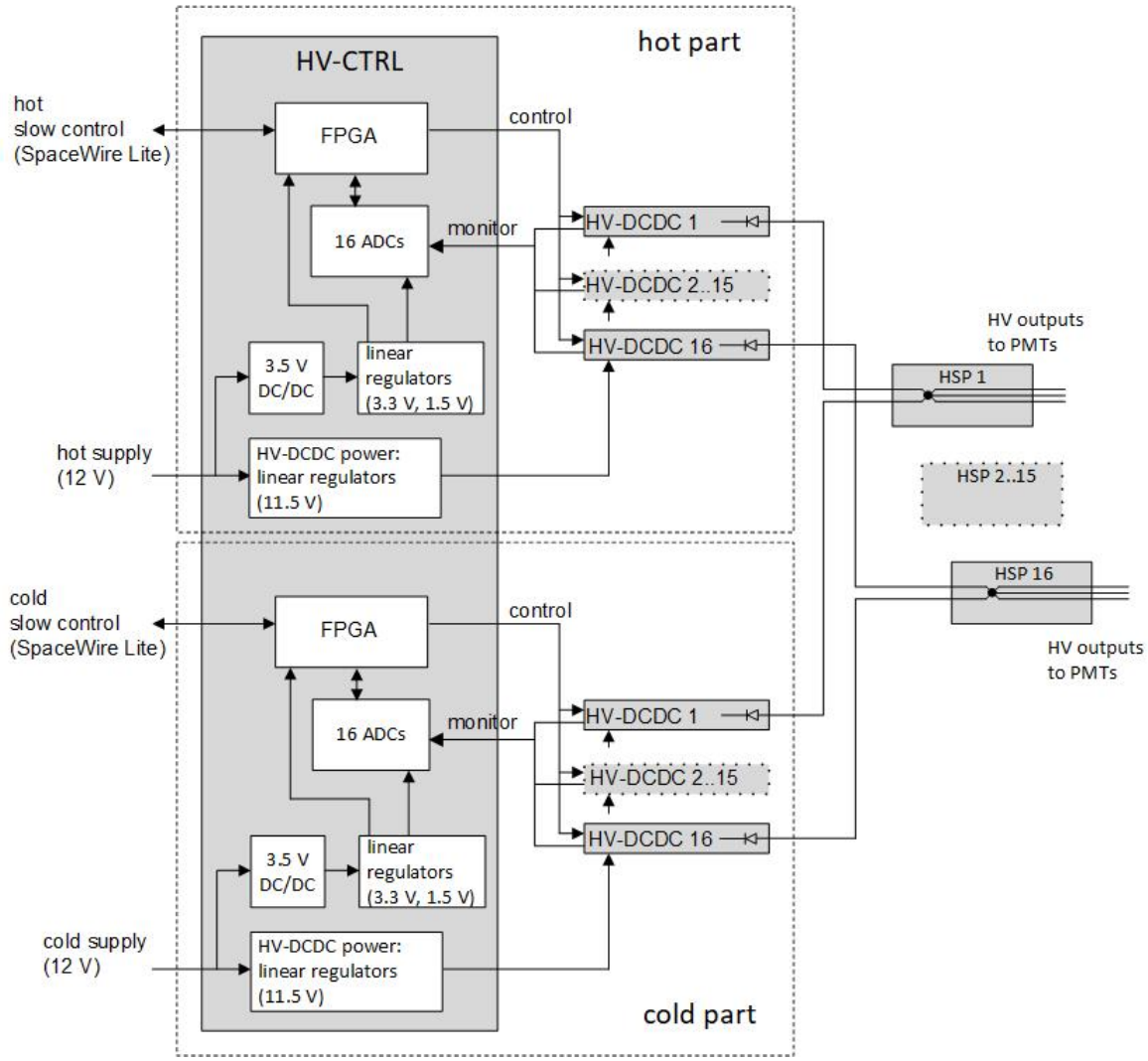

Figure 14. Block diagram of HV-PS unit.

4.1 HV-PS mechanical structure

The HV-PS mechanical structure (see figures 15 and 16) is based on a single-piece aluminium-alloy frame. The 32 HV-DCDCs are positioned along 4 columns, each board housed in a dedicated cavity of the frame, while the HV-CTRL board covers the whole rear face of the unit. The object was designed to fit in the small available volume (29.8 cm × 24.3 cm × 5.6 cm) within the electronics section of

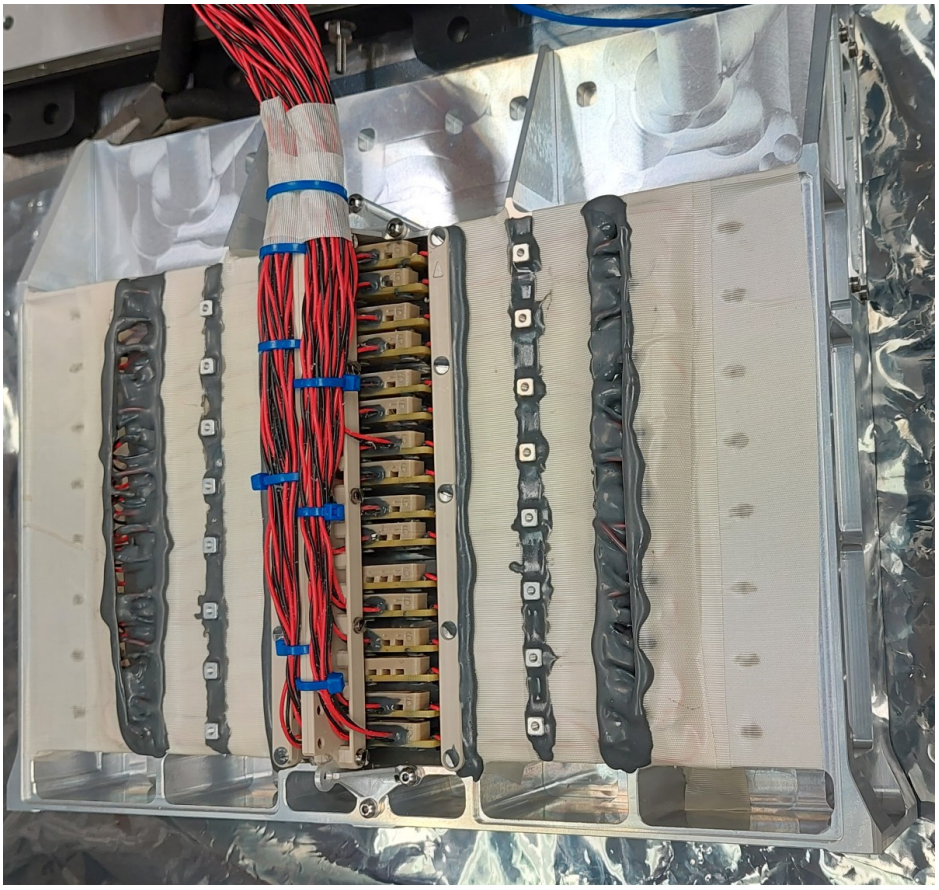

Figure 15. Front view of the HV-PS unit during integration on HEPD-02 system. The central column of 16 HSP boards is visible, with a total of 64 pairs of wires delivering HV to the PMTs. The overall dimensions are 29.8 cm × 24.3 cm × 5.6 cm.

the apparatus. Such configuration implied a tightly packed assembly of the various boards and their interconnections, which required an extensive study to obtain a feasible and reliable assembly procedure.

The compact HV-DCDC board geometry implies relatively short distances between high-voltage and low-voltage parts (including the mechanical frame); to guarantee a sufficiently high dielectric strength, also in the vacuum conditions foreseen during orbital flight (pressure < 6.65 mPa), each HV-DCDC cavity is filled with encapsulant (Dow Corning SE 1819 CV). The effectiveness of the encapsulant strongly depends on the correct technique used to fill the housing. Therefore extreme care was taken to avoid significant entrapment of air bubbles during pouring of the liquid encapsulant, especially along the external surfaces of PCB and mounted parts. In fact any residual trapped air, together with outgassing from adjacent materials, may form paths of low dielectric strength; additionally, in a low-pressure environment trapped air bubbles may explode by breaking the solidified encapsulant. The correctness of the encapsulation procedure was verified by testing the HV-PS unit operation in vacuum condition. In particular, the absence of any electric discharge between high and low-voltage parts was verified with a sensitivity of 1 V pulse amplitude, superimposed on the static value (~ 1000 V).

The connection between HV-CTRL and each HV-DCDC is implemented through a flat cable, with wires directly soldered on pads at each end. This solution avoids the use of connectors, which

2025 JINST 20 P06005

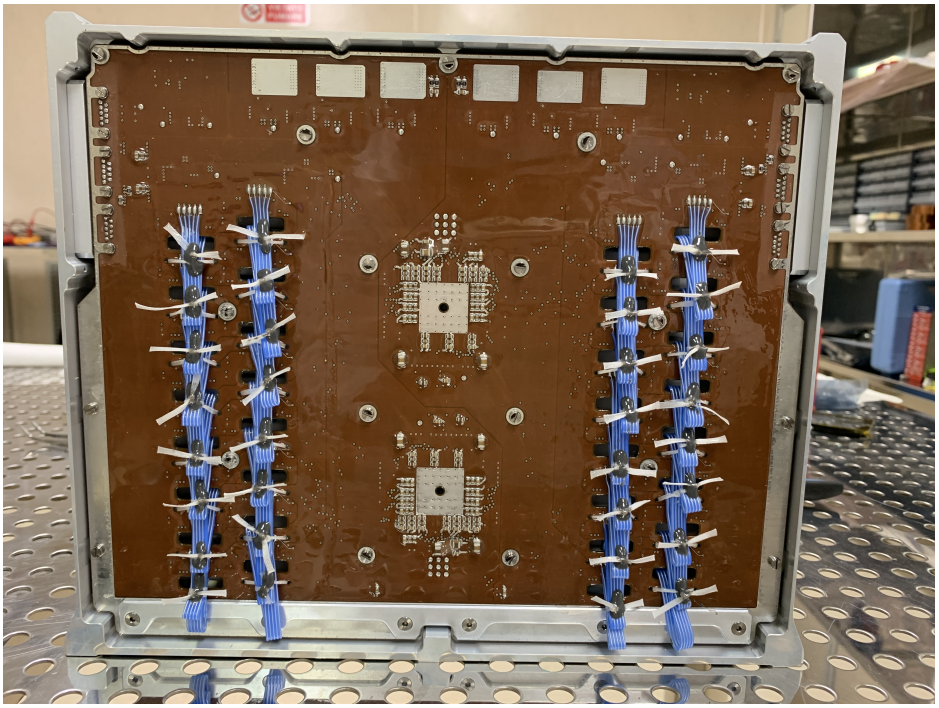

Figure 16. Rear view of the HV-PS unit, with the HV-CTRL board fully visible and covering the 32 HV-DCDCs, connected by means of flat cables passing through open slots of the HV-CTRL PCB.

are not compatible with the extremely small volumes available. The flat cable routing was studied in such a way to avoid mechanical stresses on the soldering point at each end, due to vibrations of the structure. On the HV-CTRL end, the cable is shaped into a full loop for stress relief of soldering points; a dedicated open slot in the PCB (see figure 16) allows the cable to be routed towards the underlying HV-DCDC, where it is incorporated in the solidified encapsulant.

The HV lines towards PMTs are implemented through unshielded twisted-pair wires, as a compromise between low interference pick-up and low volume occupancy. The employed FEP-insulated wire (Daburn 2475/28) was specifically selected as being compact, highly flexible and not containing ferromagnetic material (as required for use in CSES satellites).

The HV-CTRL board insulator is polyimide, while the high-voltage boards (HV-DCDC and HSP) are built with FR4 glass-reinforced epoxy laminate, characterized by higher dielectric strength and allowing a more compact design. Additionally, FR4 superficial dielectric strength is less prone to deteriorate, thanks to the higher material porosity, which implies a better absorption of impurities such as cleaning agents used in soldering operations.

The HV-CTRL and HSP board surfaces are protected with low-volatility room-temperature vulcanizing (RTV) silicone conformal coating (NuSil CV-1152), having a thickness chosen in compliance with the IPC A-610 standard.

4.2 HV-PS operation

The HV-PS operation is managed on the HV-CTRL board by an FPGA (ProASIC A3PE600) configured as synchronous machine, clocked by a 48 MHz oscillator (IQD CFPS-73 series).

2025 JINST 20 P06005

The main implemented functionalities are listed below:

- individually switch-on/off and set the high voltage on each DC/DC;
- digitize the analog monitor voltage delivered by each HV-DCDC, which is proportional to the HV level;
- read-out two on-board temperature sensors;
- interface with HEPD-02 DPCU by means of full-duplex SpaceWire Lite protocol through LVDS transceivers.

After power-on and whenever necessary, the HEPD-02 DPCU sends an initialization command sequence, in such a way to set-up the HV outputs to the desired values; these may vary according to the required instrument configuration, or because of detector and electronics aging with subsequent gain or threshold changes in the PMT signal processing line.

The DPCU periodically checks for the correct operation of HV-PS unit, by reading the content of HV-CTRL registers dedicated to monitored HV values, temperature sensors data and other status information. If any of these variables turns out to be outside of the acceptable range, the DPCU starts appropriate automatic recovery procedures, including forced initializations and power-off/on cycles of HV-PS, for a maximum number of attempts.

The HV-CTRL FPGA is configured to perform automatic setting of HV outputs at default values as response to power-on, if no initialization command is received after a fixed waiting time. This feature allows instrument operation with acceptable HV values, even in the unlikely event of permanent loss of communication with the DPCU.

The HV-CTRL FPGA drives the HV-DCDC analog voltage setting input by generating a square wave, whose duty cycle is configured according to the digital value stored in a 10-bit register; the square wave is converted into a voltage level proportional to the duty cycle through an RC low-pass filter. This method maximizes the linearity of the voltage level delivered at the HV-DCDC analog input.

The high linearity, together with the limited fabrication tolerances of both HV-DCDC boards and voltage setting driver circuits, allow to characterize the dependence of any HV channel from the 10-bit digital value, with a unique linear function and ±3% maximum discrepancy.

The correctness of the effectively generated high voltage is fundamental; therefore, each 10-bit setting register is protected by an Error Detection And Correction (EDAC) function, with automatic correction of single bit upset and detection of double bit upset, by means of Hamming logics. A single bit upset is corrected within a clock cycle (~ 20 ns), with no significant effect on the corresponding voltage, given the RC delays of the line. On the other hand, if a double bit upset is detected, the register is immediately reset to zero and the error condition written in the HV-CTRL status information, thus causing the DPCU to react with commands to restore the proper voltage. However, given the radiation intensities foreseen during orbital operation and the FPGA radiation hardness (see section 2), the probability of double upset on a single register is negligible during the expected mission duration (6 years).

As a further safety measure, the analog monitor voltage of each HV-DCDC is periodically sampled by ADC on the HV-CTRL board and compared with a fixed threshold of 10% of full scale; a corresponding alarm bit is set to 1 for an under-threshold value, which may indicate a short-circuit condition and, therefore, a collapse of high voltage.

2025 JINST 20 P06005

5 Conclusions

Two sets of fully functional LV-PS and HV-PS units were assembled and their operation was verified by extensive electrical and functional tests in a broad temperature range (from −20°C to 50°C), employing a DPCU emulator for digital interface and resistive loads to emulate the connections of LV and HV outputs to HEPD-02 sub-systems and PMTs, respectively. Additionally, the HV-PS unit was tested in vacuum conditions to verify the absence of any electric discharge between high and low-voltage parts, as discussed in section 4.1.

The main characteristics of LV-PS and HV-PS of HEPD-02 are reported in table 1 and table 2 respectively, where they are compared with those of the corresponding units of HEPD-01.

Table 1. Comparison of LV-PS units in HEPD-01 and HEPD-02.

		LV-PS	
		HEPD-01	HEPD-02
Volume (cm^3)		2926	2897
Mass (kg)		1.9	1.6
Efficiency	Primary DC/DCs	80%	85%
	Secondary DC/DCs	77%	90%
Output voltages	To HV-PS	3.6 V, 5.6 V, 12 V	12 V
	To DIR	3.6 V, 1.8 V, −2 V	1.8 V (an.), 1.8 V (dig.), −3 V (bias)
	To other boards	3.6 V, 5 V, 5.6 V	12 V
Housekeeping	Protection	Current limiter for each line	Current limiter for each line
	Monitored parameters	—	Temperature in warmest and coldest PCB zone
		—	Value of current for each line
		—	Value of voltage for selected lines
		—	Fault flag for each line

The first set of LV-PS and HV-PS units was integrated into the HEPD-02 Qualification Model (QM), while the second set was mounted in the Flight Model (FM). Both the HEPD-02 QM and FM underwent successful test campaigns for overall instrument qualification and acceptance, respectively, including vibration tests, thermal cycles both in air and vacuum, electromagnetic compatibility tests for emission and susceptibility, according to the requirements for operation on-board CSES-02 satellite, as discussed in section 2. The HEPD-02 FM was finally delivered to the CSES-02 satellite assembly and test facility, in Beijing (China), in January 2024.

2025 JINST 20 P06005

Table 2. Comparison of HV-PS units in HEPD-01 and HEPD-02.

		HV-PS	
		HEPD-01	HEPD-02
Volume (cm^3)		3356	4055
Mass (kg)		3.2	3.7
Efficiency	3.5 V DC/DC	—	90%
	12 V regulator	80%	90%
Output voltages	PMTs	1.2 kV (12 lines)	1.0 kV (16 lines)
	DIR	150 V	—
Housekeeping	Protection	Current limiter for each line	Current limiter for each line
	Monitored parameters	—	Temperature in warmest and coldest PCB zone
		Value of voltage for each output line	Value of voltage for each output line

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