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Free-Standing 3C-SiC P-Type Doping by Al Ion Implantation

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Abstract. Free standing wafers of the cubic polytype of silicon carbide (3C-SiC) grown on micromachined silicon substrates can be a platform for new power electronic devices, provided that suitable device fabrication processes are understood and optimized. In this frame, p-type doping is still an open issue, as results on the electrical activation of ion implanted Al in 3C-SiC are limited. This work analyses high level p-type doping with post-implantation annealing carried out at temperatures in the range 1650-1850 °C with different durations. A coherent picture emerges, showing that the resulting resistivity in 3C-SiC Al-implanted layers is higher than the one obtained in 4H-SiC implanted layers, the result being ascribed to low carrier mobility and possibly presence of compensation centers, rather than to poor Al electrical activation. The reported results highlight the importance of working on material and processing optimization.

Introduction

The fabrication of good quality free standing 3C-SiC wafers is opening the way to the fabrication of several types of devices: p+/n diodes [1], MOS [2], MEMS and bio-based devices. Though the material quality is still subject to improvement, preliminary studies on 3C-SiC processing can be made. Up to now, p-type doping has been studied on heteroepitaxial layers grown on silicon, where the post-implantation annealing temperature is limited by the Si substrate melting temperature. At T<1400 °C the required duration to achieve an, although weak, electrical activation of the Al dopants lies in the range of hundreds of hours, with the additional drawback of having the defect conduction contribution comparable to the Al dopant contribution [3]. Free standing 3C-SiC [4,5] gives the double advantage of extending the range of the post-implantation annealing temperature and reducing the annealing duration to industrially feasible times. This material improvement has led to the fabrication of p+/n diodes where the emitter is a 350 nm deep 1×10^{20} cm^{-3} Al-implanted box profile, annealed at 1700 °C for 2h. Sheet resistances ranging between 2500 Ω and 15000 Ω are reported for such layers [1]. However, an analysis of the Al electrical activation at comparably high temperatures is not reported in literature yet.

This work focuses on p-type doping of 3C-SiC material after 1×10^{20} cm^{-3} Al ion implantation followed by annealing at temperatures in the range 1650 °C - 1800 °C with different durations. We report on the surface morphology and electrical conduction achieved by annealing the samples either under a C-cap or with the bare surface.

Experimental

The material employed in this experiment is a 95 μm thick 3C-SiC wafer 4° off-axis. The surface was not polished before processing due to its extreme fragility. For this reason, the front side is featured by tilted pyramids of irregular size as shown in Figs. 1(a,b). As their height is not higher than 2 μm, these features are not a problem for photolithography, provided that the photoresist is thick enough to cover the whole pyramid height. Al ion implantation was performed at 600 °C to a concentration of approximately 1×10^{20} cm^{-3} to achieve a 200 nm box profile below the surface. The post implantation annealing was carried out in Ar atmosphere at temperatures in the range 1650-1800 °C for different durations. The majority of samples was annealed with the surface covered by a C-cap obtained by pyrolysis of HPR photoresist. After annealing the C-cap was removed through 850 °C oxidation. Two samples were annealed at 1750 °C and 1850 °C with no capping. Circular TLM structures (C-TLM) were produced with ohmic contacts made by Ti, Al, and Ni-based alloys. Table 1 resumes the sample process parameters as well as the measured resistivity.

Table 1. Experimental conditions (annealing temperature, time, and contact formation parameters) and sheet resistance obtained by C-TLM measurements.

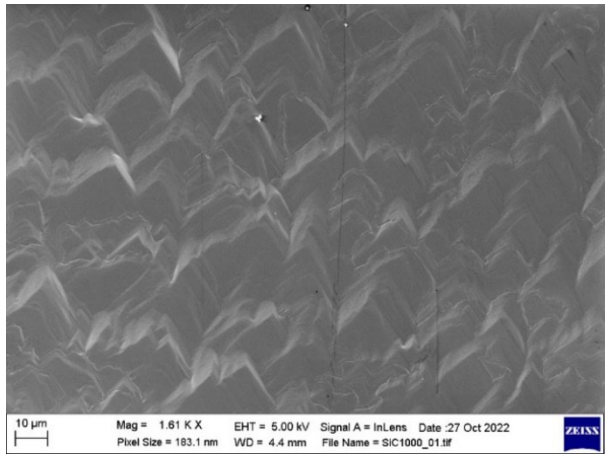
T annealing [°C]	time [min]	Metal stack [nm]	T alloy [°C]	time [min]	R_{sh} [kΩ/□]
1650	30	(Ti/Al)/Ni 35/45	1050	5	350±200
1650	120	(Ti/Al)Ni 60/50	1100	5	102±19
1700	30	(Ti/Al) 45	1100	5	180±60
1700	120	(Ti/Al)/Ni 60/50	1100	5	45±4
1800	30	(Ti/Al)Ni 60/50	1100	5	81±7
1800	120	(Ti/Al)/Ni 60/50	1100	5	29±6

The surface morphology was characterized by a LEO 1530 Scanning Electron Microscope and a Smart WLI optical profilometer equipped with 10×, 50× and 100× magnification objectives [6].

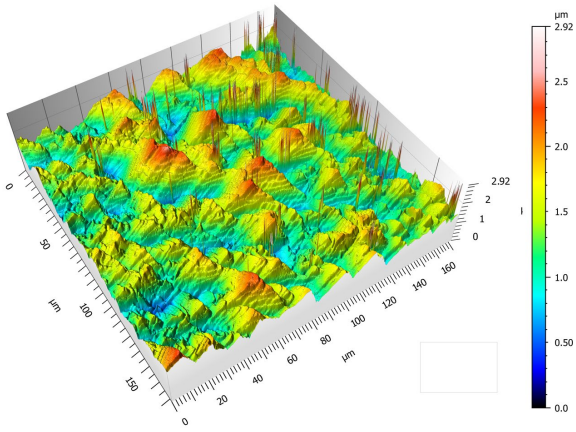
Secondary Ion Mass Spectroscopy (SIMS) and Electrochemical Capacitance Voltage (ECV) profiles were acquired by PROBION Analysis.

Results and Discussion

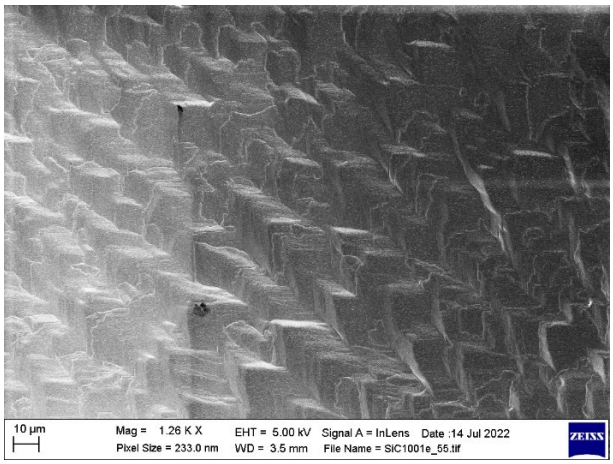
The surface morphology was characterized by SEM and optical profilometer. Figs. 1(a,b) show the as-grown surface, which was not polished due to the wafer brittleness: the surface shows the surface step bunching due to the bulk growth. Fig. 1b shows that surface height distribution lies in an interval of 3 μm amplitude, whereas the pyramid height is not higher than 2 μm. The initial presence of pyramids and steps might question the effective need for a capping to prevent surface roughness during annealing. Fig. 1(c-f) show the SEM micrograph and the surface height profile of a sample annealed at 1800 °C 2h with a C-cap (c,d) and a sample annealed at 1850 °C 30 min with no capping (e,f). While the capped sample preserves the pyramid surface, the sample annealed with no capping shows many rectangular holes on the pyramid faces, due to anisotropic evaporation. The contrast of the SEM image shown in Fig. 1e is mainly due to these features (enlarged in the inset), so that the surface texturing, that is still present, as shown in Fig. 1f, looks almost unrecognizable. It must also be remarked that the surface of the uncapped sample gave poor metal adhesion and prevented the lift-off photolithographic processing. For this reason, no electrical information was drawn for this process.



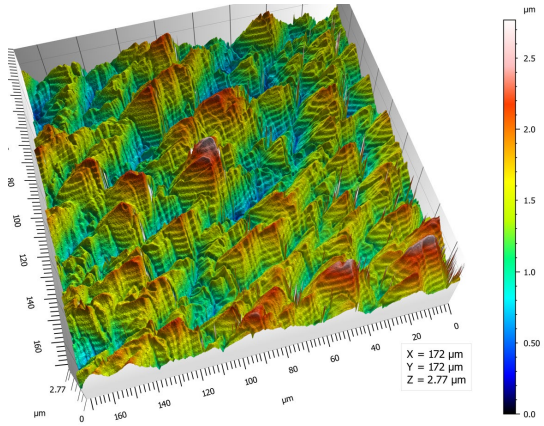
(a)



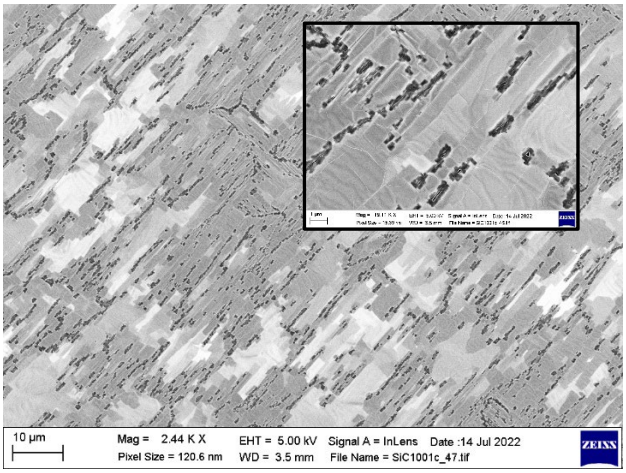
(b)



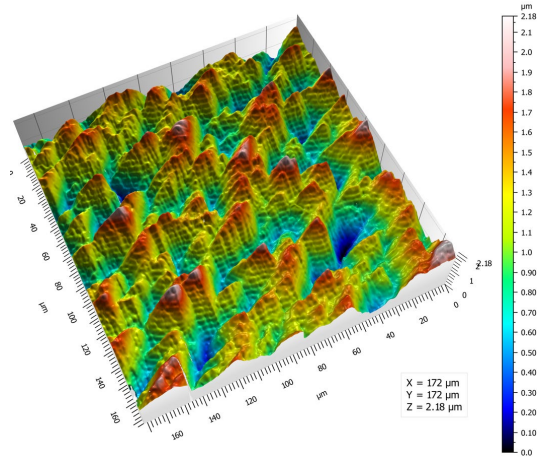
(c)



(d)



(e)



(f)

Fig. 1. SEM micrographs (a,c,e) and surface height profiles (b,d,f) of: the as grown material (a,b); a sample annealed at 1800 °C for 2h (c,d) with C-cap; and a sample annealed at 1850 °C 30 min without capping (e,f).

The remarkable difference observed between SEM micrograph in Fig. 1e and the optical profilometry in Fig. 1f is due to the specifics of the two techniques: SEM is sensitive to edges, while the optical profilometer highlights height variation; light reflection from pronounced edges, vertical walls, and holes hardly reaches the detector. Thus, the sole use of one of the two techniques might give misleading information; on the contrary, the combined use of SEM and optical profilometer provides both quantitative and qualitative information on the surface evolution along processing

steps, and allows for overcoming the drawbacks in using AFM on this kind of surfaces. Indeed, the high surface roughness exhibited by the wafer might give rise to very noisy AFM images, which, together with the limited scan size, induces the possibility of rms roughness underestimation. In this study, a quantitative determination of the surface rms along processing was not made because the pyramidal texturing accounts for the main contribution to the result. However, in analogy with the 4H- polytype [7], surface roughening under the C-cap occurs in 3C-SiC as well. Fig. 2 shows a detail of the surface after 1800 °C 2h annealing after C-cap removal and dip in diluted HF. This picture was taken on the same sample as the one shown in Fig. 1(c,d). Despite the different lattice symmetry (cubic vs hexagonal) and initial surface state (textured vs polished), at micrometric sizes the morphology of annealed 3C-SiC and 4H-SiC show remarkable similarities.

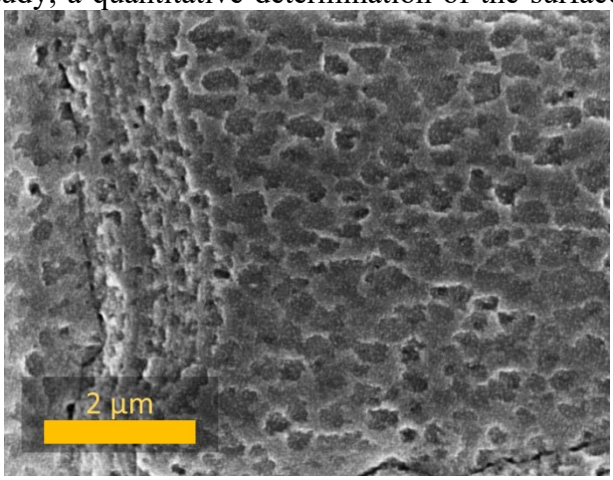


Fig. 2. SEM micrographs at high magnification of the surface annealed at 1800 °C 2 h after C-cap removal.

Fig. 3a reports the resistivity measured on the samples annealed under a C-cap for the two annealing durations 30 min and 2h. The Figure also reports the resistivity measured on 4H-SiC annealed in similar conditions [8] and the resistivity measured on a different free standing 3C-SiC wafer [1]. This graph shows that, for 3C-SiC, a prolongation of the annealing, even at temperatures as high as 1800 °C, is beneficial to the conductivity. The resistivity values obtained on 3C-SiC are systematically higher than in 4H-SiC. The measured values show also a variability dependent on the processed piece taken from the entire wafer. Fig. 3b shows the simulated as-implanted Al profile and the measured SIMS and ECV profiles in two samples annealed at 1700 °C 30 min and 2h. The SIMS profiles are in good agreement with the simulation. This is remarkable considered the high surface roughness of the 3C-SiC wafer. The ratio between integrals over the ECV and SIMS profiles yields an electrical activation equal to 35% and 47% for the samples annealed 30 min and 2h respectively.

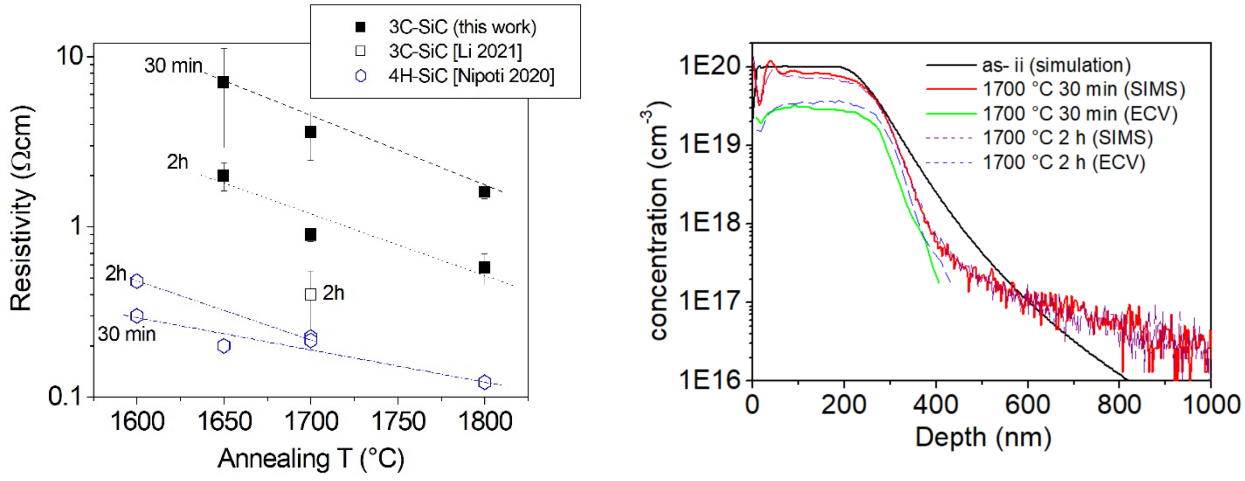


Fig. 3. (a) Sheet resistance values measured on circular TLM structures made on 3C-SiC as a function of the annealing temperature; literature values are reported for comparison. (b) Al dopant profiles obtained by Secondary Ion Mass Spectroscopy (SIMS) and Electrochemical Capacitance-Voltage (ECV) measurement for two annealing times (30 min and 2 h) at 1700 °C; the intended as-implanted Al profile calculated by SRIM simulations is also shown.

From the processing point of view, at 1700 °C, a prolongation of the annealing improves both the Al electrical activation and the conduction. While the electrical activation increases by a factor 1.3, the resistivity measured after 2h annealing at 1700 °C (Fig. 3a) is about three times lower than after 30 min: this implies also a major improvement in mobility over the annealing time, under the hypothesis that the decrease in compensation is of the same order of magnitude as the increase in dopant activation [9]. The trend exhibited by the resistivity, that is similar at all the investigated annealing temperatures, induces a generalization of this concept.

It is worth to notice that the Al activation in 3C-SiC measured by ECV (Fig. 3b) is close to the activation extracted from fitting of Hall effect measurements in 4H-SiC, that ranges between 39% at 1675 °C and 48% at 1775 °C [10]: this difference does not justify the systematically higher resistivity of the 3C-SiC implanted layers with respect to 4H-SiC, observed in Fig. 3a. It might be inferred that the high resistivity in 3C-SiC is due both to low carrier mobility and compensation or trapping at defects. A discrimination between the two factors is not possible since this study has been carried out on C-TLM structures. However, the C-TLM analysis has the advantage of giving information also on the contact resistance. All the analyzed contact schemes (see Table 1) are ohmic, but an extreme variability in contact resistivity is observed: in every sample, except the one annealed at 1800 °C 2h, the contact resistivity ranged between the 10^{-6} Ωcm and the 10^{-2} Ωcm decades. Only the sample annealed at 1800 °C 2h showed more uniform contact resistivity values between 10^{-5} Ωcm and the 10^{-4} Ωcm. This very good result is worth further investigation and, possibly verification of repeatability.

Conclusions

This work provides an analysis of 3C-SiC p-type doping processes. The morphological analysis confirms the need for surface capping during annealing even in presence of pronounced initial surface roughness. Indeed, annealing without C-cap produces anisotropic evaporation from the surface, whereas the use of a C-cap produces a microscale morphology similar to the 4H-SiC case. From the electrical point of view, the resistivity of 3C-SiC Al-implanted layers is far higher than the one of comparable 4H-SiC layers, regardless of the Al electrical activation, that is similar in the two polytypes. This result points out, once more, the importance of good wafer quality in device functionality. An improvement of the wafer conductivity is observed by increasing the annealing duration from 30 min to 2h. A prolongation of the annealing beyond the times analyzed in this work might further improve this result. The highest annealing thermal budget produces resistivities as low as 10^{-5} Ωcm with a Ti/Al/Ni contact alloy. All the presented results show the value of further optimizing 3C-SiC material growth and processing.

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