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Anomalous Electrical Behavior of 4H-SiC Schottky Diodes in Presence of Stacking Faults

Marilena Vivona[1,a*], Patrick Fiorenza[1,b], Viviana Scuderi[1,c], Francesco La Via[1,d], Filippo Giannazzo[1,e] and Fabrizio Roccaforte[1,f]

[1]CNR-IMM, Strada VIII n.5, Zona Industriale, I-95121, Catania, Italy

[a*]marilena.vivona@imm.cnr.it, [b]patrick.fiorenza@imm.cnr.it, [c]viviana.scuderi@imm.cnr.it, [d]francesco.lavia@imm.cnr.it, [e]filippo.giannazzo@imm.cnr.it, [f]fabrizio.roccaforte@imm.cnr.it

*corresponding author

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Abstract. In this work, we investigated the impact of crystallographic defects (specifically stacking faults, SFs) on the mechanisms of the current transport in 4H-SiC Schottky contacts. The electrical characteristics were studied under both forward and reverse bias. In particular, while the presence of SFs under the contact did not show a significant impact on the forward characteristics of the Schottky diode, a significant increase in the leakage current occurred under reverse bias in defective diodes. This anomalous behavior can be explained by a space-charge limited current model, consistent with the presence of a trapping state distribution in the 4H-SiC gap. An increase of the reverse bias above 30 V leads to a complete trap filling. The weak temperature-dependence of the leakage current observed at highest voltage suggests that a tunneling of the carriers through the barrier can be also present.

Introduction

Owing to the good crystalline quality of the material and the current device processing maturity, 4H-SiC Schottky barrier diodes (SBDs) are today widely used in several applications [1,2]. However, in order to further optimize their performances, understanding the physics ruling the contact properties still remains a subject of intensive investigations [3,4]. In particular, the deviations from the ideal electrical behavior of the diode can be a signature of the presence of defects in the device active area, generated during either material growth or device fabrication. Hence, understanding the current transport in defective devices always deserves specific attention. In this context, while the effects of stacking faults (SFs) on the electrical behavior of p-n junctions have been extensively investigated in 4H-SiC [5], less work has been done in the case of SBDs, where debated results have been reported [6,7]. For instance, *Kojima et al.* reported that the presence of very few SFs in 4H-SiC epilayers causes a relevant increase of the reverse leakage current in Schottky diodes [6], whereas only a small reduction of the Schottky barrier height was observed by *Konishi et al.* in the presence of a significant amount of SFs under the anode of SDBs [9]. In other cases, even with the occurrence of a relevant reduction of the Schottky barrier (0.25 eV) under forward bias, no clear correlation with the leakage current is observed [9]. Hence, additional investigation is necessary to understand and quantitatively assess the impact of SFs. In particular, it is important to clarify their effects on the electrical current transport mechanisms in 4H-SiC Schottky diodes.

In the present work, we analyzed the anomalous electrical behavior observed in Schottky diodes under reverse bias and correlated it with the presence of SFs. In particular, we proposed for the first time a physical model based on space-charge limited current to explain the increase of the reverse leakage current and its temperature behavior in the presence of SFs.

Experimental Details

The starting material was a 6.5 µm-thick n-type 4H-SiC (0001) epilayer, with nitrogen doping of 1.0×10^{16} cm^{-3}, grown onto a heavily doped 200 mm size substrate. From this wafer, two sample pieces, located in a lateral region at around 65 mm from the center, were cut and used to fabricate Schottky diodes by optical lithography and lift-off processes. The devices consisted in a large area back-side nickel silicide Ohmic contact [10] and circular tungsten (W) Schottky contacts with a diameter of 300 µm on the front side [11]. The contacts were subjected to thermal annealing treatment at 700 °C for 10 min in N_2 atmosphere. The schematic representation of the sample location over the wafer and the cross-section view of the contacts are represented in Figs. 1a and 1b, respectively. An electrical characterization was performed by means of current–voltage (I–V) measurements, under both forward and reverse bias and with testing temperature varying in the range 25-150 °C, and capacitance-voltage (C-V) measurements. The electrical curves were acquired in a Karl-Suss MicroTec probe station equipped with a parameter analyzer. Furthermore, the sample quality was inspected by micro-photoluminescence (µ-PL) carried out by a Horiba Jobin Yvon HR800 spectrometer under excitation line at 325 nm (He-Cd laser). Morphological measurements at nanometric scale were also performed by an Atomic Force Microscopy (AFM) system (Digital Instrument D3100) equipped with a Nanoscope V controller and combined with in-plan Scanning Capacitance Microcopy (SCM) analysis [12].

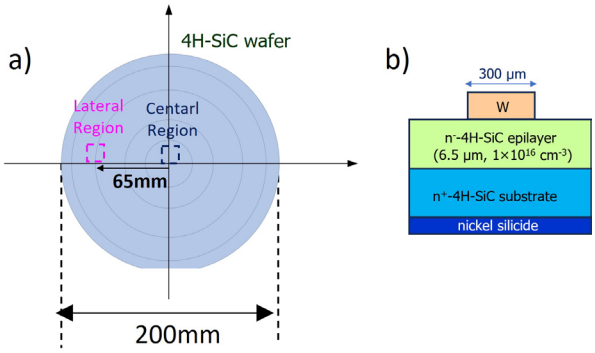

Fig. 1. a) Schemtaic view of the location on the 4H-SiC wafer for the samples under study. b) Cross-section scheme of the fabricated contacts.

Results and Discussion

Firstly, we investigated the electrical characteristics of the material by means of I-V measurements on a set of diodes fabricated in the two samples. In particular, Figs. 2a and 2b reports the current density-voltage (J-V) curves under forward and reverse bias, respectively, for the diodes in the central region, while fig. 2c and 2d are related to the forward and reverse characteristics of the diodes located in the sample from lateral region. The forward characteristics in both samples (Fig.2a and 2c) presented an extended linear region in the semilog plot that can be described by the thermionic emission (TE) theory [13]. The Schottky barrier height (ϕ_B) and the ideality factor (n), derived from this analysis, were very similar in the two cases, with $\phi_B = (1.24 \pm 0.03)$ eV and $n = 1.09 \pm 0.03$. Instead, under reverse bias, while the diodes fabricated in the central region (Fig. 2b) exhibit a leakage current that can be described by the thermionic field emission (TFE) [14], a different trend of the reverse characteristics with a significantly higher leakage current (three decades higher) were observed in the devices fabricated in the lateral region (Fig.2d) [15].

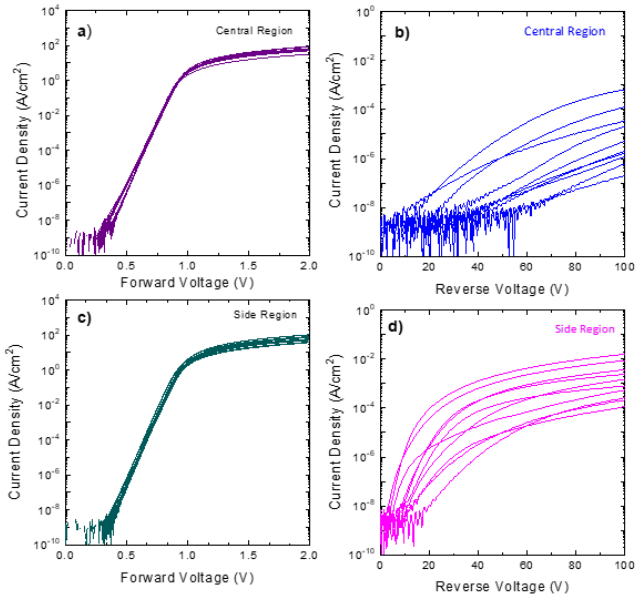

Fig. 2. Forward and reverse current density- voltage (J-V) characteristics acquired in diodeds fabricated in the central region (*a* and *b*) and in a lateral region (*c* and *d*) oft he wafer.

In order to exclude a different doping level as origin of the observed electrical features, we performed C-V measurements on Schottky contacts located in the two regions. As one can see in Fig.3a, the C-V curves exhibited a very similar behavior, indicating that in the two wafer regions the upper part of the epilayers has the same doping level. Specifically, as reported in Fig.3b, the doping concentration, derived from the C-V characterization [13], is around 1.0×10^{16} cm^{-3} for both regions. Hence, the anomalous trend of the leakage current observed in diodes fabricated in the lateral region cannot be attributed to a different doping of the sample.

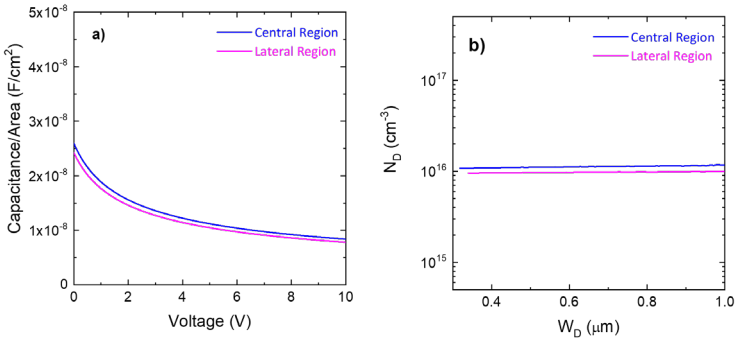

Fig. 3. *a)* C-V curves related to Schottky diodes in a cnetral and a lateral regions. *b)* Doping level as function of the depletion width extrapolated by the C-V curves.

Representative reverse characteristics of the two kinds of diodes are reported in Fig.4a. For contacts in the central region, the leakage current can be described by the TFE theory [14] (not shown here), typically used for explaining the reverse characteristics in Schottky diodes in 4H-SiC based on similar W-based metallization schemes [11,16]. Instead, it is necessary to consider different current transport mechanisms to explain the anomalous trend of the leakage current in diode in the lateral region. By considering a log-log plot of a representative reverse characteristic of this region, as reported in Fig.4b, we observed that it can be described by a power-law dependence of the current density on the applied voltage ($J\propto V^m$), with three regions characterized by a different exponent m. These can be identified as follows: $m \approx 1$ below 10V, $m = 7.5$ for $10V < V < 30V$ and $m \approx 2$ above 30V. Such behavior of the leakage current can be described by considering a space-charge-limited current (SCLC) model [17], in the presence of a trap distribution exponentially decreasing with the distance from the conduction band edge [18]. In practice, this model predicts an ohmic behavior (m=1) at low voltage, when the density of thermally generated free carriers in the semiconductor dominating over the injected carriers from the metal. With the increasing the applied voltage, a space-charge appears, due to the filling up of the traps in semiconductor with the carriers injected from the metal. In the third region, the quadratic dependence (m=2) can be associated to a complete filling of the traps, which can be compared to a trap-free situation, with the current ruled by the Mott–Gurney law [19].

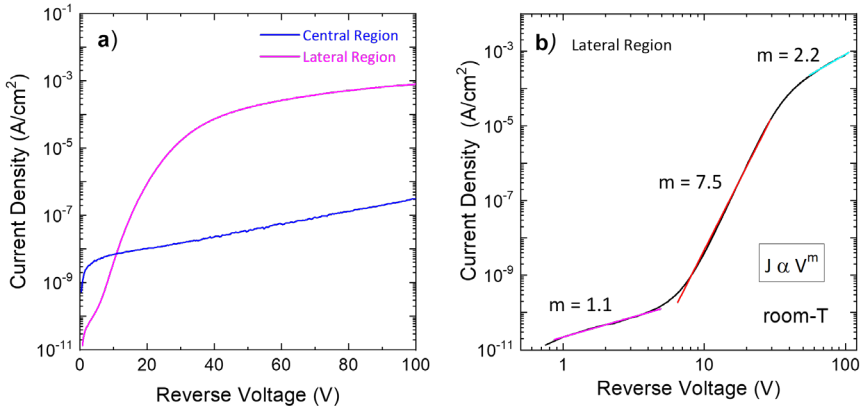

Fig. 4. a) Representative reverse characteristics fot the diodes located in the central and in the lateral regions. b) Log-log plot of the room-temperature reverse J-V characteristic for the curves of the lateral region.

In order to have a better understanding of the current transport mechanisms, we studied the temperature-dependence of the current-voltage characteristics, reported in Fig.5. In particular, in the intermediate regime (m=7.5), the curves J-V (reported by dashed lines) can be reproduced by the SCLC model according to the following equation

$$J = q\mu N_C \left(\frac{\varepsilon_S}{qN_0kT_t}\right)^l \frac{V^{l+1}}{L^{2l+1}} \quad (1)$$

where q is the elementary charge, μ is the free-electron mobility, N_C is the conduction-band state density, ε_S is the dielectric constant of the semiconductor, N_0 is the trap density, k is the Boltzmann's constant, L is the thickness of space-charge layer and l= m-1. From this equation, by choosing an arbitrary (J,V) point on the reverse characteristic, we derived N_0 value of 9×10^{18} cm^{-3} eV^{-1} at room-temperature. In this calculation, we have considered the temperature-dependence of the exponent $l=T_t/T$, with T_t a characteristic temperature parameter related to the trap distribution [20]. Furthermore, for the highest reverse bias range, the almost temperature-independence of the leakage current allows to suppose the existence of a tunneling mechanism through the barrier, favored by the high reverse bias that produces a band bending and thinning of the barrier.

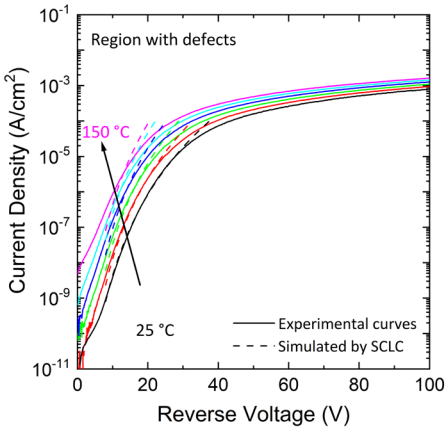

Fig. 5. Temperature-dependence of the reverse leakage current in the defective region and the simulated curves according to the SCLC model.

Finally, we inspected the surface quality by μ-PL, in order to have additional information on the origin of these trap levels. Indeed, this characterization revealed the presence of defects, as visible in Fig. 6. Specifically, Fig.6a shows a μ-PL intensity map related to the spectral range 425-430 nm acquired around the contact pad. We observed the presence of a PL-triangular shape defect that can be associated with the presence of single Shockley SF (1SSF) defects, probably coming from basal plane dislocations (BPDs) [21]. In addition to the triangular shape, also the PL signal peaked around 425 nm (2.92 eV), clearly visible in the PL spectrum reported in Fig.6b and acquired in the center of the triangular defect, is consistent with the 1SSF defect, usually observed in epitaxial 4H-SiC layers [21]. We performed this kind of measurements also on a metal pad, after removing intentionally a metal strip to enable the laser penetrating in the material. From this experiment, we observed that these defects can extend under the pad, i.e. in the active area of the device [15].

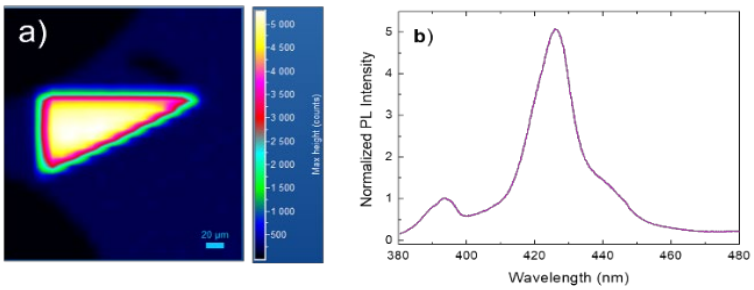

Fig. 6. a) μ-PL intensity map in the range 425-430nm acquired in the defective area. b) PL spectrum in the range 380-480 nm.

To this investigation, we combined a morphological analysis by AFM associated with a nanoscale characterization by SCM of the electrical properties carried out in a defective region. The morphological and SCM maps are reported in Figs. 7a and 7b, respectively. The surface morphology presented the commonly features of the 4H-SiC surface. Instead, the lateral variation of the capacitive signal in the SCM map indicates a local charge density variation. This can be due either to a local difference in the active dopant concentration in the epitaxy or to charges trapping in the near surface-region of the defect. However, the C–V characterization presented above allowed to exclude a different incorporation of active dopants in the defective and defect free regions. Hence, the locally increased in the SCM signal can be ascribed to trapped charges in the surface region and these can be at the origin of the trap level in the SCLC model, giving the anomalous behavior of the leakage current.

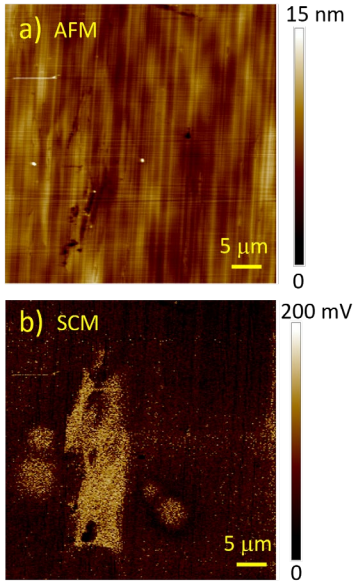

Fig. 7. a) AFM morphological and b) the associated SCM maps, acquired in a defective area.

Summary

In this work, we have studied the effects of defects (SFs) on the electrical properties of 4H-SiC Schottky diodes under both forward and reverse bias, focusing on the anomalous behavior of the leakage current in the presence of stacking faults. The diodes were fabricated in two different samples, extracted from a central and lateral region of a 4H-SiC wafer. While the forward characteristics of the two set of diodes fabricated in the different regions obeyed to the thermionic emission theory, an anomalous leakage current trend was observed in the diodes fabricated in the lateral region. After excluding a variation of doping for the two cases by analyzing the C-V characteristics for the diodes in lateral and central region, the anomalous increase of the leakage current was explained by considering a space-charge limited current (SCLC) theory. The model takes into account the presence of a trap distribution in the bandgap of 4H-SiC, whose origin can be associated to the 1SSF presence, as confirmed by photoluminescence measurements. Also, AFM and SCM analyses confirmed a variation of the local charge density in the defect area due to charge trapping. The weak temperature dependence of the reverse current at high voltage suggests that a carrier tunneling mechanism can be also present. This work can be useful to explain the defect impact on the electrical characteristics of 4H-SiC Schottky diodes.

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