Final published version of this article: **Applied Electronic Materials**,
Cite: *ACS Applied Electronic Materials* **2024** *6* (2), 669-678

Available online: 7 February 2024

DOI: https://doi.org/10.1021/acsaelm.3c01026

# Self-Rectifying Gr/TMDC Heterostructures: Candidates for Resistive Switching Memory Devices

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ABSTRACT: Self-rectifying graphene-transition metal dichalcogenides (Gr/TMDCs)-based resistive random-access memory (ReRAM or RRAM) has been shown to be a promising candidate for next-generation nonvolatile memory technology. However, the low resistance on/off ratio and the high operating voltage are still big challenges for low power-consuming devices. Here, we reported Au/Gr/$MoS_2$/Au- and Au/Gr/$WS_2$/Au-based ReRAM structures, thereby operating at a low voltage with a high on/off current ratio of $\sim 10^3$. Also, our results showed excellent endurance ($\sim 2 \times 10^2$ cycles) and stable retention performance ($\sim 10^4$ s), which demonstrate the promising characteristics of memory devices. Additionally, in the Au/Gr/$WS_2$/Au structure, the rectifying zone is observed at −2 V, which prevents interference with adjacent cells during reading operations. In reverse bias, the purposed device has an intrinsically self-rectifying property, not requiring to reset the device for operation. The self-rectifying property of the Au/Gr/ $WS_2$/Au structure allows it to cover a 48 × 49 RRAM array. This research on Gr/TMDCs-based RRAM provides the basis for future miniaturization of nanoelectronics

KEYWORDS: *resistive switching devices, 2D materials, self-rectifying, crossbararray, current−voltage (IV) and capacitance−voltage (CV) measurements, Schottky contact*

## 1. INTRODUCTION

Conventional memory storage devices, such as flash memory, if the bit line and word line junctions are only occupied by are approaching their limit in time to come. Recently, resistors with symmetric straight line I−V characteristics. Since resistance-dependent novel memories, including magnetic several cells are coupled via the bit line and word line, an random-access memory (MRAM), phase-change random accidental leakage current is produced from the nearby cells.

Additionally, when data on the target memory cell are accessed, sneak current flows through the unassigned path in a low resistance state (LRS) to the neighboring cell, which affects the overall device performance.[12−18] Work on the RRAMs with extra selectors, such as resistors and diodes, has been carried out to address this problem and extend the read margin. Several selector configurations including 1R, 1D1R, and the combination of transistors and resistors were used to access memory (PRAM), and resistive switching-based random-access memory (RRAM), have gained popularity in place of conventional three-terminal charge-based memory devices due to their dominant, simplistic 2-terminal structure, and broad device integration rate.[1−8] Among them, RRAM devices attract researchers because of their simple metal− insulator−metal (MIM) and metal−insulator−semiconductor (MIS) structures with nonvolatile nature, excellent endurance stability ($>10^3$), fast switching response (<10*ns*), and a long retention time ($>10^3$ s).[9−11] As the integration scale continues to minimize, the density of devices can be increased on a smaller area and exhibit much better performance by utilizing multiple active cells. It can be achieved by fabricating a vertically stacked crossbar arrangement structure, which increases the memory storage density to a larger extent. In the crossbar array structure, the word line and the bit line are frequently exploited to read, write, and process the data in resolve the sneak path issue but still there exist complexities in their fabrication as well as their working.[19,20]

Due to their potential for downsizing, versatility and wearable electronics, high-memory storage, mega response, and large on/off ratio, 2D materials are promising candidates for low operating voltage, high-speed processing, and forthcoming data storage. A novel material platform for the construction of superior RRAM devices is made possible by the van der Waals interface, which also permits the synthesis of several 2D material heterostructures without any lattice mismatch problems. Graphene (Gr) is the first 2D material that has high charge carriers' mobility, large surface-to-volume ratio, excellent flexibility, and high transparency used in RRAM devices.[21−23] Due to the high conductivity of graphene and its derivatives, they are used in RRAM devices as the

electrode material, as well active layer due to low power consumption, negligible sheet resistance, and stable retention performance.[24−27] More importantly, the higher value of thermal conductivity in a single-layer range from 4.8 ± 0.44 to 5.30 ± 0.48 W/mK facilitate the quick transfer of heat generation during continuous cycling in ReRAM devices.[28] The graphene solely used in RRAM devices is still facing issues due to surface effects and random formation and rupture of channel owing to its high conductivity, and thickness leads to uncontrollable switching. Transition metal chalcogenides (TMDCs), a new class of 2D material, gained a lot of attention due to its high surface-to-volume ratio, tunable band gap, and weak van der Waal interactions between the layers.[22,29−31] Tungsten disulfide ($WS_2$) and molybdenum disulfide ($MoS_2$) are the most fascinating materials due to their outstanding performance in RRAM devices. These devices also show a high on/off ratio of $10^3$, excellent cyclic stability, and superior retention performance. Simpson et al. reported that the thermal conductivity of single-layer $MoS_2$ is 34.5 W/mK, which increased to 52 W/mK for multilayer $MoS_2$ making it stable at high temperatures.[32] The major conduction mechanism in TMDCs-based RRAM devices is the formation and rupture of the sulfur-deficient filamentary channel and electrode desorption metallic channel formation. The migration of carriers needs relatively high voltage for the set and reset process in TMDCs owing to their semiconductor nature. Second, continuous formation and rupture of channels under opposite polarities cause heating effects, which degrade the resistive switching properties of the TMDCs-based devices.[33−37] Researchers have tried to fabricate Gr/TMDC and TMDC/ TMDC ($MoS_2/WS_2$, graphene/$ReS_2$, etc.)[22−26] heterostructures in which modulation of barrier at interface is responsible for set and reset processes. These techniques eliminate the random formation and rupture of the channel and provide more stable device operation over a long time.[38−41] Jo et al. reported Gr/$MoS_2$ memristors and achieved a high $10^5$ on/off ratio.[42] Gao et al. reported $MoS_2/WS_2$ heterostructures for ReRAM application and achieved an on/off ratio of $10^4$ with stable endurance after 120 cycles.[43] The border traps at the interface between 2D materials are responsible for charge trapping and detrapping at lower voltages, which leads to a filament-free conduction path. In addition, the Schottky contact between the semiconductors and the metal electrode-semiconductor is primarily responsible for the selfrectification. Instead of employing external selectors, Schottky contact RRAM devices can simplify the design and production of 3D crossbar arrays without any sneak path by providing the self-rectifying behavior.[44]

In this work, we proposed Gr/TMDCs based on bipolar and self-rectifying RRAM devices. The proposed self-rectifying Au/ Gr/$WS_2$/Au structure operating at a lower voltage is favorable to shield the data leakage and minimize the sneak path current in a dense crossbar array. The border traps calculated from capacitance voltage (CV) measurements are responsible for carrier trapping and detrapping at Gr/$MoS_2$ and Gr/$WS_2$ interface. In addition, the high effective barrier height extracted from CV measurement leads to the self-rectifying behavior in the Au/Gr/$WS_2$/Au ReRAM structure. To better understand the properties of RS when applied to an array, numerical analysis was performed to find the highest read margin (RM) value that can protect data. These findings support the realization of low operating voltage, high on/off ratio, and selector-free RRAM devices for high-dense array applications.

## 2. EXPERIMENTAL SECTION

**2.1. Sample Preparation.** Chemical vapor deposition (CVD) is one of the most promising ways to produce high-quality, large-scale, two-dimensional thin films. For graphene thin film growth, the copper foil was placed at the center of the furnace at a high temperature (1000 °C) in the methane gas ($CH_4$) environment with 95% Ar+5% H carrier gases under 20 sccm flow and remained at this temperature for 15 min and then allowed to cool down at room temperature.[45] Copper foils are used for the growth of SL graphene because copper is an effective catalyst in the CVD process to break down hydrocarbons ($CH_4$), which is essential for the formation of graphene. Furthermore, homogeneous heating during the deposition process is ensured by its excellent thermal conductivity providing uniform heat distribution and minimizing temperature variations, producing high-quality graphene. The $WS_2$ and $MoS_2$ flakes were purchased from SigmaAldrich and used without any modification.

**2.2. Device Fabrication.** The heterostructures of Gr/$WS_2$ and Gr/$MoS_2$ were synthesized by combining mechanical exfoliation and photolithography processes. Afterward, RRAM devices were fabricated using these heterostructures as an active medium between two electrodes in the device structure. Initially, PMMA is coated on graphene-grown copper foil (Cu/Gr) by spin coating at 3000 rpm for 60 s. Then Cu/Gr/PMMA was immersed in an ammonia solution, which etched away the copper foil, and graphene remained attached to PMMA. After the removal of residues by rinsing with DI water, the Gr/PMMA membrane was scraped out onto the Si/$SiO_2$

substrate. Then the Si/$SiO_2$/Gr/PMMA structure was put down into acetone to remove the PMMA, which etched the PMMA, and the final product was the graphene on the Si/$SiO_2$ substrate. The photolithography technique was used in the device fabrication process. First, a thin positive photoresist (PMMA) uniform layer of a few hundred

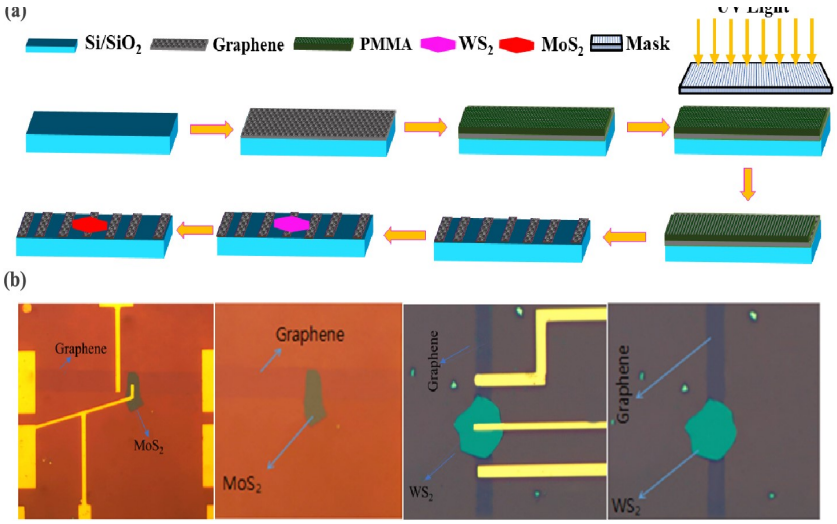


Figure 1. (a) The schematics of the step-by-step fabrication process of the Au/Gr/TMDC/Au device; (b) the real devices image fabricated by combined mechanical exfoliation and a photolithography technique with Au external contacts.

nanometers was coated on Si/$SiO_2$/Gr substrate by spin coating at 3000 rpm. Then Si/$SiO_2$/Gr/PMMA was placed on a hot plate at 200 °C to harden the PMMA. After that, the photoresistive layer was exposed to UV light through a shadow mask. The developer dissolved the polymer PMMA that was exposed to light, with the rest of the polymer film intact. To remove the uncovered graphene and PMMA residues, oxygen plasma etching was used at a power of 50 W for 120 s at room temperature. Then the wafer was cleaned with DI water and put into acetone, which removed the polymer not exposed to light, with graphene under it. Finally, 10-$\mu$m wide uniform graphene strips were on the Si/s$SiO_2$ substrate as shown in Figure 2a.

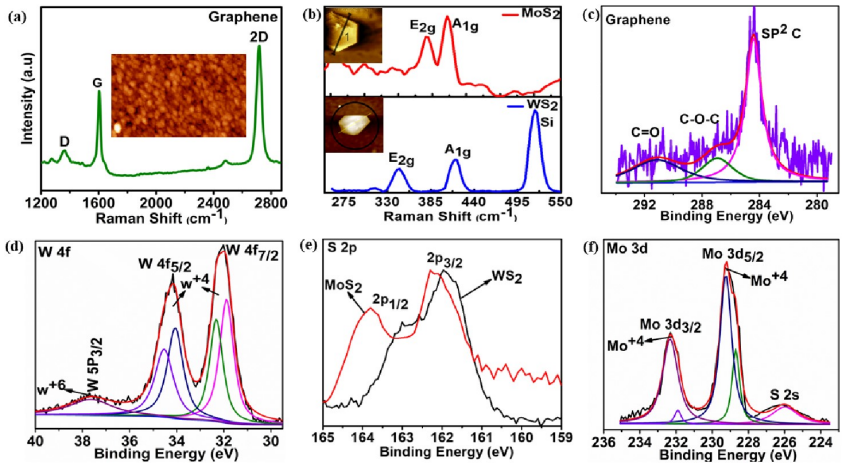


Figure 2. Raman spectra of (a) single-layer graphene, the inset shows the AFM image of the graphene on Cu foil, (b) tungsten disulfide (($WS_2$) blue color), and molybdenum disulfide (($MoS_2$) red color) films, inset shows the corresponding AFM images, XPS spectra of (c) graphene, (d) W 4f, (e) S 2p, and (f) Mo 3d.

The exfoliated flakes of $WS_2$ and $MoS_2$ were transferred on a graphene strip through PDMS by using a screw-gauge micromanipulator mechanical transfer stage equipped with a highresolution optical microscope. Then a few 100 nm positive photoresists (PMMA) were spin-coated on $Si/SiO_2/Gr/WS_2$ and $Si/SiO_2/Gr/MoS_2$. After that, the wafer was baked and exposed to UV light through the desired photo mask. Subsequently, PMMA was exposed to light, and the wafer was put into a developer that to light. The heterostructure's overlap area plays a significant role in determining the overall performance parameters. Scaling down the overlap area results in a higher array density, which is favorable for boosting memory capacity but trade-offs with other RRAM characteristics. Moreover, minimal coverage area is more sensitive to trap sites at the interface and might cause localized stress during continuous switching, which can degrade endurance, and elevate SET/RESET voltage variability. Figure 1 shows the illustration of the removed the part of the polymer that was exposed to light and the unexposed part remained intact. For external contacts, $Si/SiO_2/Gr/WS_2$ and $Si/ SiO_2/Gr/MoS_2$ wafers were mounted onto a high vacuum chamber at the base pressure of ($4 \times 10^{-6}$ Torr), where the gold contacts were deposited by a thermal evaporation process. After removal from the chamber, the $Au/Gr/WS_2/Au$ and $Au/Gr/MoS_2/Au$ structures on the $Si/SiO_2$ wafer were immersed in acetone that dissolved the residual PMMA that was not exposed to light. The heterostructure's overlap area plays a significant role in determining the overall performance parameters. Scaling down the overlap area results in a higher array density, which is favorable for boosting memory capacity but trade-offs with other RRAM characteristics. Moreover, minimal coverage area is more sensitive to trap sites at the interface and might cause localized stress during continuous switching, which can degrade endurance, and elevate SET/RESET voltage variability. Figure 1 shows the illustration of the step-by-step process for device fabrication. Figure 1b reveals the actual optical image of the heterostructures and final device with external gold (Au) contacts.

## 3. RESULTS AND DISCUSSION

**3.1. Raman Spectroscopy.** Structural characteristics and molecular vibrational modes in graphene, $MoS_2$, and $WS_2$ were investigated by using Raman spectroscopy (Model, Dongwoo Optron Co. Ltd.), equipped with an argon laser of wavelength 514 nm and a power of 30 mW. The Raman spectra of graphene show three dominant peaks, G peak, D peak, and 2D peak, as labeled in Figure 2a. The G band located at a wavenumber of 1604 $cm^{-1}$ arises from the stretching of carbon−carbon (C−C) bonds and the D peak originated at 1365 $cm^{-1}$ due to defects present in graphene. The sharp 2D band positioned at 2717 $cm^{-1}$ in the Raman spectra of graphene signifies the layered nature of the graphene.[46−48] The two prominent peaks in the Raman spectra of $WS_2$ are shown in Figure 2b. The $A_{1g}$ peak, located at 418 $cm^{-1}$, is primarily caused by the out-of-plane motion of sulfur atoms with respect to tungsten atoms, while the $E^1_{2g}$ peak located at 351 $cm^{-1}$ is caused by their in-plane motion. The peak difference in $A_{1g}$ and $E^1_{2g}$ modes in $WS_2$ is 62.5, 63.4, and 65.5 $cm^{-1}$ for single layer, double layer, and multilayer, respectively.[49] The difference in the peak position value of $A_{1g}$ and $E^1_{2g}$ in $WS_2$ as shown in Figure 2b is 67 $cm^{-1}$, which indicates the multilayer $WS_2$. Similarly, in $MoS_2$ spectra the peak difference in $A_{1g}$ and $E^1_{2g}$ peak is 18.4 $cm^{-1}$ for a single layer and increased up to 25 $cm^{-1}$ for a multilayer $MoS_2$. The peak difference in the peak position value of $A_{1g}$ and $E^1_{2g}$ in the graph of $MoS_2$ is 25 $cm^{-1}$, which also refers to the multilayer exfoliated $MoS_2$ flakes on PDMS.[49,50]

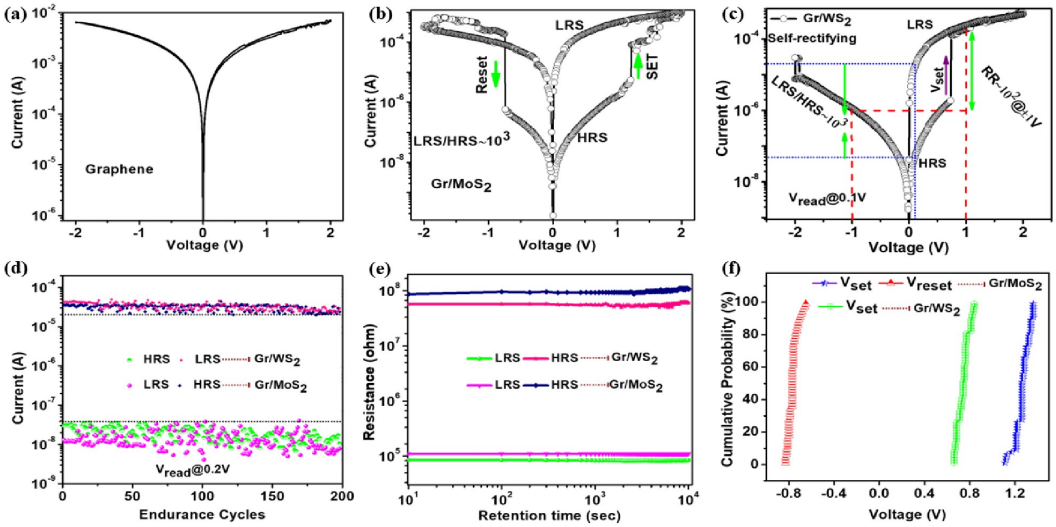


Figure 3. Current−voltage (I−V) graph of (a) graphene, (b) Au/Gr/$MoS_2$/Au, and (c) Au/Gr/$WS_2$/Au, (d) cyclic endurance after 200 cycles, (e) retention performance for $10^4$ seconds, and (f) cumulative probability of set and reset voltage, for Au/Gr/$MoS_2$/Au, and Au/Gr/$WS_2$/Au.

**3.2. X-ray Photoelectron Spectroscopy (XPS).** X-ray photoelectron spectroscopy (XPS) is a surface technique used to identify the chemical state of the elements, their composition, and the stoichiometry of synthesized samples. The carbon C 1s peak at 284.6 eV was used as a reference in Gr/$MoS_2$ and Gr/$WS_2$ XPS spectra to calibrate the binding energy scale. In XPS spectra of graphene, three major peaks at the binding energy values of 284.6, 287.03, and 291.17 eV correspond to the C−C bond, C−O−C, and C = O, respectively, as shown in Figure 2c.[51,52] Figure 2d,e presents the core level spectra of tungsten (W) and sulfur (S) in $WS_2$. The dual peaks in spectra of tungsten (W) at a binding energy of 32.02 and 34.15 eV, corresponding to W $4f_{7/2}$ and W $4f_{5/2}$, respectively, confirm the $W^{4+}$ oxidation state of $WS_2$. Additionally, the minor W $5P_{3/2}$ peak originating at a binding energy of 37.7 eV signifies the $W^{6+}$ oxidation state of $WO_3$, which is in good agreement with literature.[53−57] In Figure 2f, two peaks located at binding energies of 229.19 and 232.31 eV referring to Mo $3d_{5/2}$ and Mo $3d_{3/2}$, respectively, indicated an oxidation state of $Mo^{4+}$ in $MoS_2$.[58,59] The sulfur 2P spectra have dual peaks originated at the binding energy of 161.88 eV and 162.89 eV in $WS_2$ and (162.3 eV and 163.8) eV in $MoS_2$, corresponding to $2P_{3/2}$ and $2P_{1/2}$, respectively, which is presented in Figure 2e.

**3.3. Atomic Force Microscopy (AFM).** Atomic force microscopy (AFM) is a surface technique used to examine the surface morphology, surface roughness, and the number of exfoliated layers of graphene, $WS_2$, and $MoS_2$.[18]The variations are noticed in the thicknesses of the exfoliated $WS_2$ and $MoS_2$ flakes. The average calculated thickness of the $WS_2$ and $MoS_2$ is 54 ± 2 and 54 ± 2 nm with corresponding RMS values of 74 ± 2 and 62 ± 2 nm, respectively. However, the CVD grown graphene on Cu foil is a single layer confirmed by AFM, as presented in the Figure 2a inset. The AFM images of $WS_2$ and $MoS_2$ flakes on PDMS are shown in the inset of Figure 2b.

## 4. RESISTIVE SWITCHING (RRAM) MEASUREMENTS

**4.1. Current−Voltage (I−V) Measurements.** To investigate resistive switching characteristics of fabricated Au/Gr/Au, Au/Gr/$MoS_2$/Au, and Au/Gr/$WS_2$/Au memory cells, two probe current−voltage (I−V) measurements were performed in the direct current (DC) mode at room temperature. In single-layer graphene, no resistive switching behavior was observed due to its semimetallic nature and retained its ohmic behavior with high forward and reverse current of 10 mA as shown in Figure 3a. The Au/Gr/$MoS_2$/Au device revealed bipolar resistive switching behavior with an HRS/LRS ratio of $10^3$. A set process occurred in the positive voltage region at 1.2 V, which

switched the device from a high resistance state (HRS) to a low resistance state (LRS). When the voltage is swept back in the reverse direction, the device switches back to its HRS from the LRS at −0.73 V, known as the reset process, which is portrayed in Figure 3b. For the Au/Gr/$WS_2$/Au ReRAM cell, in addition to bipolar resistive switching with an HRS/LRS ratio of $10^3$, a self-rectifying phenomenon is also observed within the −2 V zone, exhibiting an excellent rectification ratio (RR) of $10^2$. Under the positive sweep voltage, the device altered its state from HRS to LRS at 0.74 V, referring to the set process. The current in the positive voltage region at 1 V is 10 mA, while in the negatively biased region, it decreased from 10 mA to 10 $\mu$A at −1 V, which led to the nonlinear or asymmetric I–V curve, portraying its self-current limiting feature, as presented in Figure 3c. The gradual decrease in current in the negative bias region and the absence of the reset process are due to the suppression of carriers, referring to the presence of a highly effective Schottky barrier in the Au/Gr/$WS_2$/Au memory cell. The nonlinear I–V characteristic of the Au/Gr/$WS_2$/Au ReRAM cell prevents interference in the crossbar array structure to neighboring cells during the read operation. Furthermore, both Au/Gr/$MoS_2$/ Au and Au/Gr/$WS_2$/Au ReRAM devices showed forming-free and self-compliance ReRAM behavior demonstrating their potential toward low-powered memory storage devices.

Table 1. Summary of 2D Layered-Based ReRAM Devices

| bottom electrode | top electrode | substrate | active material | on/off ratio | endurance | retention | references |
|---|---|---|---|---|---|---|---|
| Au | Au | glass | $MoS_2$ | $10^3$ | $10^2$ | $10^4$ | 71 |
| Au | Au | Si/$SiO_2$ | $MoS_2$ | $10^3$ | – | – | 72 |
| Ti | Au | Si | $MoS_2$/PbS | $10^2$ | $10^3$ | $10^4$ | 73 |
| ITO | Cu | PET | $MoS_2$/PMMA | $10^3$ | $10^5$ | $10^5$ | 74 |
| Ag | Ag | PET | $WS_2$ | $10^3$ | $10^2$ | $10^5$ | 75 |
| Pt/Ti | Al | Si/$SiO_2$ | $WS_2$ | $10^3$ | $10^2$ | – | 76 |
| ITO | Al | Glass | GO/$MoS_2$ | $10^2$ | – | – | 77 |
| Ag | Cu | paper | Gr/$MoS_2$ | $10^4$ | $10^2$ | $10^4$ | 27 |
| Cr/Au | Cr/Au | Si | $HfO_2$/$Al_2O_3$/$MoS_2$ | $10^4$ | $10^2$ | $10^3$ | 78 |
| Au | Au | Si/$SiO_2$ | $WS_2$/QDs | $10^4$ | – | $10^1$ | 79 |
| Au | Au | Si/$SiO_2$ | Gr/$ReS_2$ | $10^5$ | – | $10^4$ | 80 |
| ITO | Al | Glass | $WS_2$: PMMA | $10^4$ | $10^2$ | $10^4$ | 81 |
| $W_2N$ | Cu | Si | $MoS_2$ | $10^3$ | $10^3$ | $10^3$ | 82 |
| Au | Au | Si/$SiO_2$ | Gr/$MoS_2$ | $10^3$ | 2× $10^2$ | $10^4$ | this work |
| Au | Au | Si/$SiO_2$ | Gr/$WS_2$ | $10^3$ & RR = $10^2$ | 2× $10^2$ | $10^4$ | this work |

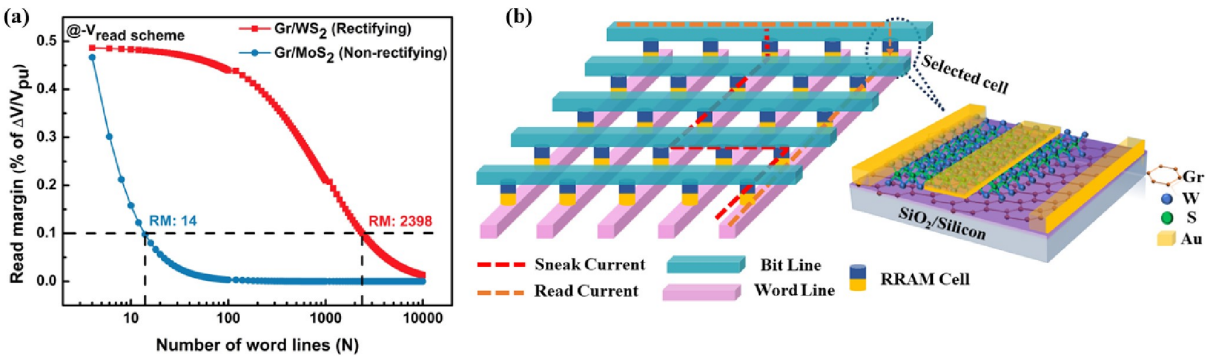


Figure 4. (a) Read margins of RRAM with Au/Gr/$MoS_2$/Au, and Au/Gr/$WS_2$/Au structures. (b) Purposed 3D crossbar array structures with fabricated Au/Gr/TMDC/Au cell.

A two-dimensional material with exceptional electrical characteristics, graphene is extensively utilized in ReRAM devices. The movement of charge carriers during the switching process is highly facilitated by single-layer graphene, owing to its remarkable electrical conductivity, which enables effective switching. The semiconducting $MoS_2$ and $WS_2$ serve as a switching medium in conjunction with highly conductive graphene in Au/Gr/$MoS_2$/Au

and Au/Gr/$WS_2$/Au, respectively. In the Au/Gr/$WS_2$/Au RRAM device, when a voltage is applied across the device, the injection and expulsion of carriers from the top electrode and graphene under the SET and RESET operations, respectively, change its resistance by forming and rupturing conductive filaments within the $WS_2$ layer, which modulate the LRS and HRS switching states. Furthermore, regulating the movement of charge carriers between the electrodes and active layers involves the modulation of Schottky barriers at the interfaces between Au/$WS_2$ and Gr/$WS_2$. The Schottky barriers function as energy barriers and the device's resistive switching behavior depends substantially on this modulation of the barrier height.

It enables control over current flow and resistance variations under SET and RESET operations, responsible for transitioning device states between LRS and HRS. The calculated effective Schottky barrier height for Au/Gr/$MoS_2$/Au and Au/ Gr/$WS_2$/Au devices is 0.28 and 0.69 eV, respectively.[60–62]

To further examine the reliability and stability of the Au/Gr/ $MoS_2$/Au, and Au/Gr/$WS_2$/Au devices, an endurance test was programmed for 2 × $10^2$ continuous DC cycles at room temperature as shown in Figure 3d. Both devices maintained their HRS and LRS after 2 × $10^2$ repetitive sweeping cycles. The LRS of both devices did not exhibit any notable variation, while a negligible variation is observed in the HRS of the device. The fabricated Au/Gr/$MoS_2$/Au and Au/Gr/$WS_2$/Au devices can withstand up to 2 × $10^2$ continuous endurance cycles and maintained the on/off ratio of $10^3$ prior to a significant degradation. To investigate the ability of the devices to store/erase data in HRS and LRS, a retention test was also performed for $10^4$ s as shown in Figure 3e. Both Au/Gr/ $MoS_2$/Au and Au/Gr/$WS_2$/Au devices retained their HRS and LRS with an on/off ratio of $10^3$. The LRS state of both the devices is highly stable, while the HRS state experienced a slight deterioration after 7 × $10^3$ s due to the gain in thermal energy by charge carriers. In Figure 3f, the cumulative probability distribution of set and reset voltage for consecutive 2 × $10^2$ DC cycles is plotted. The variation in set and reset voltage is 0.31 and 0.28 V for Au/Gr/$MoS_2$/Au, respectively, while the variation in set voltage is 0.26 V for self-rectifying characteristic Au/Gr/$WS_2$/Au devices, which are in the acceptable range for RRAM devices. The comparative study of various ReRAM structures is presented in Table 1.

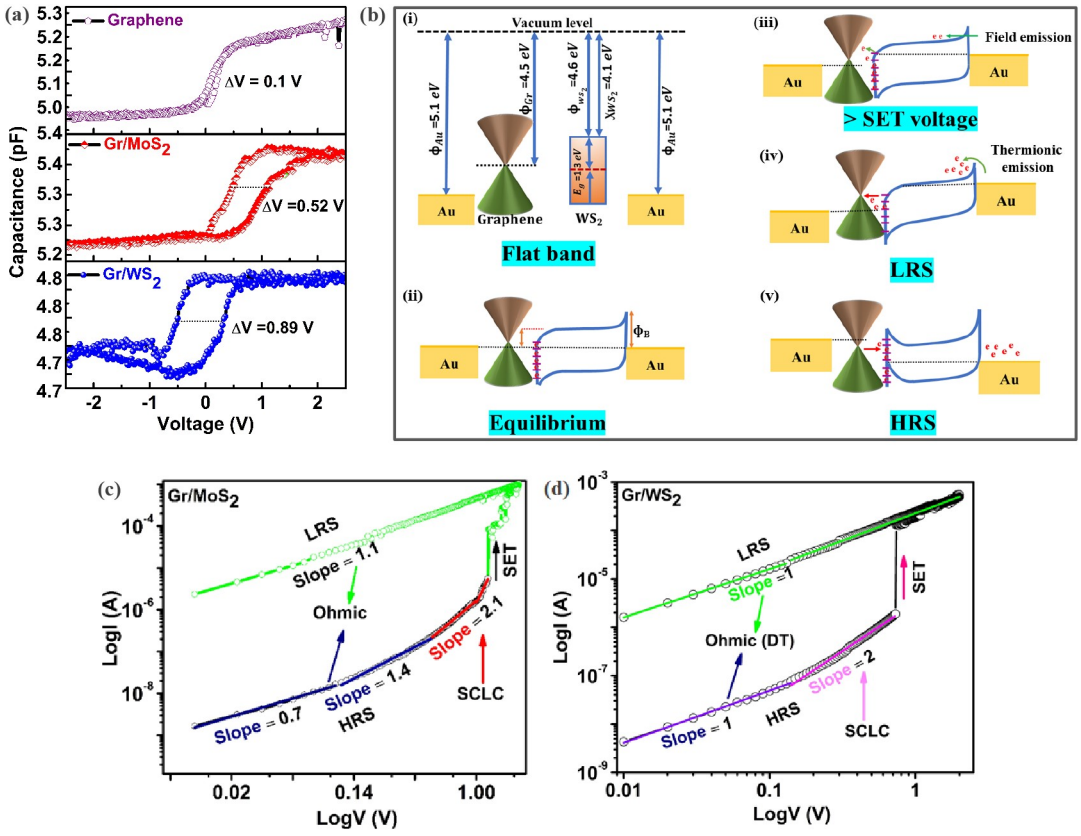


Figure 5. (a) Typical CV characteristics of graphene, Au/Gr/$MoS_2$/Au, and Au/Gr/$WS_2$/Au at sweeping voltages, (b) energy band diagram of Au/Gr/$WS_2$/Au, (i) isolated condition (ii) in equilibrium (iii) $V_{app}$ < SET voltage (iv) in LRS (v) in HRS state, Log I vs Log V plot explain the conduction mechanism in (c) Au/Gr/$MoS_2$/Au, and (d) Au/Gr/$WS_2$/Au.

To evaluate the feasibility of high-density memristor arrays directly, the normalized read margin at the pull-up voltage was calculated by solving Kirchoff's equation.[63] Figure 4a depicts the read margin results for RRAMs with Au/Gr/$MoS_2$/Au and Au/Gr/$WS_2$/Au structures. Word lines function as interconnects between multiple RRAMs to enable the data storage. When the read margin falls below 0.1% and the number of word lines increases, differentiation between resistive states in the RRAM becomes more challenging, resulting in an error in the RRAM array. The RRAM array operates within the normal range when the read margin of the number of words exceeds 0.1%. The results show that the Au/Gr/$MoS_2$/Au structure can cover a 3 × 4 RRAM array, while the self-rectifying properties of the Au/Gr/$WS_2$/Au structure allow it to cover a 48 × 49 RRAM array. Therefore, these findings suggest that Au/Gr/$WS_2$/Au is better suited for high-density RRAM arrays. The schematic of the purposed crossbar array structure and fabricated device is presented in Figure 4b.

### 4.2. Capacitance−Voltage (C−V) Measurements.

To further understand the resistive switching mechanism in ReRAM devices, C−V measurements were performed in a DC cyclic sweep mode at a 1 MHz constant frequency for graphene, Au/Gr/$MoS_2$/Au, and Au/Gr/$WS_2$/Au as shown in Figure 5a. The border traps calculated for Au/Gr/$WS_2$/Au and Au/Gr/$MoS_2$/Au in LRS are 3× $10^{10}$ $cm^{-2}$ and 1 × $10^{10}$ $cm^{-2}$, which increased to 6× $10^{10}$ and 4× $10^{10}$ $cm^{-2}$ in HRS, respectively.[64−66] In the Au/Gr/$WS_2$/Au ReRAM device, the intrinsic presence of a high Schottky barrier of 0.69 eV suppresses the carriers in the reverse direction, leading to an asymmetric self-rectifying behavior. The extent of the Schottky barrier modification can be inferred from the potential window width of the C−V hysteresis curve. A wider potential window indicates that the barrier is being modified over a broader voltage range, which may indicate that the high effective Schottky barrier height allows for effective regulation of the resistive switching process. The detailed switching mechanism is discussed in Figure 5b.

The energy band diagram assists in clarifying the switching mechanism in ReRAM devices, which entails the migration of charge carriers (often electrons) under the appliance of varying applied potentials. Figure 5b(i−v) extensively explains the switching behavior of the Au/Gr/$WS_2$/Au ReRAM device. Figure 5b(i) presents the energy band diagram of the fabricated device with respect to the vacuum level. Just after the formation of heterostructures, an equilibrium is established due to variation in the Fermi levels of the individual material, which induces the migration of electrons across the interface as shown in Figure 5b(ii). From Figure 5b(iii), initially, when the forward voltage (less than the set voltage) is applied, the electrons from the top electrode start to migrate toward $WS_2$ through the field emission process, but due to their limited energies, they are unable to cross over the barrier. Additionally, the trapped states at the Gr/$WS_2$ interface with energies near the Fermi level make it easier for electron transfer by lowering the barrier height at the junction. The enhanced thermionic emission by increasing voltage up to the set value forced the carriers to cross over the barrier by forming a conductive path in $WS_2$, which switched the device into an LRS state as shown in Figure 5b(iv). By reversing the polarity of applied voltage, modulation of LRS to HRS occurs by releasing trapped carriers in conjunction with increased Schottky barrier height, depending on the magnitude of applied voltage as presented in Figure 5b(v). The asymmetric nature of the Au/Gr/$WS_2$/ Au current−voltage (I−V) graph and self-rectifying behavior refer to the elevated effective Schottky barrier height. The Au/ Gr/$MoS_2$/Au device exhibits only bipolar resistive switching with no rectifying behavior. The junction between Au/$MoS_2$ is highly ohmic, as the work function of multilayers $MoS_2$ varies from 5.1 to 5.3 eV exactly matching with the work function of as-deposited Au electrode (5.1 eV), which implies that the switching behavior is purely controlled by Gr/$MoS_2$ interface junction[67,68]

## 5. CONDUCTION MECHANISM

The Schottky emission model is best suited to further examine the real conduction mechanism. The log scale current−voltage (I−V) graph was plotted for Au/Gr/$MoS_2$/Au and Au/Gr/ $WS_2$/Au as shown in Figure 5c,d. In both devices, the slope in the HRS at low voltage is approximately 1, which satisfies the Ohm's law ($I \propto V^1$). In this region, current increases linearly with voltage as electrons from the top electrode are initially injected into

semiconducting $WS_2$ via the field emission process. When the applied voltage is further increased, the value of the slope is approximately equal to 2, and the relation between voltage and current is ($I \propto V^2$), which is in great agreement with the space charge limited conduction (SCLC) mechanism.[69,70] At this applied voltage, electrons approached toward Gr/$WS_2$ junction and accumulated at the interface by forming a concentrated space charge region. As the voltage is increased further up to the SET value, allowing these carriers to move freely and the formation of a conduction channel switches the device from HRS to LRS. The LRS of both devices follow Ohm's law and satisfy the linear ($I \propto V^1$) relation with a slope equal to 1. When the polarity of the applied voltage is swept in reverse, the formation of a high Schottky barrier at the Gr/$WS_2$ and $WS_2$/Au interface impedes the flow of carriers to effectively switch the device back into HRS. Importantly, the Au/Gr/$MoS_2$/Au curve has a comparatively large area as compared to Au/Gr/$WS_2$/Au as shown in Figure 5c,d. It is owing to the free motion of carriers both in forward and reverse directions in Au/Gr/$MoS_2$/Au, while in Au/Gr/$WS_2$/Au the carriers are suppressed in the negatively biased region due to an increase in effective Schottky barrier height.

## 6. CONCLUSION

In summary, we highlighted the nature of the graphene heterostructure with TMDCs and investigated the resistive switching mechanism while keeping the Gr/TMDC heterostructure as an active channel. Both the Au/Gr/$MoS_2$/Au and Au/Gr/$WS_2$/Au devices displayed resistive switching behavior with a high HRS/LRS (on/off) ratio of $\sim 10^3$, endurance stability after $\sim 2 \times 10^2$ cycles, and retained the states after $\sim 10^4$ s. In addition, an interesting self-rectifying behavior was observed in the Au/Gr/$WS_2$/Au device, which eliminates crosstalk phenomena up to 48 × 49 arrays while reading operation. The CV measurements explained the insightswitching phenomena along with a detailed conduction mechanism. A high HRS/LRS ratio and self-rectifying behavior in Au/Gr/$WS_2$/Au prove it is the best candidate for dense crossbar arrays in NVM ReRAM devices to minimize the sneak current.

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**Notes**

The authors declare no competing financial interest.

## ACKNOWLEDGMENTS

The work was funded by the Higher Education Commission of Pakistan through NRPU # 13858, PSF-MSRT/Eng/CCOMSATS-01 and PSF/NSFC-IV/ENG/P-VU (24). A.A. is also thankful to CNR, Italy for funding during postdoctoral research work at TASC lab, Trieste Italy.

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