

Replacing Doping in Nano-Silicon: Ultimate Miniaturization, Energy Efficiency, and Cryo-Functionality

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ABSTRACT: Hard entropy limits of impurity doping prevent further miniaturization of low nanoscale silicon-based very large scale integration (VLSI) devices, thereby obstructing the path toward more energy-efficient VLSI designs with higher yield in compute power. As demonstrated here by synchrotron UV photoelectron spectroscopy (UPS) and X-ray absorption spectroscopy in total fluorescence yield mode (XAS-TFY), intrinsic Si at the bottom of the nanoscale (i-nano-Si) turns into strong p- or n-Si by embedding in silicon nitride (Si_3N_4) or silicon dioxide (SiO_2), respectively. The associated Nanoscale Electronic Structure Shift Induced by Anions at Surfaces (NESSIAS) creates a p/n junction in i-nano-Si by the quantum-chemical impact of Si_3N_4 - vs SiO_2 -coating, providing energy landscapes to accumulate electrons (holes) when SiO_2 - (Si_3N_4 -) coated, with free charge carriers provided by metallic interconnects. Hybrid density functional theory (h-DFT) calculations demonstrate Si NWire FETs with physical gate lengths down to 3 nm, while the electronic structure remains stable under carrier injection. A mesoscopic band model derived from synchrotron characterization data on ultrathin embedded Si nanowells (NWells), and from h-DFT confirms and further explains the NESSIAS impact to generate p/n homojunctions in i-nano-Si. Presenting a paradigm shift for Si-based VLSI, NESSIAS removes miniaturization limits, achieves faster charge carrier transport with massive reductions of energy demand and associated heat generation as required for ultralow power VLSI, and enables full cryo-functionality for quantum computing.

KEYWORDS: intrinsic nanosilicon, VLSI, p/n junction, ultralow power, cryo-electronics, FET

INTRODUCTION

Impurity doping¹ of silicon (Si) has been key to integrated circuit (IC) design since its inception in 1959.² Yet, what once enabled IC manufacturing has turned into an obstacle for Si-based very large scale integration (VLSI).³ Further device miniaturization of fin- and nanowire- (NWire-) field effect transistors (FETs) is prevented by dopant out-diffusion,⁴ self-purification,^{5,6} dopant clustering,⁷ and dopant inactivation by electrostatic screening.⁸ In addition, inelastic scattering induced by impurity dopants converts a considerable share of the electric energy provided to a chip into waste heat, yielding to low energy efficiency and thermal problems. Quantum computing suffers from thermal bridging of metal interconnects to qubits, with their control electronics working at substantially higher temperature where dopants can be ionized, or alternatively require much higher current densities; both present serious cooling issues.⁹ These seemingly unrelated issues can be addressed jointly if a dopant-free principle is found to introduce electron- and hole-dominated conductivity in intrinsic silicon at the bottom of the nanoscale (i-nano-Si).

Here, direct experimental and theoretical evidence is reported on the Nanoscopic Electronic Structure Shift Induced

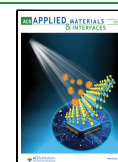
by Anions at Surfaces (NESSIAS) which pushes the electronic structure of i-nano-Si to higher vs lower binding energies for Si_3N_4 - vs SiO_2 -coating, whereby the electronic charge transfer from Si into SiO_2 vs Si_3N_4 differs by a mere 1%.¹⁰ When coated with Si_3N_4 , i-nano-Si goes devoid of free electrons, becoming perceptible to positive charge carriers (holes), thus turning into p-Si, while i-nano-Si coated with SiO_2 attracts free electrons, turning into n-Si. Instead of dopants providing free charge carriers *in situ*, the NESSIAS provides a suitable energy landscape^{10–12} to attract the respective carrier type *ex-situ*, e.g., from a metal electrode with matching Fermi energy to the i-nano-Si volume with respective coating. The quantum-chemical nature of nitrogen (N) vs oxygen (O) in the form of Si_3N_4 vs SiO_2 covering i-nano-Si is at the heart of the NESSIAS effect.¹⁰

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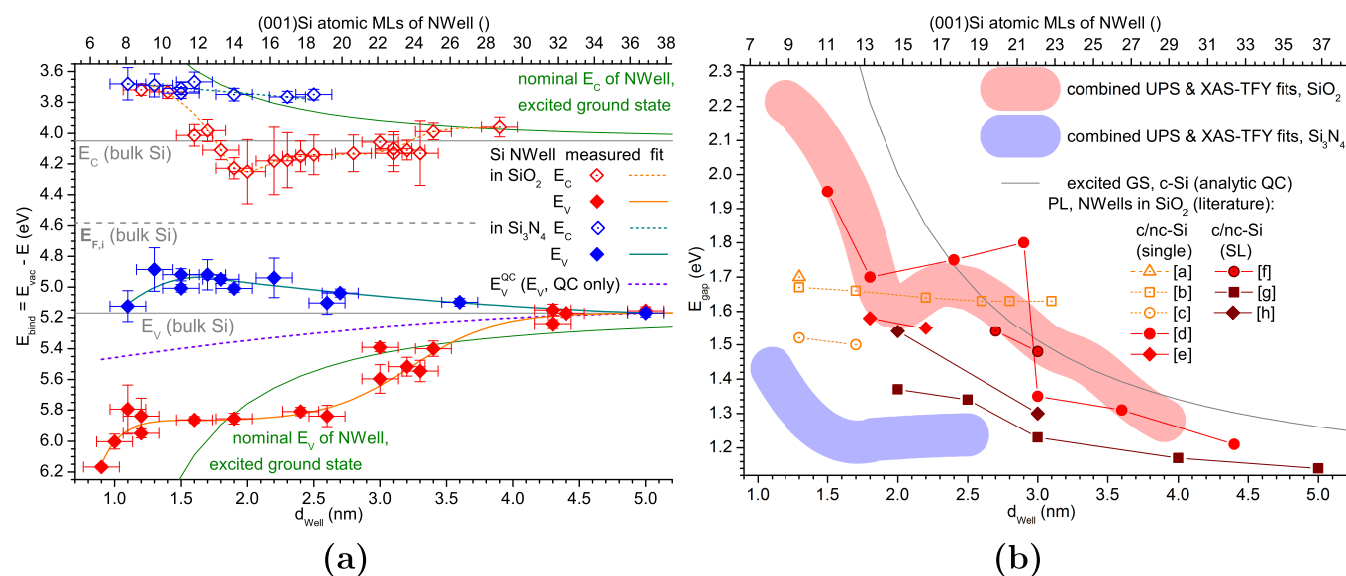


Figure 1. Synchrotron data: (a) UPS for E_V (filled symbols), XAS-TFY for E_C (empty symbols) of Si NWells over their thickness d_{Well} . Energies shown relative to E_{vac} ; blue (red) symbols refer to Si_3N_4 –(SiO_2 –) embedding. Error bars show standard deviations in E and d_{Well} (Supporting Information, Table S1). Full (dashed) dark cyan and orange lines show least-squares residual (LSR) fits to E_V (E_C) of NWells embedded in Si_3N_4 and SiO_2 , respectively. Thin gray lines show band edges of bulk Si, gray dashed line shows the Fermi energy of intrinsic Si $E_{\text{F,i}}$. Dashed violet line shows E_V by QC only; E_V^{QC} (Supporting Information, Section IAS). Green lines show E_V , E_C of NWell for photon absorption (unrelaxed excited state) as per standard analytic theory.⁵³ (b) Plot of fundamental bandgap energy E_{gap} from the literature as a function of NWell thickness d_{Well} using photoluminescence (PL), and E_{gap} (d_{Well}) as derived from UPS and XAS-TFY, using the respective LSR fitting functions. Lines between symbols are a guide to the eye only. NWells consist of single crystalline/nanocrystalline (c-/nc-) Si (red symbols) or of c-/nc-Si NWell superlattices (SLs, brown symbols); symbol of brown circle with red filling refers to SL with very thick SiO_2 barriers, effectively behaving like a single NWell. Values of single c-/nc-Si NWells in orange without filling originate from radiative interface defects⁵⁴ which becomes apparent by their weak dependence on d_{Well} . Thick faint red (blue) lines show E_{gap} for SiO_2 –(Si_3N_4 –) embedded Si NWells as derived from data of graph (a). The faint gray line shows the NWell gap for photon absorption (incl. exciton binding energy, excl. lattice relaxation) as per analytic theory from text books.⁵³ References: 54 = [a], 55 = [b], 56 = [c], 57 = [d], 58 = [e], 59 = [f], 60 = [g], 61 = [h].

As already shown,^{10–12} no existing effect such as interface dipoles,¹³ the pushback or pillow effect,¹⁴ or leaking electron wave functions from the adjacent dielectric nor quantum confinement (QC) can explain such band offsets. Synchrotron data assembled on Si NWell structures over ten beamtimes (Figure 1) show, in compound with a highly optimized sample preparation¹⁵ and {001}-SOI being thinned down to the respective NWell thickness, that all SOI-based samples have excellent interfaces to the Si-Well. Thereby, interface defect densities are way too low to interfere with the NESSIAS effect which tackles the electronic structure of Si-Wells via all interface bonds ($1.36 \times 10^{15} \text{ cm}^{-2}$ for {001}Si interfaces),¹⁶ thus outrunning interface defect densities at plain {001} Si interfaces ($5 \times 10^{11} \text{ cm}^{-2}$)¹⁷ by a factor of ca. 3×10^4 . In analogy to conventional Si electronic devices, H-passivation anneals have a positive influence on the electronic impact of the NESSIAS by decreasing the interface trap state density about 40-fold to ca. $1.5 \times 10^{10} \text{ cm}^{-2}$.¹⁷ While significant strain exerted onto Si NWells by the embedding dielectric could be another source of electronic structure change, our data clearly miss such a signature, cf. Figure 1. Thin Si_3N_4 films deposited by rapid thermal chemical vapor deposition (RTCVD) were shown to have a Young's modulus of $Y = 150\text{--}200 \text{ GPa}$.¹⁸ Thin SiO_2 films produced by dry oxidation yielded $Y = 50\text{--}67 \text{ GPa}$.^{19,20} Therefore, any impact of stress is primarily expected for Si_3N_4 -embedded Si NWells, contrasting with Figure 1 where the shift of the electronic structure for Si_3N_4 -embedded Si NWells is smoother and less pronounced as compared to their SiO_2 -embedded counterparts, *en par* with quantum-chemical considerations.¹⁰ In addition, no structural damage or

even notable deviations of the Si lattice constant was found when investigating 1.1 nm thin Si NWells embedded in Si_3N_4 (Figure 2b, and Supporting Information, Section IC).

The complete absence of dopants to induce p- or n-type characteristics in i-nano-Si result in a considerable decrease of inelastic carrier scattering rates and nonradiative recombination rates. Strongly decreased inelastic carrier scattering rates yield to higher carrier mobilities, considerably lower energy demand and heat generation, offering opportunities to further increase VLSI clock frequencies at ultralow power. The absence of dopants also results in a much lower nonradiative recombination rate which is key for on-chip ultrabroadband high-gain optical interconnects in Si VLSI.²¹ Without dopants to be ionized, the strong preference of i-nano-Si for the respective carrier type induced by the dielectric coating works down to virtually absolute zero temperature, rendering the NESSIAS effect to be key for peripheral electronics in quantum computing. The absence of dopants eliminates spatial limitations due to dopant out-diffusion, failed activation, and clustering, whereby the miniaturization limit expressed by the physical gate length in VLSI of currently 18 nm for the most advanced 5 nm technology node²² can be reduced prospectively by a factor of up to ca. 36.

While this work focuses exclusively on the various fundamental aspects of the NESSIAS effect of the Si_3N_4 /i-nano-Si/ SiO_2 system, it may be of interest that other weak polar and covalent semiconductors such as GaSb, BSB, or GaAs are likely suitable materials as well for exploiting the NESSIAS effect to a full extent. This would require thin NWells or NWires with a diameter of $\leq 6 \text{ nm}$ ¹² for GaSb as an

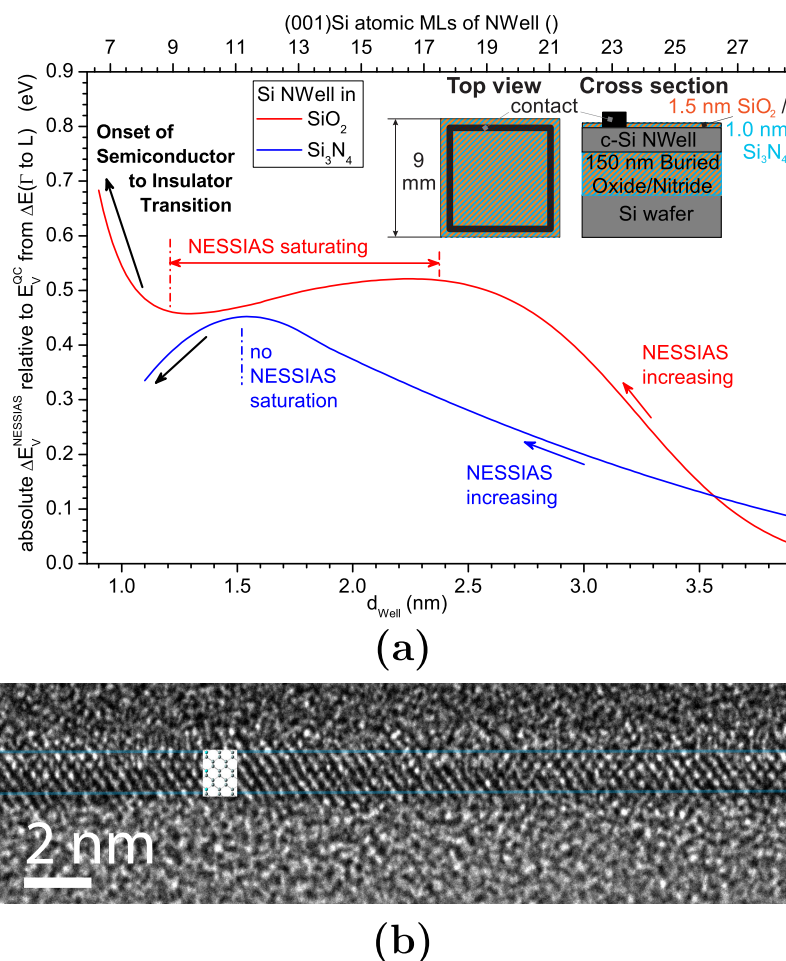


Figure 2. Evolution of NESSIAS with NWell thickness, sample structure: Absolute deviation of $E_V^{NESSIAS}$ from $E_V^{QC}(d_{Well})$ – purple dashed line in Figure 1(a) – over d_{Well} . NESSIAS impact for SiO_2 -embedding is stronger vs Si_3N_4 -embedding, saturating from $d_{Well} \approx 2.4$ nm; semiconductor–insulator transition occurs at $d_{Well} \approx 1.20 \pm 0.14$ nm. A weaker NESSIAS impact for Si_3N_4 -embedding increases monotonically up to the onset of NWell semiconductor–insulator transition at $d_{Well} \approx 1.50 \pm 0.14$ nm. Inset shows sample structure, with c-Si NWell ((001)Si on insulator – SOI) described by d_{Well} . (b) High resolution transmission electron microscope image, 1.1 nm thick Si_3N_4 -embedded Si NWell (sample Si_11_1; Supporting Information, Section IC). Inset shows positions of Si atoms. More high resolution TEM images of ultrathin Si NWells embedded in SiO_2 or Si_3N_4 as part of an ongoing investigation into the NESSIAS have been shown elsewhere.^{10,12,41}

example, and exclusive {110} interface facets to remove interface dipoles as a possible degrading effect on device applications. Such nanowires were already utilized in device prototypes,²³ though not in the size range of NWires mentioned above as yet.

METHODS

Sample Processing. After determining the Deal-Grove parameters²⁴ for the furnace oxidation of silicon-on-insulator (SOI) samples, the SOI crystalline Si (c-Si) layers (p-type, 1 Ω cm) on Si wafers with 145 nm buried SiO_2 (BOx) were oxidized down to a thickness of 1.9 to 6.0 nm. The SiO_2 was removed by etching in a buffered oxide etch (BOE; 1 wt % HF buffered with NH_4F), followed by a self-limiting oxidation in 68 wt % HNO_3 at 120 $^\circ$ C, yielding a 0.9 to 5.0 nm thick Si-NWell with 1.4 nm SiO_2 capping. A lateral metal contact frame was processed on the front surface by photolithographical structuring, wet-chemical etching in BOE for opening the top SiO_2 layer and thermal evaporation of 300 nm Al, followed by a lift-off in acetone. The Si reference samples¹⁵ were contacted directly on their front surface. Immediately after processing, samples were measured by Mueller matrix ellipsometry to obtain the respective NWell thickness, followed instantly by coating with photo resist to prevent oxidation in air. Resist was removed just prior to sample mounting at the beamline, the latter carried out under an N_2 shower to prevent oxidation in air.

Si reference samples consisted of (001)-Si wafer (Sb-doped *n*-type, 0.01 Ω cm) which were treated with a BOE immediately before sample mounting under a N_2 gas flow with swift loading into the ultrahigh vacuum (UHV) annealing chamber. A detailed description of the processing sequence is given in.¹⁵

Si-NWells in Si_3N_4 were processed in analogy to the ones in SiO_2 , using the same SOI wafers as starting point. The SOI was thinned down to a remanent Si device layer which was 1.5 to 2.0 nm thicker than the final NWell thickness, accommodating for Si consumption during the growth of Si_3N_4 . Next, the SiO_2 capping was removed with BOE immediately before growing 3 nm of Si_3N_4 in an ammonia atmosphere by rapid thermal nitridation (RTN). Afterward, 20 nm of Si_3N_4 and 80 nm of SiO_2 were deposited by plasma enhanced chemical vapor deposition, followed by chemical mechanical polishing of the SiO_2 layer. After an RCA clean,²⁵ the samples were bonded to a Si sample²⁶ covered by SiO_2 of ca. 1.5 nm thickness which was grown by an RCA-SC2 step. The original Si substrate of the SOI samples was etched back using a cyclic deep reactive ion etching process based on passivation with C_4F_8 and etching with SF_6 . The BOx served as a stopping layer and was subsequently removed by a BOE immediately before growing 1 nm of Si_3N_4 onto the remnant SOI constituting the NWell by RTN in ammonia atmosphere. Contacts to the NWells were fabricated by photolithography, etching the Si_3N_4 with 1 wt % hydrofluoric acid and deposition of 300 nm Al.

Characterization. Synchrotron UV Photoelectron Spectroscopy (UPS). All samples were subject to a UHV anneal for 60 min at 500 K to desorb water and air-related species from the sample surface prior to measurements. Synchrotron UPS measurements were realized at the BaDElPh beamline²⁷ at the Elettra synchrotron radiation facility in Trieste, Italy. NWells samples were excited with photon energies of 8.9 eV for test purposes, then initially 8.7 eV and later routinely with 8.0 eV, and a photon flux of ca. $2 \times 10^{12} \text{ s}^{-1}$. The incident angle of the UV beam onto the sample was 50° with respect to the sample surface normal, the excited electrons were collected with an electron analyzer along the normal vector of the sample surface. Energy calibration of the UPS was realized using a tantalum (Ta) stripe in electrical contact to the sample as work function reference.

X-ray Absorption Spectroscopy Measurements in Total Fluorescence Yield (XAS-TFY). All samples were subject to a UHV anneal for 60 min at 500 K to desorb water and air-related species from the sample surface prior to measurements. Synchrotron XAS-TFY measurements were carried out at the BACH CNR beamline^{28,29} at the Elettra synchrotron radiation facility in Trieste, Italy. The photon energy scale has been calibrated using the energy position of the Si L3-edge (99.6 eV) measured on a reference (001)-Si wafer. A multitude of spectra was recorded per sample to obtain the data ensemble required for statistical postprocessing. The energy resolution of the monochromator was approximately 23 meV.

Mueller Matrix Ellipsometry. The thickness of Si-NWells and its adjacent SiO_2 or Si_3N_4 layers of all samples submitted to synchrotron characterization were measured using an ACCURION nanofilm ep4se ellipsometer³⁰ which utilizes a Mueller matrix approach.^{31–33}

Transmission Electron Microscopy (TEM). Additional thickness measurements of the Si NWells were realized by TEM on selected samples to confirm and/or calibrate ellipsometry measurements, see e.g., Figure 9 in ref 15, Figure 5(b) in ref 10, or Figure 1(b) in ref 12. Here, focus is set on a sample featuring a Si NWell with minimum thickness characterized by synchrotron UPS; sample SiN_11_1. Sample SiN_11_1 was capped with a protective ca. 50 nm thick SiO_2 layer and covered with a 20 nm thick gold (Au) layer on top to facilitate the preparation of cross sections by the lift-out technique.^{34,35} To this end, the focused ion beam (FIB) milling was applied, using a Helios NanoLab 600i from Thermo Fisher Scientific. The TEM characterizations were carried out in a JEM 2200FS (JEOL Ltd., Japan), which was equipped with a field emission gun operating at 200 kV, a CESCOR probe aberration corrector (CEOS GmbH, Germany), an ultrahigh resolution objective lens ($C_s = 0.5 \text{ mm}$), an in-column energy filter (Ω -filter), and a highly sensitive $2k \times 2k$ CCD camera (Gatan Inc.). The Ω -filter was used to filter inelastically scattered electrons, thereby improving the quality of the TEM images.

Density Functional Theory (DFT) Calculations. Real space calculations (nonperiodic boundary conditions) were carried out with a molecular orbital basis set (MO-BS) and Hartree–Fock (HF)/hybrid-DFT (h-DFT) methods, employing the GAUSSIAN09 program package³⁶ with the GaussView program³⁷ for visualization. Initially, the MO-BS wave function ensemble was tested and optimized for describing the energy minimum of the system (variational principle; stable = opt) with the HF method.^{38–40} Exact exchange interaction inherent to HF is crucial in obtaining accurate bond geometries (Supporting Information in⁴¹). The Gaussian type 3–21G MO-BS⁴² was utilized. This HF/3–21G route was used for the structural optimization of approximants to obtain their most stable configuration (maximum integral over all bond energies). Root mean square (RMS) and peak force convergence limits were $0.98 \text{ meV } \text{\AA}^{-1}$ and $58.1 \text{ meV } \text{\AA}^{-1}$, (19 and $1129 \mu\text{Ha}/a_{\text{B,0}}$), respectively. An own 'bracket' code⁴³ was applied which intercepts the numerical noise during structural optimization, restarting the optimization with the most recent geometry. This 'bracket' code slows down optimization jobs by 6 to 8%, but enables GAUSSIAN09 to successfully optimize approximants with up to ca. 1,500 atoms for a HF/3–21G computation route. Optimized geometries were used to calculate their electronic structure by testing and optimizing the MO-BS wave function ensemble with the nonlocal h-DF B3LYP.^{44–46} Previous investigations demonstrated that the Heyd-Scuseria-Ernzerhof hybrid

DF^{47,48} with its parameters from 2006 (HSE06,⁴⁹) arrives at very similar results (Supporting Information in¹⁰). As MO-BS, the Gaussian type 6–31G(d) MO-BS was used which contains d-polarization functions (B3LYP/6–31G(d)).⁵⁰ For all calculations, tight convergence criteria were set to the self-consistent field routine and no symmetry constraints to MOs were applied. Ultrafine integration grids were used throughout. Detailed accuracy assessments can be found in the Supporting Information of refs 41,51,52.

Mesoscopic Band Picture of a nano-Si Type II Homo Junction Due to the NESSIAS Effect. Data from h-DFT was used to derive the mesoscopic band structure along the length axis of the Si NWell induced by the NESSIAS effect. The Supporting Information contains a detailed discussion and derivation thereof.

RESULTS AND DISCUSSION

Characterization. Experimental work was carried out on ultrathin Si NWells embedded in SiO_2 or in Si_3N_4 (Figure 2(a) [inset] and (b)) to detect the energies of the valence band (VB) and the conduction band (CB) edges E_V and E_C , respectively. Synchrotron ultraviolet photoelectron spectroscopy (UPS) was applied to detect VB edge features along with E_V and the adjacent Van Hove singularity (Supporting Information, section IA). Synchrotron X-ray absorption spectroscopy in the total fluorescence yield mode (XAS-TFY) was utilized to detect E_C (Supporting Information, section IB).

These characterization results demonstrate a significant downshift of the entire electronic structure of SiO_2 -embedded Si NWells with thicknesses of $d_{\text{Well}} \leq 3.3 \text{ nm}$ (Figure 1(a)). Data for E_C show that a minimum exists at $d_{\text{Well}} \approx 2.0 \text{ nm}$, rendering SiO_2 -embedded Si NWells to be prone to electron injection from metallic electrodes, turning the Si NWell highly electron-conductive. Interestingly, qualitative deviations of the electronic structure of small SiO_2 -embedded Si nanocrystals from analytic quantum-mechanical values were briefly reported in 2006,⁶² though without providing an explanation or a more detailed follow-up. In contrast, Si_3N_4 -embedded Si NWells experience an upshift of the electronic structure with decreasing d_{Well} , rendering their electronic structure to push electrons onto metallic electrodes, becoming hole-conductive in the process. Figure 1(a) clearly shows that $E_C(d_{\text{Well}})$ and $E_V(d_{\text{Well}})$ as per textbook quantum confinement (QC) model⁵³ deviate significantly from measured values, though E_V can be described by the quantum-chemical NESSIAS model.¹⁰ Moreover, a notable drop of E_V to higher E_{bind} can be seen for $d_{\text{Well}} \leq 1.5 \text{ nm}$ for Si_3N_4 -, and for $d_{\text{Well}} \leq 1.2 \text{ nm}$ for SiO_2 -embedding. Arguably (Supporting Information, section IA4), this drop in E_V presents the onset of a semiconductor–insulator transition. Such NWells appear to undergo an electronic transition to the respective dielectric, effectively starting to behave like a subnitride (-oxide) SiN_x (SiO_x), although 9 ML (SiO_2 -embedding) to 11 ML (Si_3N_4 -embedding) of (001)Si are physically present. The appearance of this transition at thicker NWells, yet to a lesser degree for Si_3N_4 -embedding vs SiO_2 -embedding is in accord with NESSIAS theory.¹⁰

Combining the experimental data from UPS and XAS-TFY, the fundamental bandgap energy E_{gap} of Si nanowells (NWells) embedded in SiO_2 vs Si_3N_4 can be derived. Such data are shown in Figure 1(b), using the least-squares residual (LSR) fits from Figure 1(a), combined with NWell bandgap data published in the literature. The E_{gap} data of this work are in accord with other experimental findings, provided the Si NWells are isolated from each other to an extent where they

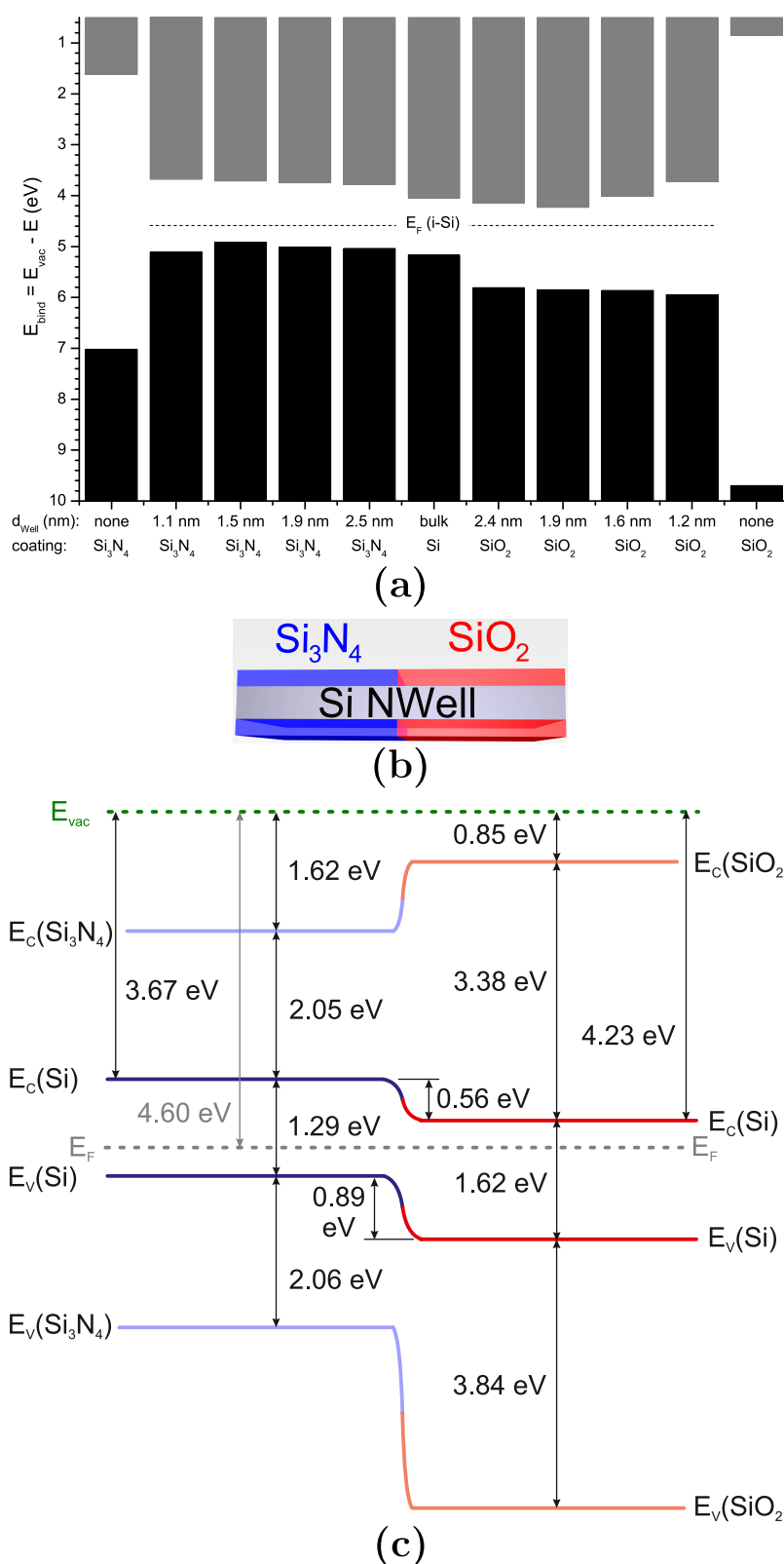


Figure 3. NWell band edge data and scheme: (a) Fundamental gap with CBs (gray) and VBs (black) over d_{well} from Figure 1(a). Center bar shows bulk i-Si, with NWell systems in Si_3N_4 -coating to the left, and in SiO_2 -coating to the right. Values of bulk Si_3N_4 and bulk SiO_2 set limits for $d_{\text{well}} \rightarrow 0$ at outer edges. The dashed line shows the intrinsic Fermi energy of bulk i-Si $E_{\text{F},i}$. (b) Scheme of $\text{Si}_3\text{N}_4/\text{SiO}_2$ -embedded Si NWell to illustrate the (c) full electronic band scheme of the NESSIAS-induced junction in Si NWell for $d_{\text{well}} = 1.9$ nm, cf. graph (a). Additional data for band edges E_{C} , E_{V} of SiO_2 and Si_3N_4 were calculated with experimental data^{65–72} and Supporting Information of refs 41. Dark blue (red) lines show band edges E_{C} , E_{V} of the Si NWell in Si_3N_4 (SiO_2), faint blue (red) lines show band edges E_{C} , E_{V} of the Si_3N_4 (SiO_2), the gray dashed line shows the Fermi energy E_{F} , and the dashed dark green line shows the vacuum level E_{vac} (more details in Supporting Information, Section III).

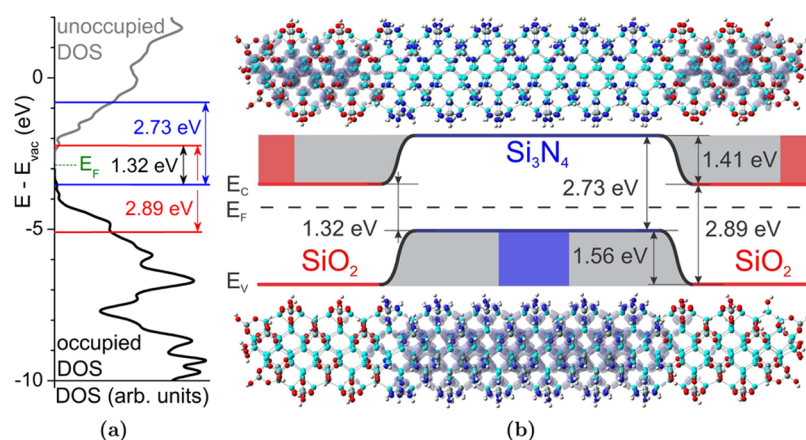


Figure 4. h-DFT results, neutral NWire: (a) Electronic DOS, neutral Si_{395} NWire ($d_{\text{Wire}} = 1.2$ nm, $l_{\text{Wire}} = 8.8$ nm), embedded in 2 ML SiO_2 (Si_3N_4) in outer quartile sections (in center section); energies shown relative to E_{vac} . Red (blue) lines present VB and CB edges of NWire sections embedded in SiO_2 (Si_3N_4), green dotted line shows Fermi energy E_F .⁶⁶ (b) Approximant of Si NWire (cyan atoms) with 2 ML embedding (O atoms are red, N atoms blue, Si in dielectrics gray, H atoms white). Iso-density plots, electronic DOS of 0.36 e/nm^3 per state; CB states reside in the SiO_2 -coated NWire sections (top), and VB states reside in the Si_3N_4 -coated NWire section (bottom). The junction width is ca. 1.0 nm. Center graph shows the resulting band diagram of the electronic structure of the Si NWire. Red (blue) bars show energy range of CB (VB) offsets, corresponding DOS given by iso-density plots shown above (red bars) and below (blue bar) band scheme.

behave like single NWells (no significant inter-NWell coupling of electronic states). As pointed out,⁵⁴ many bandgap data measured by photoluminescence (PL) are not originating from Si NWells, but from radiative defects located at NWell interfaces or within SiO_2 . Such bandgap values can be recognized by their weak dependence on d_{Well} , cf. orange symbols in Figure 1(b). For completeness, PL data of Si NWell superlattices (SLs) were included as well, showing significant inter-NWell overlap of electronic states through ultrathin SiO_2 barriers. As expected from the relaxed QC conditions, such bandgap energies are somewhat lower as compared to individual or well isolated Si NWells. The 'kink' feature of E_{gap} between $d_{\text{Well}} \approx 3$ to 2 nm is reproduced by literature data of single NWell samples with SiO_2 -embedding, and to some extent also by Si NWell SLs, provided there are enough data points over d_{Well} to detect the feature. As expected, inter-NWell coupling in SLs diminishes this 'kink' feature somewhat. For Si NWells embedded in Si_3N_4 , no reliable PL data exist in the literature. In analogy to Si nanocrystals (NCs) embedded in Si_3N_4 , a discrimination of the PL signal for *in situ* vs *ex-situ* NWell states is not possible due to the high density and strong radiative recombination rate of defects in Si_3N_4 .⁶³

Since E_V shifts to higher E_{bind} due to QC, the energy difference between E_V and the adjacent Van Hove singularity of the Si NWells was exploited to estimate the evolution of $E_V(d_{\text{Well}})$ exclusively due to QC (Figure 1(a); Supporting Information, section IA 5). Thereby, the shift of E_V over d_{Well} can be separated into a partition due to QC only $-\Delta E_V^{\text{QC}}$ and another one due to NESSIAS only; $\Delta E_V^{\text{NESSIAS}} = \Delta E_V - \Delta E_V^{\text{QC}}$. Absolute values of $\Delta E_V^{\text{NESSIAS}}$ are shown in Figure 2(a) for Si NWells embedded in SiO_2 vs Si_3N_4 . The VB shift saturates due to the NESSIAS effect for $d_{\text{Well}} = 2.4$ to 1.2 nm for SiO_2 -embedding. For Si_3N_4 -embedding, the impact of NESSIAS onto the electronic structure of the Si NWell is weaker, but does not enter saturation. Above data allow to extract a NESSIAS impact length of $d_{\text{NESSIAS}} \approx 1.5$ nm, whereby $d_{\text{Well}} \approx 2.4$ to 1.8 nm is optimal for inducing a p/n junction. This value translates to Si NWire diameters of ca. 5 to 3 nm as a function of their interface orientation.^{12,64}

Summarizing results of Figure 1(a), a clear picture of the band structure of Si NWells is provided as a function of d_{Well} and their embedding dielectric (Figure 3). Clearly, the band offsets of bulk Si to the respective dielectric becomes more symmetric for Si NWells when d_{Well} decreases, again being in accord with their strong electron (hole) preference when embedded in SiO_2 (Si_3N_4). Above characterization results and NESSIAS theory¹⁰ demonstrate that a specific manipulation of the electronic structure of Si NWells and other Si nano volumes can be exploited to define the conductivity type in analogy to conventional impurity doping if electrons can be injected into or collected from metallic electrodes. The band diagram of the NESSIAS junction resembles a somewhat asymmetric type-II heterojunction (Figure 3(c) and Supporting Information, Section III). With nano-Si as the only semiconductor throughout a prospective electronic device, there are no band edge discontinuities. Carrier effective masses remain constant apart from stress exerted by the dielectric onto nano-Si. This effect is exploited by Si_3N_4 -spacers around gate electrodes in VLSI yield to a decrease in effective masses in the channel region,⁷³ resulting in higher carrier mobilities and faster response times of electronic devices (higher clock frequencies).

Electronic Structure Calculations. For investigating the impact of NESSIAS onto the electronic structure of i-nano-Si, *ab initio* material simulations were realized for an approximant containing a i-nano-Si NWire as typical for gate-all-around (GAA) NWire FETs.⁷⁴ Such a NWire with diameter $d_{\text{Wire}} = 1.2$ nm and length $l_{\text{Wire}} = 8.8$ nm, featuring embedding in 2 ML $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$, was calculated utilizing real-space hybrid density functional theory (h-DFT) for its electronic structure (Supporting Information, section II). Figure 4(a) shows that high band offsets exist between Si NWires sections coated with SiO_2 vs Si_3N_4 , confirming experimental data above. Spatial distributions of electronic eigenstates over energy are obtained within the Si NWire (Figure 4(b)), clearly showing that Si_3N_4 -(SiO_2 -) coated i-nano-Si becomes strongly hole- (electron-) dominated, thereby mimicking acceptor- (donor-) doping. The associated p/n junction has a lateral extension of ca. 1.0 nm, yielding to a minimum gate length of ca. 3 nm for a self-

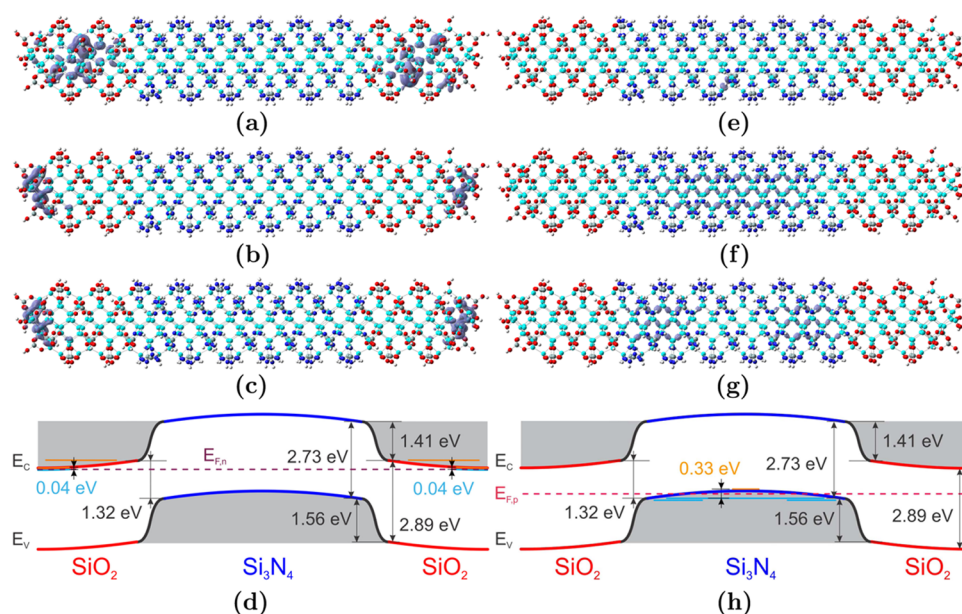


Figure 5. h-DFT results, charged NWire: Spatial distribution of electronic state of next-above lowest occupied molecular orbital (LUMO+1) (a), LUMO (b), and highest occupied MO (HOMO) (c), the latter taking up the extra negative charge in the Si₃₉₅ NWire (see Figure 4 for details) when charged with one electron. (d) Mesoscopic band scheme derived from the spatial distribution of above states, their eigen-energies, and the distances along the longitudinal axis of the Si NWire. Red (blue) lines present VB and CB edges of NWire sections embedded in SiO₂ (Si₃N₄), purple dotted line shows Fermi energy E_F .⁶⁶ Cyan lines show HOMO, orange lines show LUMO and LUMO+1 with decreasing binding energy (going upward). Spatial distribution of electronic state of LUMO (e), HOMO (f), and next-below HOMO (HOMO−1) (g), the first one taking up the extra positive charge in the Si₃₉₅ NWire (see Figure 4 for details) when charged with one hole. (h) Mesoscopic band scheme derived from the spatial distribution of above states, their eigen-energies, and the distances along the longitudinal axis of the Si NWire. Red dashed line shows Fermi energy E_F , orange line shows LUMO, cyan lines show HOMO and HOMO−1 with increasing binding energy (going downward). All iso-density plots have an iso-density surface of 0.36 e/nm^3 . Further details can be found in Supporting Information, sections II and III.

blocking GAA-NWire FET, and an associated miniaturization factor per square of up to ca. 36.

Electronic properties of above device structures must be robust to carrier injection. To this end, the same approximant was used for injecting one electron or hole into the Si NWire. With 395 Si atoms forming the NWire, this single charge carrier amounts to a volume charge density of $\rho \approx 1.3 \times 10^{20} \text{ cm}^{-3}$,⁶⁶ likely rendering such small NWire FETs to be a device governed by a single charge carrier (Supporting Information, Section II B). Related data for the Si NWire approximant charged with one electron ($q = -1e$) or with one hole ($q = +1e$) are shown in Figure 5. From the respective frontier electronic states of the Si NWire, it becomes apparent that the Fermi energy E_F is located very near E_C ($q = -1e$), or E_V ($q = +1e$), reflecting the high values of ρ mentioned above. The location of the highest occupied molecular orbital (HOMO) and the lowest unoccupied MO (LUMO) as frontier electronic states for the NWire with $q = -1e$ are located at the far ends of its SiO₂-coated sections (Figure 5(e)–(g)), with the next higher electronic state (LUMO+1) being located more toward the centers of the SiO₂-coated quartile sections of the NWire. When looking at the location of frontier electronic states for the NWire with $q = +1e$ (Figure 5(a)–(c)), the LUMO is clearly located in the center of the Si₃N₄-coated section of the NWire, and states disperse further out toward the p/n junction when going to the HOMO and HOMO−1 state. Spatial locations of such frontier electronic states are in full agreement with a band bending model due to an extrinsic charge as shown in Figures 5(d) and (h). Hence, two completely different solid state descriptions – the molecular orbital picture obtained by h-DFT, and the band bending model from semiconductor

physics – arrive at the same electronic structure. The electronic structure of the NWire is robust against a rather massive charge injection of $\rho \approx 1 \times 10^{20} \text{ cm}^{-3}$ as the only minor changes if any occur in the electronic DOS around E_F (Supporting Information, section IIB).

Basic Concept of Si NWire FETs and CMOS Logic. A simplified band diagram of the NESSIAS-induced p/n junction in nano-i-Si with zero and small forward bias is shown in Figure 6(a). Apart from the zero gradient of E_{vac} when no bias is applied, the junction mimics a conventional p/n structure as obtained with impurity doping, although free charge carriers are sourced from metallic interconnects. Figure 6(b) shows the concept of an i-nano-Si NWire FET where the required conductivity type of drain, channel and source regions is accomplished by coating with SiO₂ (n-type) or Si₃N₄ (p-type). With the spatial limits due to impurity doping removed, such NWire FETs can be miniaturized significantly. One of the key features of a CMOS logic being implemented with the NESSIAS effect is the change in conductivity type in a FET. This change is achieved by swapping the dielectric coating between the regions of drain and source with the channel region as per Figure 6(c),(d). As all materials are Si-based and omnipresent in Si VLSI processing, the remaining challenge of implementation appears to be the structuring of such ultrasmall devices.

CONCLUSIONS

It was demonstrated in experiment and theory that the electronic structure of i-nano-Si shifts considerably to higher (lower) binding energies by coating with SiO₂ (Si₃N₄) as per NESSIAS effect, turning i-nano-Si into n-type (p-type) for

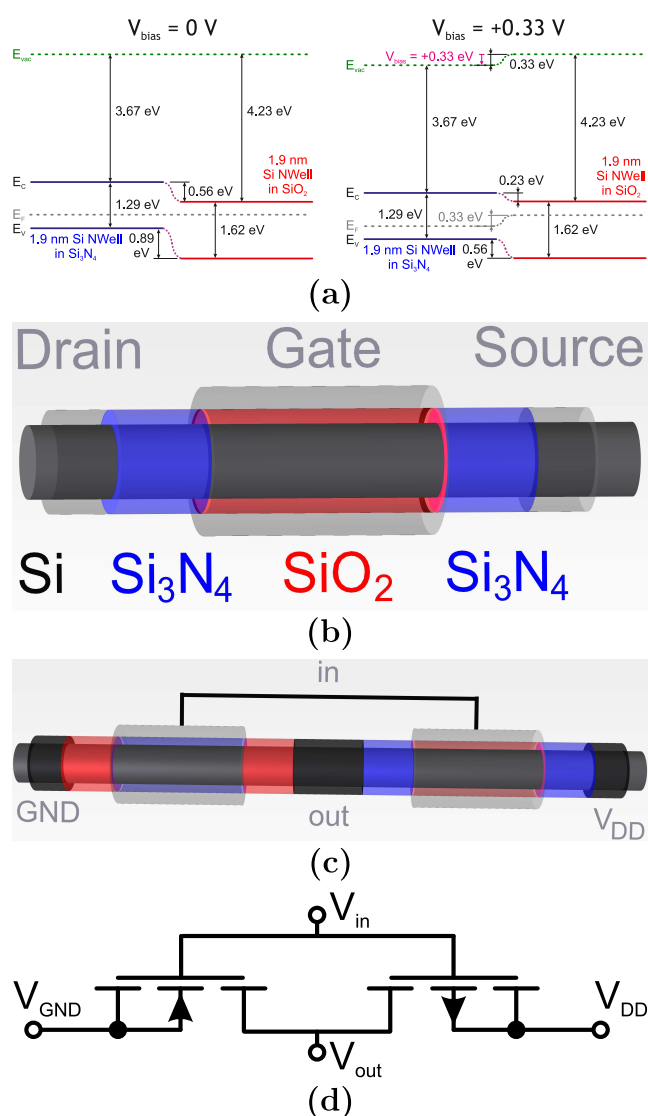


Figure 6. NESSIAS junction, Si NWire FET concept, associated CMOS logic: (a) Band alignment of NESSIAS junction resulting from synchrotron and h-DFT data under zero bias (left) and small forward bias (right), focusing on the i-nano-Si as active device volume. Values taken from UPS and XAS-TFY of samples with $d_{\text{Well}} = 1.9 \text{ nm}$, cf. Figure 3(a). (b) Si NWire with $\text{Si}_3\text{N}_4/\text{SiO}_2/\text{Si}_3\text{N}_4$ -coating, constituting a self-blocking p-channel FET (antipolar to FET in Figure 4), setting drain and source regions to be n-type, and channel region to be p-type. Total length of FET would be 10–12 nm. (c) Explanatory concept of CMOS logic inverter (logical NOT) implemented on one Si NWire exploiting the NESSIAS effect. The left FET connected to ground (GND) has n-type drain and source regions by SiO_2 -coating, and a p-type channel region due to Si_3N_4 -coating, rendering it to be a self-blocking n-channel FET in analogy to Figure 4. The right FET connected to the bias voltage (V_{DD}) has the same polarity as in (b). (d) Electronic device scheme describing NWire arrangement in (c).

SiO_2 - (Si_3N_4 -) embedding. The NESSIAS impact length of ca. 1.5 nm renders Si NWells of $\leq 3 \text{ nm}$ thickness, and Si NWires of $\leq 5 \text{ nm}$ diameter, to experience substantial energy shifts. The resulting energy landscape in i-nano-Si renders SiO_2 - (Si_3N_4 -) coated Si to be highly electron (hole) dominated, effectively behaving like strong n- (p-) type nano-Si by sourcing charge carriers from adjacent device electrodes. In addition, onsets of semiconductor-to-insulator transitions of Si NWells were detected by synchrotron UPS for ca. $\leq 9 \pm 1 \text{ ML}$

001-Si ($d_{\text{Well}} \leq 1.2 \pm 0.14 \text{ nm}$) for SiO_2 -embedding, and from $\leq 11 \pm 1 \text{ ML}$ 001-Si ($d_{\text{Well}} \leq 1.5 \pm 0.14 \text{ nm}$) for Si_3N_4 -embedding. Below such limits, the remaining Si MLs NWells start to show an electronic structure of the respective substoichiometric dielectric – SiO_x or SiN_x – while *physically* still presenting an extremely thin Si layer.

Large-scale h-DFT calculations showed the electronic structure of a 2 ML $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$ -coated Si NWire to be robust against electron or hole injection, demonstrating full electronic functionality for prospective devices which fully agree with a mesoscopic band scheme in semiconductor physics. The NESSIAS-induced p/n junction removes all disadvantages associated with Si impurity doping. Prospective devices have no lower temperature limit of functionality, have ionized dopants eliminated as inelastic scattering centers along with associated recombination centers, and have dopant out-diffusion and statistics issues removed, allowing for a ca. 36-fold areal miniaturization in VLSI. The NESSIAS for Si-based VLSI devices thus should enable cryo-functionality down to virtually 0 K, extremely low energy demand and operating voltages, associated ultralow heat generation, and optimum properties of on-chip ultrafast optical interconnects, using CMOS-processing compatible materials and preparation methods. Creating n- and p-channel FETs as required for CMOS logic is simply achieved by swapping the dielectric coating between drain and source with the channel region. With device structuring on such an ultrasmall scale being mastered, Moore's law for Si-based VLSI may not be as dead as it currently seems.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at <https://pubs.acs.org/doi/10.1021/acsami.5c08073>.

Detailed descriptions, results, and discussions of synchrotron UPS, XAS-TFY and TEM characterization, of the onset of the semiconductor-to-insulator transitions of Si NWells, of exploiting the VB substructure in synchrotron UPS measurements to estimate the VB shift exclusively due to quantum confinement, of h-DFT calculations of neutral and charged approximants, and the derivation of a quantitative band model of $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$ -embedded Si NWires from h-DFT data (PDF)

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Notes

The authors declare no competing financial interest.

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