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Side-Gate Modulation of Supercurrent in InSb Nanoflag-Based Josephson Junctions

Bianca Turini, Sedighe Salimian, Matteo Carrega, Federico Paolucci, Valentina Zannier, Lucia Sorba, and Stefan Heun**

InSb nanoflags, due to their intrinsic spin–orbit interactions, are an interesting platform in the study of planar Josephson junctions. Ballistic transport, combined with high transparency of the superconductor/semiconductor interfaces, is reported to lead to interesting phenomena such as the Josephson diode effect. The versatility offered by the planar geometry can be exploited to manipulate both carrier concentration and spin–orbit strength by electrical means. Herein, experimental results on InSb nanoflag-based Josephson junctions fabricated with side gates placed in close proximity to the junction are presented. It is shown that side gates can efficiently modulate the current through the junction, both in the dissipative and in dissipation-less regimes, similar to what is obtained with a conventional back gate. Furthermore, the side gates can be used to influence the Fraunhofer interference pattern induced by the presence of an external out-of-plane magnetic field.

1. Introduction

Hybrid superconductor/semiconductor devices have attracted a lot of interest in the last decades due to their potential applications in a wide range of fields, such as radiation sensing, quantum computing, particle detection, and telecommunications.[1–4] Among all, the pursuit of new topological states of matter[5–10] triggered intense research on strong spin–orbit semiconductors interfaced with superconductors. Progress in fabrication techniques has been achieved recently,[1,11–21] as well as more efficient models to describe proximity effects.[22–25] However, conclusive results on the emergence of nontrivial topological states are still lacking to date, although there has been some recent progress.[26–28]

In parallel, hybrid devices such as Josephson junctions (JJs) with a strong spin–orbit material as the normal channel constitute an interesting platform for nonreciprocal dissipation-less transport.[29–36] Indeed, in the presence of a finite magnetic field, the so-called Josephson diode effect has been demonstrated,[29,32] which is related to the simultaneous breaking of both inversion and time-reversal symmetry. These achievements opened interesting possibilities for future applications in low-power superconducting electronics. In this respect, it is thus important to inspect tools such as electrostatic gates that allow for easy and precise manipulation of the device performance.[37–43]

InSb nanoflags represent a promising semiconductor material platform, due to their strong intrinsic spin–orbit interactions and quasi-2D character.[1,12–15,44–49] Previous studies have reported detailed characterization of planar JJs based on InSb nanoflags,[13,15,29,50] showing ballistic transport and sizeable Josephson diode effect.[29]

In this work, we consider InSb nanoflag-based JJs fabricated with lateral electrostatic gates (side gates). The aim is to demonstrate that side gates can be used as a tool to manipulate device transport properties both in the dissipative and in the dissipation-less regime.

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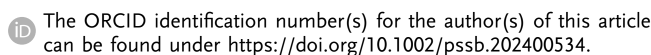
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2. Results

2.1. Device Geometry

In this work, two devices have been studied: SC20-F6 and SC20-F7. The devices, in addition to a conventional back gate, are fabricated with two lateral gates, or *side gates*, which are placed at a distance of about 250 nm from the nanoflag, as shown in **Figure 1** (see the Experimental Section for details on the device fabrication). When the side gates are grounded, the devices behave consistently with what is reported in refs. [15,29,50], where InSb nanoflag-based JJs without side gates have been investigated.

Here, we concentrate on the impact of side gates on transport properties and supercurrent flow, while for a detailed characterization of JJ behavior, for example, back-gate modulation and

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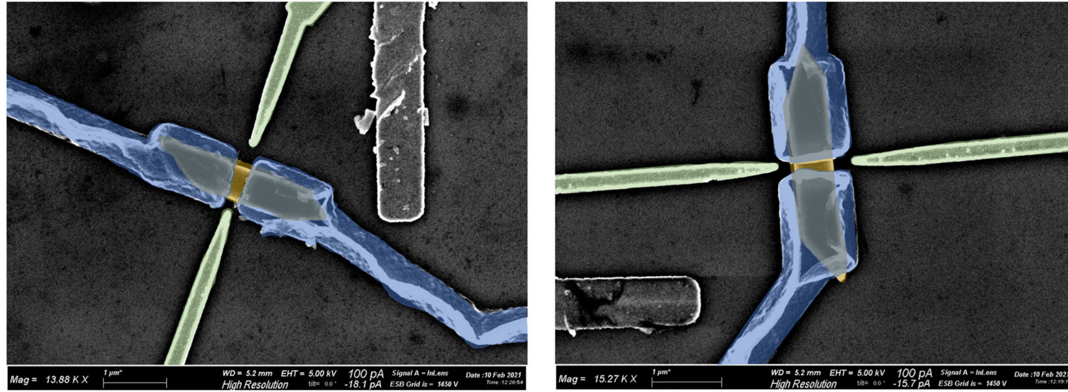

Figure 1. Device F6 and Device F7 from sample SC20. The SEM images have been color coded: InSb, orange; Nb, blue; and side gates, green.

nonreciprocal supercurrent transport, we refer the reader to refs. [15,29,50] and to Section S1, Supporting Information.

2.2. Conductance Modulation by the Gates

The main focus of this section is to quantify the efficiency of the side gates, with respect to the global back-gate, and to extract valuable information about the charge dynamics in the nanoflag, via magnetotransport measurements. For these measurements, the devices are kept in the normal state, since the chosen bias current is higher than the critical current I_c (see Section S1.1, Supporting Information). Firstly, the device conductance is measured as a function of back-gate voltage (V_{BG}), at $T = 4.2$ K, as shown in **Figure 2**a for device SC20-F6. The acquisitions are performed with a low-frequency AC bias set-up. We observe that the pinch-off value of the device, that is, the value of back-gate voltage below which the conductance is negligible, depends on the sweep direction. In the forward direction, the conductance is zero below $\approx$1 V, while, in the backward direction, it drops to almost zero below $\approx$7 V. Hysteresis in the conductance versus back-gate voltage characteristics is known to appear in this kind of device because of defect-assisted charge trapping from the insulating substrate. Indeed, structural defects in silicon dioxide serve as active electron (Si-dangling bonds) or hole (*O*-dangling bonds) trapping centers.[51] Due to their high charge transfer rate, *O*-dangling bonds are expected to provide a larger contribution to the creation of such hysteresis. To have a consistent set of data, in the following, each sweep in back-gate voltage is performed starting from the high-conductance plateau; each time that a higher voltage is needed, the back gate is brought to $V_{BG} = 70$ V and then decreased to the desired value. A measurable conductance value is found only for positive V_{BG}, which indicates that the semiconductor majority carriers are electrons. Thus, the InSb nanostructure is of n-type.

The same measurement is repeated in the presence of a nonzero side-gate voltage V_{SG}. Using the symmetric configuration ($V_{SG1} = V_{SG2} = V_{SG}$), the conductance is measured as a function of V_{SG}, at fixed values of V_{BG}. Three traces are shown in Figure 2c–e at the working points $V_{BG} = 30$, 15, and 5 V, respectively. A linear fit is performed for each curve, from which the value of the slope $m(V_{BG})$ is extracted. Figure 2b shows the dependence of this slope versus back-gate voltage working point, compared with the differential variation of the conductance with respect to the back-gate dG/dV_{BG}. The latter is calculated via numerical differentiation of the curve in Figure 2a. The two curves have similar behavior: in both cases, the maximal modulation occurs for $V_{BG}:15$ V, and no change is induced below the pinch-off value 7 V. Note that the two scales differ by a factor of 30. From this analysis, we deduce that the relative efficiency of the side gates is 1/30.

Individual side-gate sweeps show a background modulation which can be related to universal conductance fluctuations (UCF). This is a common feature of mesoscopic systems,[39,52–54] in which the phase coherence length is larger than the geometrical size. Based on the random matrix theory,[55] a fluctuation of magnitude $G_0 = 2e^2/h$, that is, one conductance quantum, is expected in structures which do not show any spin texture. Here, the observed fluctuations have a magnitude of the order of 10 μS, corresponding to $\approx$0.3 G_0. This reduced value is consistent with predictions for a system with a strong Rashba spin–orbit interaction.[56]

Finally, we report that the side gates efficiently pinch off the device, if the working back-gate point is properly chosen. **Figure 3** presents conductance traces versus side-gate voltage, for different values of V_{BG}, close to the pinch-off. Conductance drops to zero below a threshold value, which depends on the working point in V_{BG}.

2.3. Magnetic Field-Induced Interference Pattern

We now consider the effect of side gates when supercurrent flows through the JJ. The supercurrent flow depends on the magnetic flux through the normal region of the JJ.[57] Due to this mechanism, it is possible to extract information about the effective geometry of the system by looking at the dependence of the $I-V$ curves as a function of applied perpendicular magnetic field. In this configuration, where the magnetic field vector $\mathbf{B} = B\hat{z}$ is aligned with the normal direction of the junction plane $(x-y)$, the magnetic flux is

$$\Phi(B) = A_{\mathrm{eff}} B_{\mathrm{eff}} = W(L + 2\lambda_L)FB \tag{1}$$

with L and W the length and width of the JJ, respectively. Here, the effective area A_{eff} is not directly given by the geometric dimensions of the junction, since the magnetic field penetrates the two superconducting niobium leads for a distance defined by

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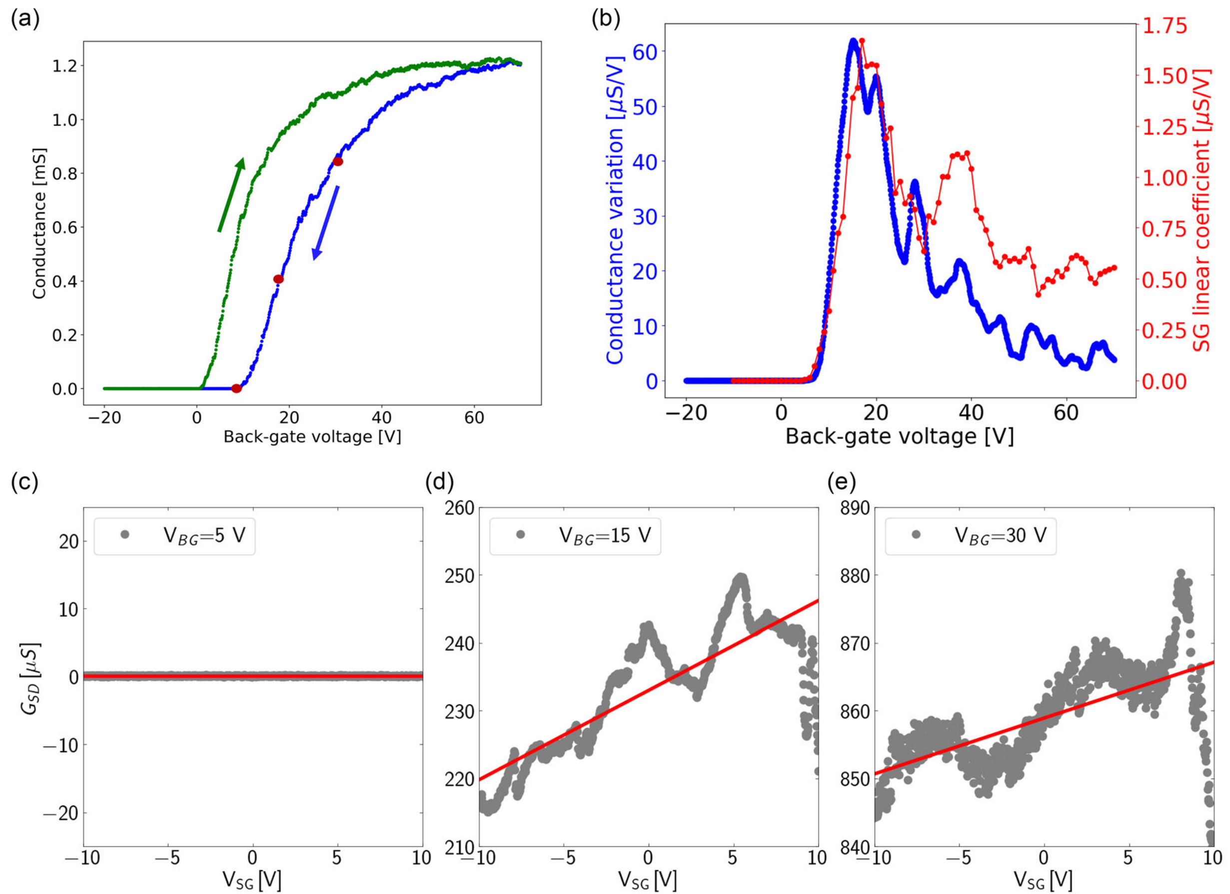

Figure 2. Back-gate and side-gate modulation of the conductance. a) Source-drain conductance as a function of back-gate voltage. The three red dots indicate the back-gate values for which the data in (c-e) were taken. b) Comparison between the conductance variation with respect to the back-gate voltage (left axis) and the side-gate voltage (right axis). The two quantities have analogous structures but they differ in magnitude by a factor of 30. c–e) Conductance versus side-gate voltage for $V_{BG} = 5$, 15, and 30 V, respectively. Gray points represent the experimental data, while the red lines are linear fitting curves. $T = 4.2$ K. $B = 0$. Device SC20-F6.

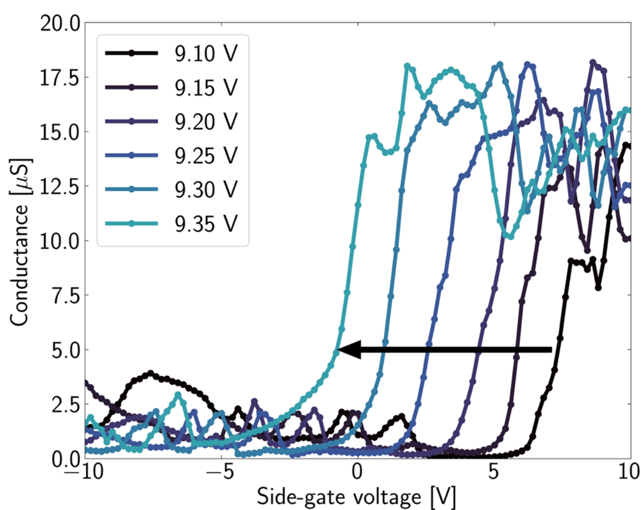

Figure 3. Conductance pinch-off versus side-gate voltage. Six traces are reported, for different values of V_{BG} between 9.1 and 9.35 V. The conductance drops for V_{SG} below a threshold voltage, which depends monotonically on V_{BG}. $T = 250$ mK. $B = 0$. Device SC20-F6.

the London penetration length (λ_L). This quantity only depends on the superconducting material and equals $\lambda_L = 40$ nm in niobium.[58] Moreover, the magnetic field lines are deflected in the presence of the superconducting leads, due to the Meissner effect,[57,59,60] and therefore, the effective value of the magnetic field is increased. This effect can be taken into account with the flux focusing coefficient F, such that $B_{eff} = FB$.[38,40,61–63]

Figure 4a,b shows the $I - V$ characteristics and the differential resistance, respectively, as a function of bias current and magnetic field B, obtained at $V_{BG} = 40$ V and $V_{SG} = 0$ for device SC20-F6. The value of the critical currents $I_c(B)$ is extracted by setting a threshold voltage of $V_{th} = 2$ μV in the $I - V$ curves and is indicated by orange dots in Figure 4. A robust dissipation-less region is present for -12 mT $\leq B \leq 0$ mT: the lobe is centered in $B_0 = -6$ mT, and its half-width is $\Delta B = 7.3$ mT. The maximal supercurrent in a single planar junction is, in fact, expected for $B = 0$. We attribute the small offset to a residual magnetization of the cryostat.

Observation of a Fraunhofer pattern is expected in a planar JJ, under the assumption of 1) a uniform supercurrent distribution $J(x)$ and 2) a wide junction ($W >> L$). However, if W/L is finite, the effective periodicity is larger than the ideal prediction[64] of

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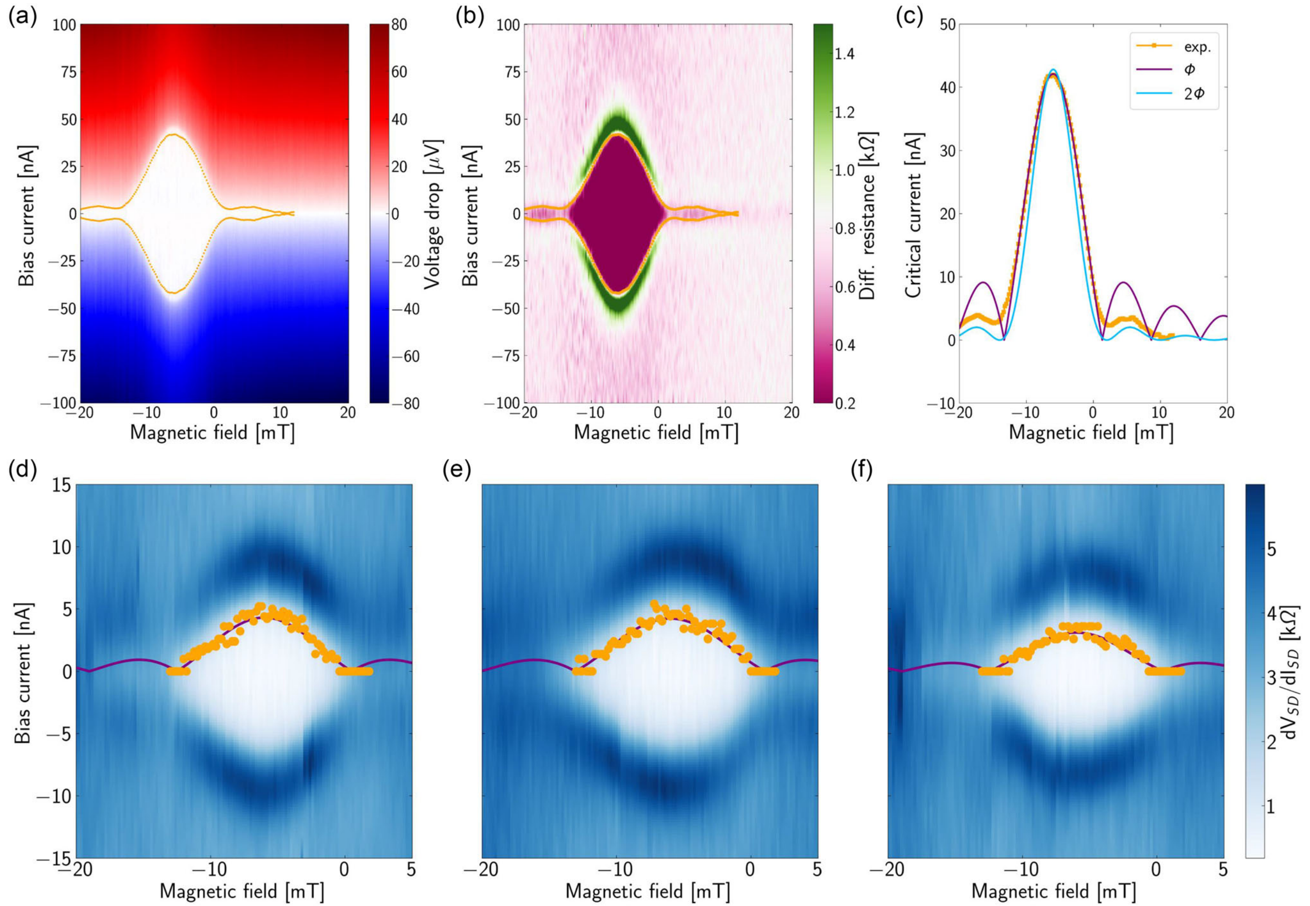

Figure 4. a–c) Interference pattern of the critical current in the presence of a perpendicular magnetic field. a) Voltage drop and b) differential resistance, obtained by numerical differentiation, are reported as a function of perpendicular magnetic field (x-axis) and bias current (y-axis). The critical current is indicated by orange dots. c) Comparison between the extracted values of critical current I_c and the models in Equation (2) (purple) and Equation (3) (light blue). A robust superconducting region is present, centered at $B = -6$ mT, due to a residual magnetization of the cryostat (see text). The first side lobes weakly appear in the experimental data. For the measurements shown in (a–c), the side gates were grounded. d–f) Fraunhofer pattern for different values of the side-gate voltage V_{SG}. d) $V_{SG} = 10$ V, e) $V_{SG} = 0$ V, and f) $V_{SG} = -10$ V. The 2D maps show the differential resistance versus perpendicular magnetic field and bias current. The orange dots represent the experimental values of I_c, while the purple lines are the best-fit curves based on the model in Equation (2). a–c) $V_{BG} = 40$ V, and d–f) $V_{BG} = 16$ V. $T = 250$ mK. Device SC20-F6.

the superconducting flux quantum $\Phi_0 = h/(2e)$. Indeed, the occurrence of an anomalous Fraunhofer pattern has been previously associated with the geometry of the system.[64] In ref. [65], a continuous and nonmonotonic change of the periodicity from Φ_0 to $2\Phi_0$ is demonstrated when the ratio L/W grows.

Our experimental data show only a weak trace of the first lateral lobes. Notably, the height of these features is of the order of the intrinsic thermal current noise of the junction $\delta I_{th} = 2ek_B T/\hbar$;[66,67] here, $\delta I_{th} = 10.5$ nA. Therefore thermal fluctuations may mask the side lobes. Nevertheless, a trace of the first lateral lobes is visible in the differential resistance.

The devices under study present a ratio $(L + 2\lambda_L)/W{:}0.5$. The orange (light blue) line in Figure 4c stands for the best-fit function in the limiting case $L/W << 1$ ($L/W >> 1$). The two models are[64,65,68,69]

$$I_c = I_{c,0} \left| \frac{\sin\left(\frac{\pi\Phi(B)}{\Phi_0}\right)}{\frac{\pi\Phi(B)}{\Phi_0}} \right| \quad L/W << 1 \tag{2}$$

$$I_c = I_{c,0} \left[\frac{\sin\left(\frac{\pi\Phi(B)}{2\Phi_0}\right)}{\frac{\pi\Phi(B)}{2\Phi_0}} \right]^2 \quad L/W >> 1 \tag{3}$$

respectively, with $\Phi(B) = A_{\text{eff}} F(B - B_0)$. The center of the interference pattern B_0, the critical current for $B = B_0$, that is, $I_{c,0}$, and the flux focusing factor F are left as free parameters. When Equation (2) is used for the fit, a maximal critical current $I_{c,0} = 42$ nA is obtained as a fit result, consistent with the experimental observation, which underlines the high quality of the fit, especially close to zero magnetic field. The resulting flux focusing coefficient $F = 1.6$ is comparable to results found in the literature.[61] On the other hand, the model in Equation (3) results in $F = 2.3$. As shown in Figure 4c, Equation (2), represented by the purple line, fits well with the central region, while the side lobes are better modeled by Equation (3) (light blue line). This intermediate regime is consistent with the ratio L/W of the devices.

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Table 1. Results of the fit procedure of the Fraunhofer patterns for different values of the side-gate voltage V_{SG}.

V_{SG} [V]	10	0	−10
$w^{a)}$ [mT]	7 ± 1	8 ± 1	9 ± 1
$I_{c,0}$ [nA]	5.4 ± 0.2	5.0 ± 0.2	4.0 ± 0.2

a) w is the width of the central lobe of the Fraunhofer pattern (in mT), while $I_{c,0}$ is the critical current (in nA) for zero magnetic field applied. $T = 250$ mK. $V_{BG} = 16$ V. Device SC20-F6.

The Fraunhofer pattern measurement was repeated for different values of V_{SG} of the side gates in a symmetric configuration. The Fraunhofer patterns obtained at $V_{BG} = 16$ V for $V_{SG} = 10$, 0, and −10 V are presented in Figure 4d–f, respectively. In each plot, the experimental values of I_c are shown as orange dots, while the purple line is the best-fit curve obtained with the model in Equation (2).

By using the flux focusing factor $F = 1.6$ previously estimated, we can compare the effective area A_{eff} for each configuration. The width of the fitting function (w), which is inversely dependent on A_{eff}, changes for the three configurations. The values are reported in **Table 1**. The monotonic trend is in line with the expected result: when the side-gate voltage is negative, the charge density in the nanoflag is locally reduced in the region where V_{SG} is more effective, that is, the external part of the junction. This implies that the current density $J(x)$ is spatially dependent. This can be seen as an effective reduction of the channel width, which would increase the width of the Fraunhofer pattern, consistent with our results. At the same time, the critical current $I_{c,0}$ at $B = B_0$ is reduced by decreasing V_{SG}, in a similar fashion to the back-gate dependence. In summary, we have shown that the presence of side gates can impact the supercurrent flow through the JJ, modulating both the critical current amplitude of the interference pattern and the effective area of the junction.

2.4. Conductance Behavior at High Magnetic Fields

Next, we inspect the behavior of the device when a strong perpendicular magnetic field is applied, with the two side gates grounded ($V_{SG} = 0$). At high magnetic fields, conductance is predicted to have quantized values with respect to back-gate voltage, due to the formation of Landau levels (LLs). The interplay between magnetic field and carrier density modulation is shown in **Figure 5**a for device SC20-F7, which represents conductance as a function of a perpendicular magnetic field (x-axis) and back-gate voltage (y-axis). Here, we note a kink at $B = 3.15$ T, which corresponds to the transition of the Nb contacts from the superconducting to the normal state. To observe magnetoconductance effects, the conductance variation dG/dV_{BG} is shown in Figure 5b.

In Figure 5b, the relative minima are clearly collected in straight lines. We obtained the relative minima for each trace; the resulting points are shown as white dots. For $4\,T < B < 7\,T$, two families of minima are present, whose slope is $m_0 = 0.7 \pm 0.1$ V/T and $m_1 = 2.1 \pm 0.1$ V/T. These are represented by light-blue lines in Figure 5b. For higher values of the magnetic field ($B > 7$ T), each of the two curves splits up into two (red lines), symmetrically with respect to the original lines.

Following the Shubnikov-de-Haas theory of magnetotransport in 2D electron gases, the conductance is predicted to show a set of minima located on straight lines, emerging from integer filling of LLs. The energy spectrum E_n is discrete, $E_n = \hbar\omega_c(n + \frac{1}{2})$, where $\omega_c = eB/m^*$ is the cyclotron frequency, $\hbar$ the reduced Planck constant, and m^* the effective mass,[70] that is, the LL energy depends linearly on the magnetic field. The two light-blue lines indicate the two lowest spin-degenerate LLs ($n = 0$ and $n = 1$), corresponding to filling factors $\nu = 2$ and $\nu = 4$, respectively. Introducing the back-gate lever arm α_{BG} as the ratio between induced charge ρ_{2D} and applied back-gate voltage V_{BG}, $\alpha_{BG} = \rho_{2D}/V_{BG}$, the slope of the curves is related to the quantum number n as

$$m_n = \frac{\hbar e}{m^*}\frac{\rho_{2D}}{\alpha_{BG}}\left(n + \frac{1}{2}\right) \tag{4}$$

where $\rho_{2D} = m^*/\pi\hbar^2$ is the spin-degenerate density of states in the semiconductor per unit area and e the elementary charge. The ratio between the first two coefficients $m_1/m_0 = 3$ is consistent with the experimental evidence. Moreover, due to the large effective g-factor of InSb, the levels are expected to be spin

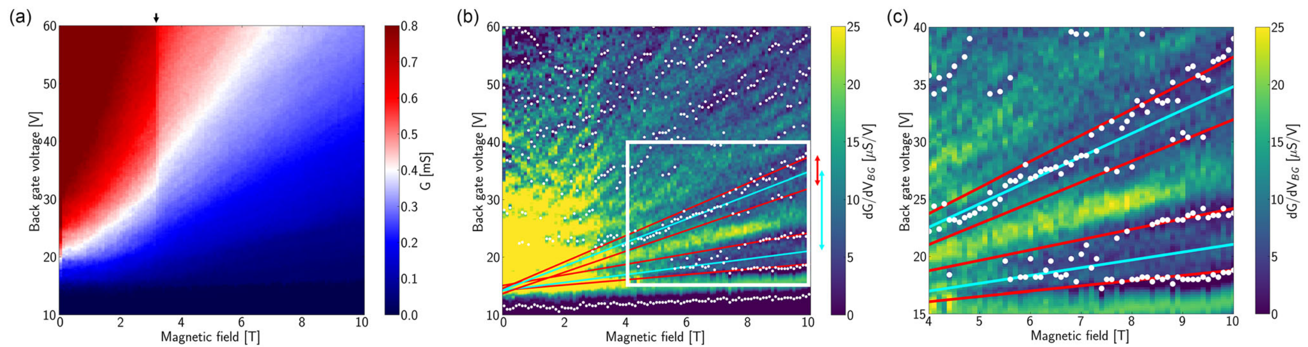

Figure 5. Conductance modulation as a function of perpendicular magnetic field and back-gate voltage. a) Conductance as a function of B (x-axis) and V_{BG} (y-axis). A kink is present at $B = 3.15$ T, indicated by the black arrow, due to the transition of the contacts (see text). b) Conductance variation with respect to V_{BG}, versus B (x-axis) and V_{BG} (y-axis). The white dots represent the local minima of the traces. Two families of minima follow the light-blue lines for $B \leq 7$ T and subsequently split up in 4 total traces, indicated by the red lines. The arrows denote the line separation at $B = 10$ T. c) Zoom-in of panel (b), to highlight the spin splitting at about $B = 7$ T. The range of (c) is indicated by the white rectangle in (b). $T = 250$ mK. Device SC20-F7.

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resolved for high fields, with a gap given by the Zeeman energy. In our case, the relevant energy scales are the spacing between LLs E_L and the Zeeman energy E_Z

$$E_L = \hbar\omega_c = \frac{\hbar e B}{m^*} \tag{5}$$

$$E_Z = g^* \mu_B B \tag{6}$$

where g^* is the effective g-factor associated to spin-orbit interactions and μ_B the Bohr magneton. The separation between the two light-blue lines at $B = 10\,T$, in units of back-gate voltage, is $\delta E_L = 13.9\,V$ and $\delta E_Z = 5.5\,V$ for the original (light-blue) and split (red) lines, respectively. These values are indicated by the arrows in Figure 5b. By comparing them, we can extract the effective g-factor, resulting in

$$g^* = \frac{\delta E_Z}{\delta E_L}\frac{\hbar e}{m^* \mu_B} = 44 \tag{7}$$

which is consistent with the values reported in the literature for InSb nanostructures.[71]

3. Conclusions

We have reported measurements on InSb nanoflag-based JJ devices where two side gates have been laterally placed 250 nm from the junction. We have shown that in a certain range of voltages on the back gate, side gates can completely pinch off the device, with a relative efficiency of 1/30 with respect to the back-gate action. In the dissipation-less regime, both critical current amplitude and Fraunhofer interference pattern can be manipulated by means of the side gates. Thus, side gates represent a useful additional electrical knob to be used in conjunction with back gates,[38] and we expect that their efficiency can be further improved by fabricating them closer to the flag. The electrostatic control of InSb nanoflags with side gates might also be used to tune spin–orbit interactions[39,43,72] or to realize more advanced device layouts[73] and could result in an additional knob for the Josephson diode effect.

The observation of LLs at high magnetic fields clearly shows that the transport in the nanoflags has a 2D character, while the measured g^* confirms the strong spin–orbit interaction predicted for InSb-based devices.

4. Experimental Section

The InSb nanoflags were grown by chemical beam epitaxy (CBE) from metal-organic precursors in a Riber Compact-21 system. Tapered Indium Phosphide nanowires (NW) are used to provide full support to the nanoflags. This strategy allowed to obtain InSb nanoflags of $(2.8 \pm 0.2)\,\mu m$ length, (470 ± 80) nm width, and (105 ± 20) nm thickness.[14,74]

Initially, InP nanowires were grown on InP(111)B substrates via Au-assisted growth. The catalyst particles were 30 nm Au colloids dropcasted onto the bare substrate. The InP nanowire stems were grown with sample rotation for 90 min at 400 °C, with 0.6 Torr TMIn (trimethylindium) and 1.2 Torr TBP (tert-butylphosphine). Then, the growth temperature was reduced by 30 °C (in the presence of TBP flux only) to the InSb growth temperature. The InSb nanoflags were grown without rotation, after aligning the ⟨112⟩ crystal direction toward the Sb precursor beam, as described in ref. [14,74], initially for 30 min with 0.6 Torr TMIn and 2.3 Torr TMSb (trimethylantimony), and then for additional 60 min, linearly increasing the TMSb line pressure from 2.3 to 2.6 Torr, in order to enhance the asymmetric radial growth.

The JJs were defined by the deposition of niobium contacts. Figure 1a,b reports images of devices SC20-F6 and SC20-F7, respectively, captured by scanning electron microscopy (SEM). These devices are equipped with two side gates, made in Cr/Au as described in the following.

Firstly, the InSb nanoflags are dry transferred onto a prepatterned highly conductive p-type Si(100) substrate, which serves as a global back gate. A 285 nm thick SiO_2 layer covers the Si substrate as dielectric. During the mechanical transfer, the InSb nanoflags are detached from the InP NW stems, resulting in well-isolated InSb nanoflags, which were randomly distributed on the substrate. The position of selected InSb nanoflags was determined relative to predefined alignment markers using SEM images. Considering the thickness and the edge geometry of the InSb nanoflags, electrodes were patterned on a 400 nm-thick layer of AR-P 679.04 resist with standard electron-beam lithography (EBL). Prior to metal deposition, the native oxide of the InSb was removed using a sulfur-based etching solution which results also in a smoother InSb surface.[75] To this end, the native oxide was etched for 30 s in an optimized sulfur solution of $(NH_4)_2S_x$ (1:9 $(NH_4)_2S_x$:DI water at 40 °C). Then, the samples were rinsed in DI water for 30 s. Next, a 10/150 nm Ti/Nb film was deposited with a high deposition rate after an intense presputtering of each target, followed by lift off in hot acetone. In order to fabricate side gates, another lithographic step was performed, using AR-P 679.04 resist. In this step, 10/130 nm of Cr/Au were deposited by thermal evaporation.

Table 2 collects the geometric dimensions of the nanoflag-based devices, measured from SEM images.

Table 2. Device dimensions extracted from SEM images.

Device	$W^{a)}$ [nm]	L [nm]	d [nm]
SC20-F6	540	250	260
SC20-F7	530	110	240

a) W stands for the nanoflag width, L is the average normal region length, and d is the distance of the side gates from the nanoflag, computed as the mean between the left-side and right-side-gate. The error is ±10 nm.

While device SC20-F7 was measured in a *quasi-four* terminal configuration, in SC20-F6, three-probe measurements were performed, because of damage in one lead. This resulted in a series resistance of $R_s = 2500\,\Omega$, measured at $T = 4$ K, which was numerically subtracted before processing the data.

For the measurements, we have used an *Oxford Heliox* ^{3}He cryostat, whose base temperature is $T = 250$ mK. The cryostat is equipped with a magnet whose field is perpendicular to the junction plane. The insert is equipped with RC- and π-filters. For AC measurements, a lock-in amplifier (LIA) was used to generate a sinusoidal voltage, with frequency $f = 13.321$ Hz, which was sent to the sample through a 10 MΩ resistance. By measuring both current and voltage drop across the junction with phase-sensitive detection, the conductance of the device can be properly evaluated.

For measurements in DC configuration, in the same ^{3}He cryostat, the current bias configuration was used. To improve the signal-to-noise ratio, the sampled signals in the DC configuration pass through low-noise preamplifiers before being measured.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available in the supplementary material of this article.

Keywords

InSb, Josephson junctions, side gates

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