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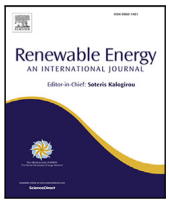

Influence of the temperature on the intrinsic parameters of thin-film photovoltaic modules

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ABSTRACT

The electrical parameters, the ideality diode factor and the parasitic resistances of a photovoltaic module can be estimated from its current–voltage (I–V) curve. However, there are only very few studies focused on thin-film devices, that could have a thermal behavior different from crystalline silicon technologies. This study analyzes the variation of these parameters from a set of current–voltage curves of several commercial modules from different technologies: single-crystalline silicon (sc-Si), multi-crystalline silicon (mc-Si), amorphous silicon (a-Si), tandem of micro-crystalline silicon and amorphous silicon (a-Si/μc-Si), tandem of cadmium selenide and cadmium telluride (CdS/CdTe), and copper indium selenide (CIS).

Most of the modules present a positive value for the current thermal coefficient (α), but the voltage and power temperature coefficients (β and γ) are negative in all the cases. With respect the series resistance (R_S), it is significantly higher for the thin-film modules than for the crystalline silicon ones. Moreover, the thermal coefficient of the series resistance (κ) varies depending on the technology. Regarding the shunt resistance (R_{Sh}), it seems to be insensitive with respect the temperature for a small range. Finally, the diode ideality factor (m) seems to be constant for crystalline silicon whereas it depends on the temperature for thin-film.

1. Introduction

The power output of photovoltaic (PV) cells and modules is very dependent on the incident irradiance, but also on the operation temperature of the device [1]. The influence of the device temperature (T) on the electrical parameters has yet been studied by previous literature (see Table 1) through the typical temperature coefficients α, β and γ, which are referred to the short-circuit current I_{SC}, the open-circuit voltage V_{OC}, and the power in the maximum power point P_{max}, respectively. In addition, changes in this temperature results as a variation in the values of the intrinsic parameters that appears in the single diode model (SDM), e.g. the diode ideality factor (m), the series resistance (R_S) and the shunt resistance (R_{Sh}). Therefore, it is possible to define their respective temperature coefficients μ, κ, and λ. Although this phenomenon has been widely studied for crystalline-silicon modules (c-Si), including both single-crystalline (sc-Si) and multi-crystalline (mc-Si), there is a scarcity of works analyzing this relationship for different PV technologies that do not have the same thermal behavior (see Table 2). From previous literature [2,3] it is known that for rising operation temperatures, a crystalline silicon device will experiment an increment of R_S and a decrement of R_{Sh}. However, for a thin-film cell or module we cannot state if the parasitic resistances will increase or decrease. In fact, this behavior could be different depending on each specific technology. On the other hand, some parameters cannot be estimated directly from measurements and it is necessary to fit a model to their calculation. For that reason, there are very few papers addressing the thermal evolution of those parameters, specially for thin-film modules.

It must be taken into account the negative influence of R_S on the power output of a PV device. An increase of R_S causes a decrement of the slope of the current–voltage (I–V) curve around the open-circuit region with a consequent drop of the maximum power [4]. On the other hand, a low value of R_{Sh} leads to a high slope of the I–V curve in the short-circuit point, obtaining also a reduction of the power output [5]. Veissid and De Andrade [6] performed a study using a sc-Si

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Table 1
Summary of some previous studies reporting estimations of the temperature coefficients α, β and γ.

Reference	Type	α (%/°C)	β (%/°C)	γ (%/°C)
Emery et al. [7]	sc-Si	+0.0411	−0.2817	−0.3619
	sc-Si	+0.0130	−0.3413	−0.5035
	mc-Si	+0.0435	−0.2632	−0.3318
	mc-Si	+0.0675	−0.3675	−0.4690
	mc-Si	+0.0407	−0.2925	−0.3996
	a-Si	+0.0493	−0.2429	−0.2929
King et al. [8]	sc-Si	+0.032	−0.41	
	sc-Si	+0.022	−0.39	
	sc-Si	+0.016	−0.38	
	mc-Si	+0.091	−0.36	
	mc-Si	+0.063	−0.42	
	a-Si	+0.099	−0.41	
	a-Si	+0.082	−0.38	
	a-Si	+0.076	−0.43	
	CdTe	+0.019	−0.37	
Van Dyk et al. [9]	sc-Si	+0.04	−0.35	−0.48
	mc-Si	+0.07	−0.37	−0.46
Fanney et al. [10]	sc-Si	+0.0401	−0.355	
	sc-Si	+0.0350	−0.399	
	a-Si	+0.0916	−0.439	
	a-Si	+0.0940	−0.469	
Virtuani et al. [11]	sc-Si	+0.006	−0.33	−0.45
	a-Si	+0.12	−0.33	−0.45
	a-Si/μc-Si	+0.05	−0.37	−0.36
	CdTe	+0.04	−0.24	−0.21
	CIGS	+0.02	−0.31	−0.36
Dubey et al. [12]	sc-Si	+0.028	−0.30	
	mc-Si	+0.03	−0.28	
	CIGS	+0.003	−0.271	
Dash and Gupta [13]	a-Si	+0.098	−0.294	−0.234
	CdTe	+0.071	−0.28	−0.176
	CdTe	+0.034	−0.197	−0.168
Cotfas et al. [14]	sc-Si	+0.0138	−0.3835	−0.4798
	mc-Si	+0.0870	−0.3725	−0.3713
	a-Si			−0.18
Paudyal and Imenes [15]	mc-Si	+0.085	−0.25	−0.51
	mc-Si	+0.061	−0.25	−0.49
	CIGS	+0.06	−0.26	−0.29
Piliougine et al. [16]	sc-Si	+0.036	−0.34	−0.43
Gasparin et al. [17]	sc-Si	+0.065	−0.34	−0.40
	sc-Si	+0.063	−0.33	−0.42
	sc-Si	+0.066	−0.35	−0.46
	sc-Si	+0.040	−0.36	−0.46
	mc-Si	+0.051	−0.32	−0.44
	sc-Si	+0.060	−0.32	−0.41
Meflah et al. [18]	sc-Si		−0.385	
	mc-Si		−0.519	
	a-Si		−0.121	
	a-Si/μc-Si		−0.254	

cell to discover the effect of an increase of the cell temperature on the diode ideality factor (m) and on the parasitic resistances, both in dark and illuminated conditions. Whereas there is a decrement of m and an increment of R_S, the conclusion for R_{Sh} is not clear.

Banerjee and Anderson [19] stated that R_{Sh} of a sc-Si device will experiment a decrement of around one order of magnitude if the cell temperature is increased in 50 K. In addition, Özdemir and Altindal [20] state that m for this technology experiments a decrement from 1.59 to 1.32 when the temperature increases from 295 K to 375 K.

Karatepe et al. [21] reported, for a sc-Si module under constant irradiance, that the value of R_S increases from 1 Ω to more than 3.5 Ω when the cell temperature increases from 15 °C to 65 °C, but R_{Sh} decreases strongly in a negative exponential way. In addition, a decrement of the diode ideality m with increasing temperatures was also observed. Similar results for the same technology were achieved by Dhass et al. [2], in such a way that an increment of 30 K in the device temperature implies an increment of around 20% in R_S and a decrement of more than half in R_{Sh}. Bai et al. [22] confirmed also the decrement of m (from 1.30 to 1.27 at 1 Sun) for increasing cell temperatures (an increment of around 12 K) for monofacial PERC cells. This fact is also confirmed by [23].

Bensalem and Chegaar [24] studied the effects of the temperature on both parasitic resistances for mc-Si technology . They concluded that whereas the R_S shows a positive derivative as a function of the temperature, R_{Sh} has the inverse behavior. Putri et al. [25] also obtained similar results, confirming that as the temperature of the device increases, there is also an increase of R_S and a decrease of R_{Sh}.

Taking only into account the a-Si technology, Ataboev et al. [26] reported a decrement of both R_S and R_{Sh} when the device temperature increases. For other TH technologies similar results were achieved, for example by Kim and Wojkovich [27] for copper indium gallium selenide (CIGS) cells. In another work [28], InGaAs cells were analyzed, obtaining also that both parasitic resistances and the diode ideality factor decrease as the cell temperature is increased. Finally, there are also some very recent works about the effect of the temperature on perovskite cells, as the one by Sahoo and Manik [29], that find a reduction of m with increasing device temperature.

Table 2
Previous estimations of the diode ideality factor m, the series resistance R_S, and the shunt resistance R_{Sh}, with their respective temperature coefficients μ, κ, and λ. These values are related with the number of cells in series (N_s) and the number of cells in parallel (N_p).

Reference	Type	N_s	N_p	m_{STC} (–)	μ (%/°C)	$R_{S,STC}$ (Ω)	κ (%/°C)	$R_{Sh,STC}$ (Ω)	λ (%/°C)
Derick et al. [30]	mc-Si	36	1	1.417		0.1132		747.4	
El Achouby et al. [31]	sc-Si	36	1	1.148		0.2110		192.8	
	mc-Si	54	1	1.107		0.3519		790.4	
Lawi et al. [32]	sc-Si	60	2	1.63		0.320		205.2	
	mc-Si	72	1	1.20		0.220		410.6	
Nayak et al. [33]	sc-Si	36	1	1.706		0.1287		2136	
	mc-Si	54	1	1.371		0.2072		1692	
	CIS	42	1	1.381		0.508		1913	
Ćalasan et al. [34]	mc-Si	36	1	1.333		0.2235		914.7	
Feng et al. [35]	sc-Si	36	1	1.007		0.5084		317.7	
	mc-Si	36	1	1.223		0.5084		373.6	
	CIS	42	1	1.243		1.3017		217.2	
Reddy and Yammani [36]	sc-Si	36	1	1.244		0.1702		515.5	
	mc-Si	36	1	1.341		1.218		848.4	
Nguyen [37]	mc-Si	36	1	1.454		0.3489		157.7	
Ćalasan et al. [38]	sc-Si	36	1	1.179		0.630		70.53	
	mc-Si	36	1	1.347		0.2265		466.9	
	CdTe	116	1	2.865		2.4211		2670	
Piliougine et al. [3]	sc-Si	36	1			0.288	+0.5		
Bounouar et al. [23]	sc-Si	36	1	1.906	−0.53	0.0226	−0.74	226.3	−1.75
Soon and Low [39]	sc-Si	36	1	1.394	−0.43	0.3855	+0.37	183.03	–
	sc-Si	36	1	1.415	−0.51	0.3263	+0.49	182.3	–
	CIS	42	1	1.148	−0.97	1.6588	+0.60	263.8	–
Alam et al. [40]	CIS	42	1	1.493	−0.057	1.1228	+0.029	356.3	–
Hali and Khlifi [41]	sc-Si	72	1	1.22		0.82		1060	
	mc-Si	48	1	1.52		0.36		100	
	sc-Si	36	1	1.8	−0.045	0.12	+0.2	290	+0.14
	mc-Si	36	1	1.53	−0.014	0.15	−0.099	880	−0.5
Hali and Khlifi [42][a]	a-Si/μc-Si	?	1	5.925		7.2304		4185	

[a] Not reported under STC but at $G = 1001.9$ W/m^2 and $T = 31$ °C.

Despite some discrepancies among the literature about the thermal behavior of the series resistance, there is a consensus about the decrement of the parallel resistance and diode ideality factor for increasing temperatures.

The objective of this work is to study how the temperature affects these three parameters for several PV cell technologies. We measured a sequence of I–V curves of several photovoltaic modules of single-crystalline silicon, multi-crystalline silicon, amorphous silicon, micromorph silicon, cadmium telluride, and CIGS technology exposing the modules to increasing temperature. Then we determined both parasitic resistances and the ideality factor by means of a curve-fitting procedure using the SDM.

The main novelty of this article is the use of a consolidated model as the SDM to perform an in-depth study of the evolution with respect increasing temperatures of six different photovoltaic technologies (four of them considered as thin-film), not only analyzing the temperature coefficients of the main electrical parameters α, β and γ (yet present in the literature), but also studying how the parasitic resistances (the series resistance R_S and shunt resistance R_{Sh}) and specially the diode ideality factor m depend on the cell temperature. The particularities of each different technology are highlighted, focusing on the differences of the thin-film modules, which have a very different thermal behavior with respect the classical crystalline silicon ones.

With this paper we will try to cover the scarcity of studies focused on thin-film technologies and to link the obtained results with information published in previous studies. In the literature there are a few works in the same line that this one, but obtaining different results depending on the cell technology. For example, Cuce et al. [43] analyzes the influence of the temperature on the electrical parameters, the parasitic resistances and the diode ideality factor, but that study is restricted only to a sc-Si module and to a mc-Si one. Ghani et al. [44] also perform a similar work focused on R_S and R_{Sh}, but without including any thin-film module in their study. Only Cotfas et al. [14] perform an wider study including some thin-film modules and considering the parasitic resistances as an element of discussion, but with different results to the ones obtained by ourselves, as it will be seen.

The rest of this paper is organized as follows: Section 2 describes each device under test and the measurement system; Section 3 provides the most relevant results and links this work with previous literature; finally, Section 4 summarizes the key findings of the article.

2. Methodology

The objective of this work is focused on the study of the thermal behavior of different thin-film technologies: amorphous silicon (a-Si), amorphous silicon in tandem with microcrystalline silicon (a-Si/μc-Si), cadmium sulfide in tandem with cadmium telluride (CdS/CdTe) and copper indium selenide (CIS). For comparative purposes, two commercial PV modules of the classical single-crystalline and multi-crystalline silicon technologies have also been added to the list of specimens. The nominal specification values reported by the manufacturer of each PV module have been summarized in Table 3.

One specimen for each technology has been used, labeled as A, B, C, D, E, and F. The first one (A) is a classical PV panel (1515 mm × 662 mm) composed of 36 single-crystalline silicon cells (156 mm × 156 mm) connected in series with a 4 × 9 configuration. It is laminated with a micro-structured glass and provided with an anodized aluminum frame. The second specimen (B) is a PV module (1500 mm × 668 mm) with 36 multi-crystalline Silicon cells (156 mm × 156 mm) connected

Table 3
Nominal values reported in the specification sheets of the modules under study.

Technology	*A* sc-Si	*B* mc-Si	*C* a-Si	*D* a-Si/μc-Si	*E* CdS/CdTe	*F* CIS
N_s	36	36	108	96	116	104
$I_{SC,STC}$ [A]	8.55	8.68	1.19	3.34	1.23	3.18
$V_{OC,STC}$ [V]	22.4	22.1	92.0	59.20	88.7	59.7
$P_{max,STC}$ [W]	145	140	60	121	72.5	120
$I_{Pmax,STC}$ [A]	8.00	7.91	0.90	2.69	1.09	2.79
$V_{Pmax,STC}$ [V]	18.1	17.7	67	45.00	66.6	43.1
α [A/°C]	+0.0036	+0.0052	+0.0009	+0.0023	+0.0005	+0.0001
β [V/°C]	−0.072	−0.080	−0.28	−0.18	−0.22	−0.22
γ [W/°C]	−0.67	−0.64	−0.14	−0.29	−0.18	−0.6

* STC stands for Standard Test Conditions as defined by IEC TS 61836:2016 [45].

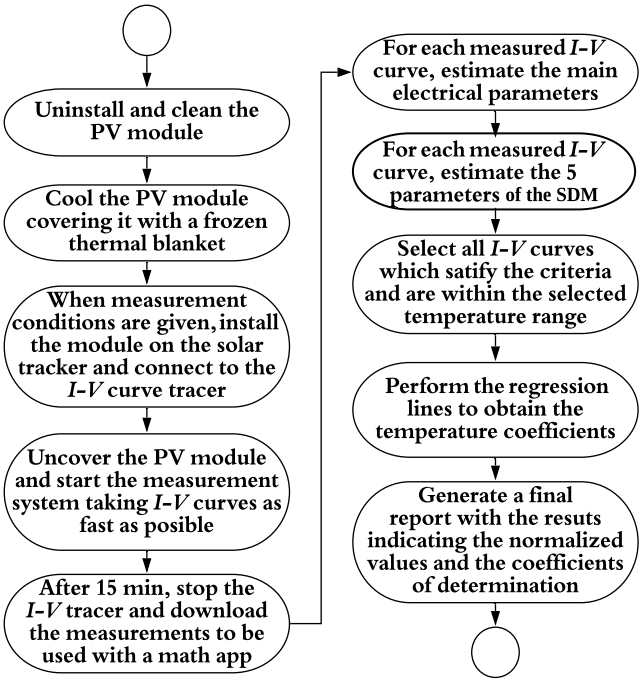


Fig. 1. Description the mechanism used to determine the intrinsic parameters.

also in series and protected by a black aluminum frame in a 4 × 9 layout.

Modules *C* and *D* belong to the amorphous silicon technology. Module *C* (990 mm × 960 mm) is a single-junction a-Si:H module with 108 p-i-n cells over a 5 mm float glass. Amorphous silicon is hydrogenated in order to passivize the dangling bonds and improve the efficiency. Module *D* (1409 mm × 1009 mm) is composed of 96 cells each one including a top a-Si sub-cell and a bottom μc-Si sub-cell. It is built over a 4 mm low-iron front glass. Both modules include foil back-sheets and aluminum frames.

Module *E* (1200 mm × 600 mm) is composed of 116 cells in series of CdS/CdTe technology with a frameless double-glass of 3.2 mm thickness each side, laminated using an edge seal. Module *F* (1595 mm × 685 mm) has 104 cells (in series) of CIS technology. The black aluminum frame is extremely rigid and corrosion-resistant. The glass is mounted floating on a layer of highly elastic polymer.

A concise flow-chart of the experiment is shown in Fig. 1. Several *I–V* curves of each module have been measured on the roof of *School of Engineering* of the *University of Malaga* (Spain). At the beginning, each device under test remains inside a refrigerated room without light during several hours trying to keep it as cool as possible. Before starting the experiment the PV module is covered with a frozen cooling mat. Under a perfect clear-sky day and close to solar noon, each specimen is installed on a 2-axis solar tracker, by adjusting manually its orientation in order to reach an irradiance around $G = 1\,000$ W/m^2 as possible. Four Pt100 thermo-resistive sensors have been plugged on the backside surface and the four acquired temperature values have been averaged. Then, the specimen is uncovered, initiating continuous *I–V* curve acquisition. During the experiment the temperature of the PV module will increase before reaching the thermal equilibrium after a few minutes of exposure.

The acquired data have been post-processed in order to select those ones corresponding to an irradiance value within the range $G = 1\,000 \pm 20$ W/m^2, with a difference of irradiance before and after a measurement smaller than 5 W/m^2, and with a wind speed lower than 4 m/s. More information about the measurement system is provided by Piliougine et al. [46].

Following the procedure described above under outdoor conditions (where the user cannot control the range of the temperature or its increment rate because they depend on the external environment) it is only possible to acquire a few *I–V* curves throughout a small temperature range (a maximum temperature spamming of 12 °C) in such a way the number of samples will be small and this could imply poor R^2 values when performing the linear regressions to estimate the temperature coefficients. This can be solved performing the experiment indoors using a solar simulator inside a temperature-controlled enclosure. However, the aim of this article is just to estimate these intrinsic coefficients under outdoor conditions because this is closer to the operating scenario of a real PV plant.

In order to characterize the PV modules, a number of laboratory instruments have been connected to a personal computer that coordinates them, as it is depicted in Fig. 2. A four-quadrant programmable power supply is programmed to perform a voltage sweep of each specimen whereas a pair of multi-meters are triggered to take measurements of the PV voltage and PV current (this last through a shunt resistor). As both multimeters are commanded by the same input trigger signal, we are ensuring the simultaneous acquisition of the voltage and current components of the *I–V* pairs. In addition, this system is able to take a full *I–V* curve, because the four-quadrant power supply can operate as a load but also as a source covering all the required quadrants. The developed software allows also to program automatic campaigns of measurements without the presence of an operator and also to store the results in a database whose content is available through a web portal on internet [47].

In order to estimate the electrical parameters and temperature coefficients, the following steps have been followed: (1) the *I–V* curves measured outside $G \in [980, 1020]$ W/m^2 were discarded; (2) if the irradiance measured before the *I–V* curve differed more than 5 W/m^2 from the irradiance measured after, the *I–V* curve was also discarded, (3) the *I–V* curves measured under a wind speed more than 5 m/s were discarded, (4) for each *I–V* curve, the main electrical parameters were estimated by means of the procedure described by Emery [48]: the short-circuit current I_{SC}, the open-circuit voltage V_{OC}, the power in the maximum power point P_{max}, and finally the current and voltage at that point, I_{Pmax} and V_{Pmax} respectively. Finally, for each *I–V* curve, we

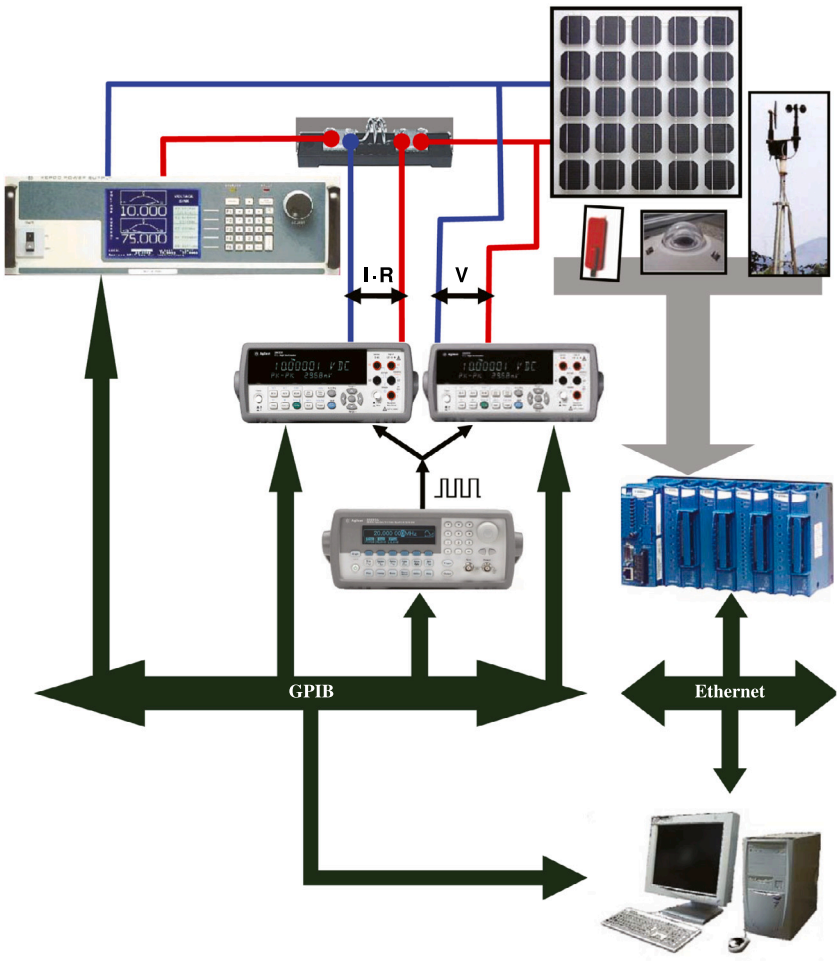


Fig. 2. Experimental system used to characterize the different photovoltaic modules.

Table 4
Ranges used the curve fitting procedure for each parameter of the SDM model.

	I_{ph} [A]	I_s [A]	m[a]	m[b]	R_S [Ω]	R_{Sh} [Ω]
Lower value	0.1	1e-15	1	1	0	10
Upper value	15	1e-2	2	5	50	1e10
Initial value	I_{SC}	5e−6	1.5	3	$\left\|\frac{\partial V}{\partial I}\right\|_{I=0}$	$\left\|\frac{\partial V}{\partial I}\right\|_{V=0}$

[a] Used for modules *A* and *B*.
[b] Used for modules *C*, *D*, *E*, and *F*.

need to extract the single diode model (SDM) parameters, including: the photo-generated current I_{ph}, the dark saturation current I_s, the series resistance R_S, the shunt resistance R_{Sh}, and the diode ideality factor m.

This last step, known in the literature as *parameter identification*, can be performed by a classical method like curve fitting or by means of artificial intelligence approaches. In this paper, three different techniques have been implemented:

- Curve fitting trust-region algorithm
- Genetic differential evolution
- Covariance matrix adaptation evolution strategies

The *trust-region* (TR) algorithm is a classic numerical optimization method that allows to specify, in addition to an initial approximation, a feasible interval for each parameter. For crystalline silicon technologies a value of $m \in (1,2)$ is assumed, whereas for thin-film a range of $m \in (1,5)$ is more suitable . The ranges used for all the parameters and the initial value required by the algorithm are listed in Table 4.

With only five parameters to identify, and by using the narrow intervals proposed by previous literature, it is possible to perform the identification with fast convergence and reliability [3,16,49,50]. In contrast, for models with a higher number of parameters, such as the seven-parameter double diode model, artificial intelligence approaches are more suitable, such as *differential evolution* (DE) or *covariance matrix adaptation evolution strategy* (CMAES), both of them considered in this work for comparative purposes.

The DE method is based on evolutionary computation and it is aimed at determining the parameters of the SDM model through an iterative generation of a population of potential solutions by means of the application of the mutation operator and the combination operator [51]. It is able to explore the solution space in an effective way for non-linear problems like the SDM model.

In turn, the CMAES method is a stochastic approach that works by the iterative updating of a multivariate normal distribution of candidate solutions [52], and it is effective for high-dimensional problems with many parameters to determine.

In order to estimate all the parameters at STC, it is necessary to perform a linear regression of each magnitude versus the device temperature. However, we cannot measure this device temperature directly because it is impossible to put a temperature sensor in contact with the internal cell. In addition, each cell operates at a slightly different temperature in such a way there is not a unique value for this magnitude. This issue can be solved by using several temperature

sensors (four in this work) adhered on different points of the back-surface of each module and estimating the internal temperature based on these measurements. We used the model presented by King et al. [53] (Eq. (1)), which estimates the internal temperature T using T_b and the irradiance value G. The average value of the four measurements was used as T_b. In this model ΔT is a constant which value has been assumed as 3 °C in this work for all the modules.

$$T = T_b + \frac{G}{\mathrm{G_{STC}}} \cdot \Delta \mathrm{T} \tag{1}$$

Following the indications from previous literature [7,8,54], and specially the International Standard IEC 60891:2021 [55], we must to plot (scatter plot) each parameter under study with respect the estimated value of T. After, we can apply over this plot a regression using a linear model such as $M + N \times (T - \mathrm{T_{STC}})$, being M the value of the parameter at the standard temperature $\mathrm{T_{STC}}$ = 25 °C and N the temperature coefficient associated to that parameter. The obtained value of the correlation coefficient $R^2 \approx 0$ means that the temperature T has not any influence on the studied parameter. In that case, we assume its value as a constant with respect to T, reporting only the mean value among all the measurements within the temperature range.

3. Results and discussion

According to the procedure described above, we have estimated the values of (I_{SC}, V_{OC}, P_{max}, R_S, R_{Sh}, m) in STC. In addition, it has been possible to estimate their respective temperature coefficients whenever the magnitude exhibit a dependence on the temperature. The procedure has been applied to the six PV modules under study to show the thermal behavior of all the parameters under study. For all the PV modules, the results obtained for the three different parameter identification techniques are shown in the plots included from Figs. 3 to 14. As it can be seen, the results obtained using the classical trust-region fitting procedure (**TR**) obtains better results than the plots using differential evolution (**DE**) or covariance matrix adaptation evolution strategies (**CMAES**). For that reason the results of **DE** and **CMAES** are not included in the table that summarizes the results given by the regression plots (see Table 5).

3.1. Modules A and B (sc-Si and mc-Si)

Figs. 3 and 5 show the results of the estimation of the main electrical parameters ($I_{SC,STC}$, $V_{OC,STC}$ and $P_{max,STC}$) and their respective temperature coefficients of the modules A and B respectively, whereas Figs. 4 and 6 focus on the parasitic resistances and the ideality factor. From a comparative of their respective columns of Tables 3 and 5, it can be seen that, for module A (manufactured by a high-top company), all the electrical parameters (and also their respective temperature coefficients) are very close to the nominal values reported by the manufacturer. We can assume this fact as a proof that validates the accuracy of our measurement system and the procedure followed to process the data. Contrary, the estimated values of β and γ in module B differ significantly from data given in its specification sheet (we have only obtained a similar value of α).

Figs. 3(a) and 5(a) show that an increase of T produces a slight increase (positive slopes) on I_{SC}, with α being precisely the rate of this increase. As can be expected, this effect will repeat with most of the modules studied in this paper, but depending on the case this effect may be more or less noticeable. This phenomenon on crystalline silicon devices has been reported in many previous works [7–18,43,44,56]. On the other hand, the same papers also report the strong negative effect of an increment of T on V_{OC} (negative value of β in Figs. 3(b) and 5(b)). The reason of the increase of I_{SC} and the decrease of V_{OC} is the reduction of the band-gap energy of the semiconductor material when the temperature increases [57]. More than 80% of the negative impact of the temperature on the energy output of a PV module is due to this fact [58]. Therefore, as it can be seen in Figs. 3(c) and 5(c), we will obtain a negative value of the temperature coefficient of P_{max}. In general, this fact continues being true for most PV devices [59].

Referring to the behavior of R_S with respect to T (Figs. 4(a) and 6(a)), it can be seen that TR and DE obtain very similar results whereas CMAES report a worse estimation due to a outlier value around 43 °C. There is a clear positive correlation for crystalline silicon. This finding is in line with some earlier papers [2,3,6,21,23,44]. Contrary, other authors [14,19,43,56] have reported a decrement of R_S for increasing values of T, also for the same technology. According to Figs. 4(b) and 6(b), the influence of T on R_{Sh} is not significant for these crystalline silicon modules, but this result does not agree with other works from the literature [2,14,43,56] where a clear decrement of this parameter is reported for rising values of T. This could be due to the small range of temperature (only around 10 °C) taken into account in our study in comparison to the ranges used in those previous papers. In any case, it is known from some authors [5,60–62] that the most influential variable on R_{Sh} is by far the irradiance G. It can be seen that both DE and CMAES overestimate the mean value of R_{Sh} with respect TR, reporting a higher standard deviation.

Based on Figs. 4(c) and 6(c), m seems to be invariable with respect to T, but this behavior should not be a surprise because it has been assumed as a constant throughout the literature [53,63–66]. Even IEC 60891:2021 [55] does not take into account the possibility of using a variable value of m. However, some studies state decrements of m for rising values of T in crystalline silicon devices [6,14,20,43,56]. For those cases, Sauer et al. [60] state that the relationship between m and T should be given by a linear function (Eq. (2)), being μ the temperature coefficient of m) obtaining larger values of R^2 as T has more influence on m:

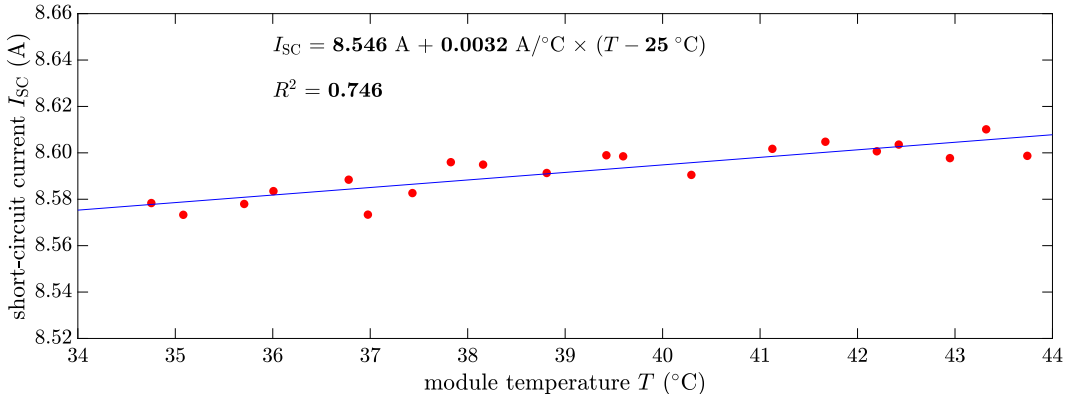
$$m = m_{STC} + \mu \times (T - \mathrm{T_{STC}}) \tag{2}$$

3.2. Module C (a-Si)

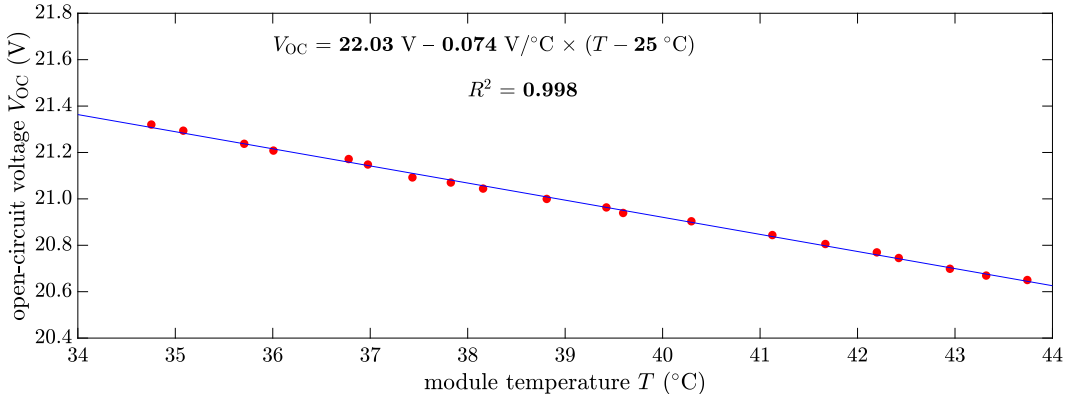
Comparison between the nominal (Table 3) and experimental (Table 5) values corresponding to the C module (a-Si) reveals that there is a high discrepancy in P_{max} although I_{SC} and V_{OC} are quite similar. The experimental values estimated for α, β, and γ are positive in the first case and negative in the other two cases.

As it can be seen in Fig. 7(a), the estimation of α in absolute terms is +0.0008 A/°C (whereas its nominal value is +0.0009 A/°C), which means a relative coefficient of +0.065 %/°C. On the one hand, King et al. [8] reported relative values of α equal to +0.076 %/°C, +0.082 %/°C, and +0.099 %/°C for other three PV modules of the same technology. In fact, a typical value for a-Si technology could be +0.08 %/°C [67]. On the other hand, Fanney et al. [10] stated a value around +0.09%/°C, quite smaller than the value of +0.12 %/°C reported by Virtuani et al. [11]. Cotfas et al. [14] reported a value around +0.225%/°C. According to experiments performed by Riesen et al. [68], this parameter α could range between +0.05%/°C and more than +0.20%/°C depending on the different deposition parameters used during the manufacturing process. In general, the variability of this temperature coefficient for a-Si devices seems to be greater than the same parameter for crystalline silicon.

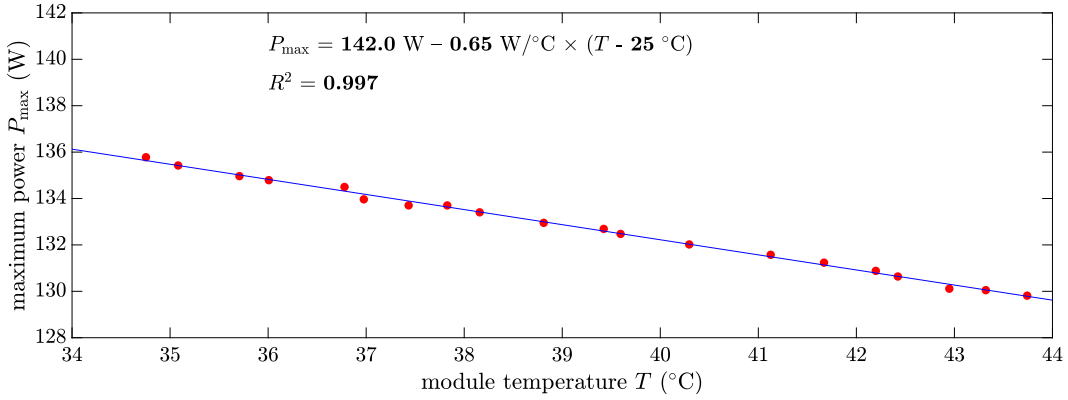
From Fig. 7(b) we can state an absolute value of −0.31 V/°C (equivalent to −0.33 %/°C) for β, that is enough close to the value −0.28 V/°C given by the manufacturer. This also agrees to the estimation given by Cotfas et al. [14], with a value β = −8.09 mV/°C whereas $V_{OC} \approx$ 2.64 V, that means a relative value of −0.31 %/°C. Similar results were stated by Virtuani et al. [11], who achieved a relative value of −0.33 %/°C. However, King et al. [8] obtained results between −0.37 and −0.43 %/°C. Even Fanney et al. [10] gave an estimate close to −0.47 %/°C for the same technology. Depending on the tuning parameters of the manufacturing process, Riesen et al. [68] obtained results in the range (−0.4, −0.2) %/°C.



(a) estimation of $I_{SC,STC}$ and α for the module A



(b) estimation of $V_{OC,STC}$ and β for the module A

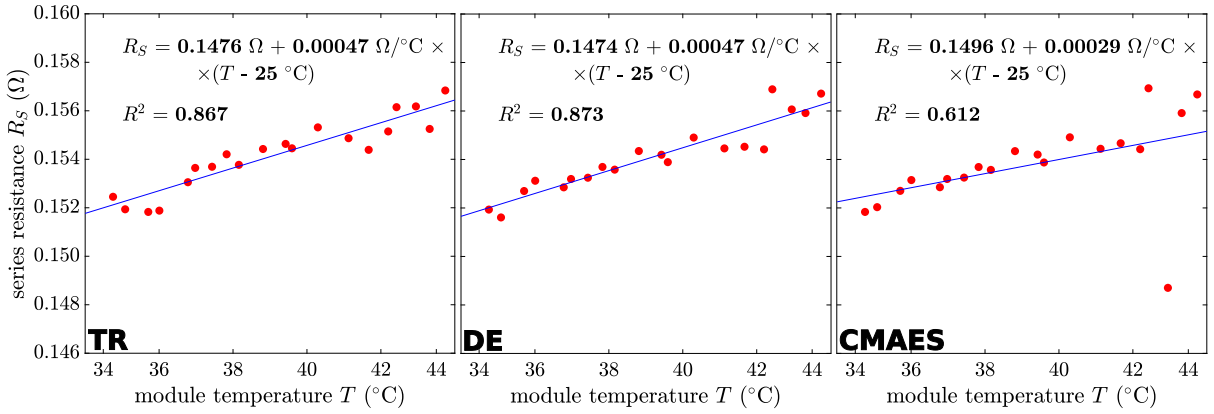


(c) estimation of $P_{max,STC}$ and γ for the module A

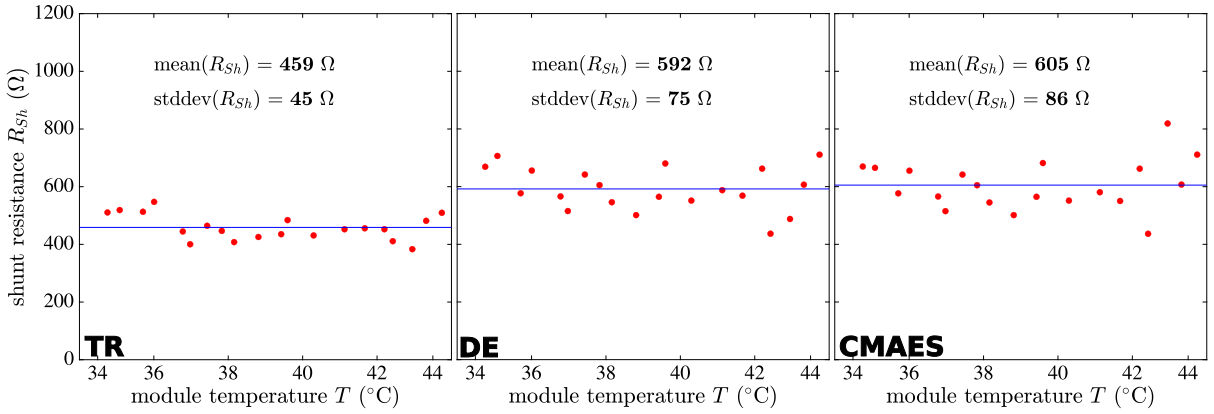
Fig. 3. Main electrical parameters and temperature coefficients of module A.

The results obtained for γ can be seen in Fig. 7(c), where a negative slope of −0.15 W/°C is reported (−0.21 %/°C), whereas the nominal value is −0.14 W/°C. Again, this is inline with Riesen et al. [68], which established an interval as $(-0.3, -0.1)$ %/°C. Other works from the literature also reported values within this previous interval [11,14,67]. The γ coefficient of crystalline silicon devices is significantly more negative than that for amorphous silicon devices, in such a way the energy output of the modules of this technology is more insensitive to changes in the temperature [69].

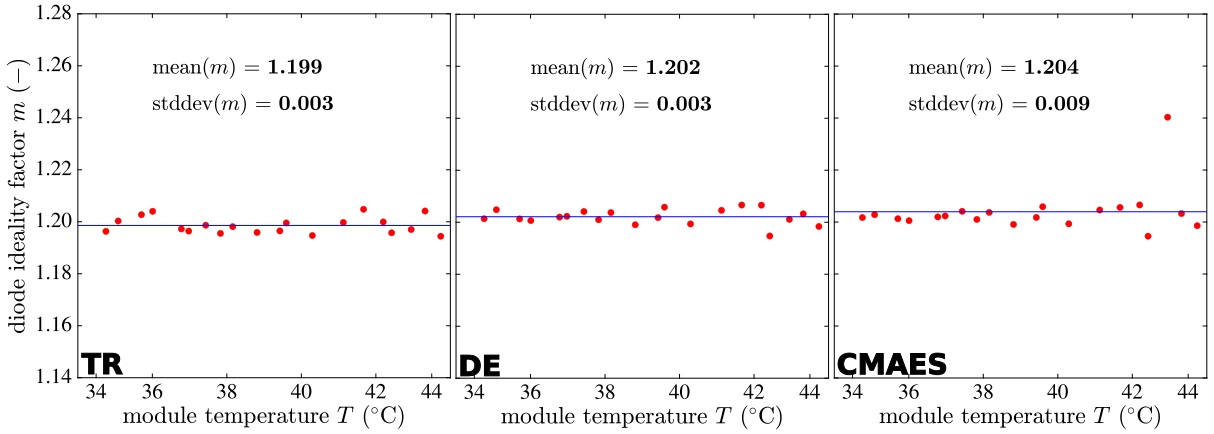
Figs. 8(a) and 8(b) refer to the estimation of the parasitic resistances of the amorphous silicon module. As it can be seen, the result using TR obtain a very high coefficient of determination R^2 but for DE and CMAES this coefficient is around 0.6 and both of them underestimate R_S. It must be highlighted that the value of the series resistance R_S = 5.87 Ω for this a-Si device is of more than one order of magnitude greater than for the crystalline silicon modules A and B. This discrepancy cannot be justified only taking into account the difference in the number of cells (108 in the amorphous device versus 36 in the crystalline ones), but also considering the individual contribution of each cell to the total R_S. According to the results reported by Cotfas et al. [14], the R_S of an a-Si cell is much more greater than the R_S of a sc-Si cell or a mc-Si cell. However, instead of experimenting an increment of R_S for rising values of T (as happen with crystalline silicon), in the amorphous case the impact for the temperature is inverse, i.e., the value of κ is negative for this technology. In absolute terms, the value of κ is 2 orders of magnitude greater than the value reported for crystalline silicon. For another a-Si module with very similar values for I_{SC} and V_{OC}, Eke and Oktik [70] provided a formula to estimate R_S that in



(a) estimation of $R_{S,\text{STC}}$ and κ using trust-region, differential evolution and covariance matrix adaptation evolution strategies



(b) estimation of $R_{Sh,\text{STC}}$ using trust-region, differential evolution and covariance matrix adaptation evolution strategies



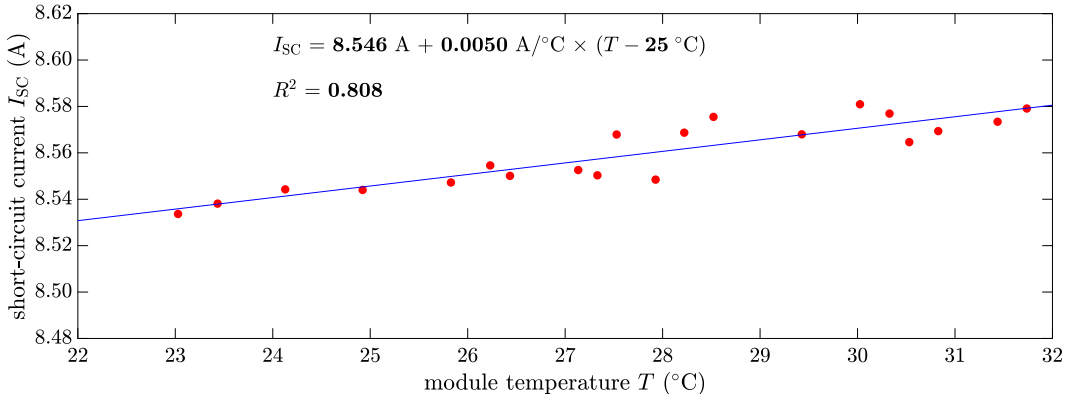
(c) estimation of the ideality factor using trust-region, differential evolution and covariance matrix adaptation evolution strategies

Fig. 4. Parasitic resistances and ideality factor of module *A* using different methods of parameter identification.

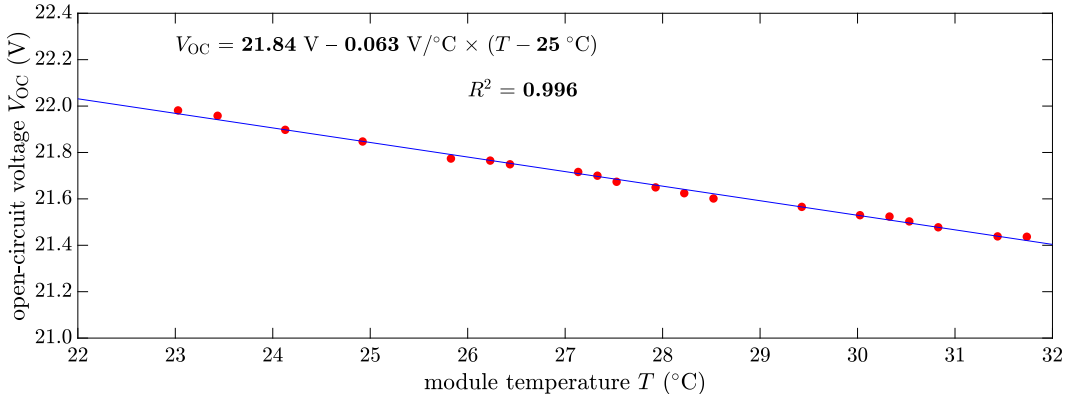
STC provides a value of 5.45 Ω, very close to our result. In a study of degradation of a-Si modules performed by Osayemwenre and Meyer [71], at the beginning of the exposition period, the range of values was $R_S \in [6.8, 9.7]$ Ω (with $I_{\text{SC}} \in [1.2, 1.4]$ A and $V_{\text{OC}} \in [22.0, 22.3]$ V). As it can be seen, for commercial a-Si modules, these values for R_S could be assumed as normal.

As for the shunt resistance, taking into account that the range of temperature is very small, we cannot appreciate that there is any influence of T on R_{Sh}. We obtained a mean value for C of 916 Ω (using TR as parameter identification method), significantly greater than the values obtained for modules *A* and *B*. Again, it is possible to see in the paper by Cotfas et al. [14] that R_{Sh} is greater for amorphous silicon than for crystalline silicon. However, that previous work reported a dependence of R_{Sh} on T, but in that case the studied interval of temperatures spams throughout 60 °C. Eke and Oktik [70] provided an equation to estimate R_{Sh} for a very similar a-Si module, that allow us to obtain R_{Sh} equal to 518.9 Ω.

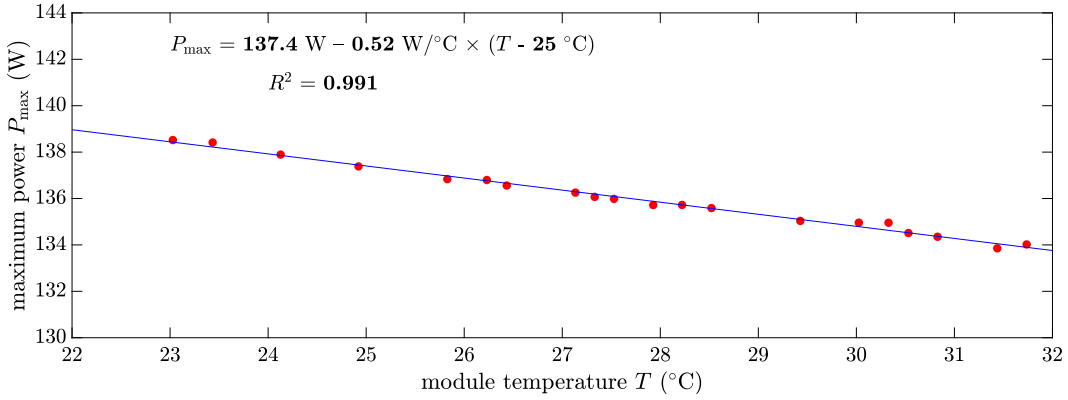
Concerning the estimation of m, for this a-Si module, there is a clear dependency on the device temperature T contrary to the results obtained for modules *A* and *B*, where no dependency was found. Therefore, it is necessary to take into account a temperature coefficient μ for the ideality factor m, in the sense expressed by (Eq. (2)). For this technology, there is a significant decrement of m as the temperature T increases, in such a way the module can have a more squared *I–V* curve. This trend has been also analyzed by Kind et al. [72] also for a-Si, but reporting smaller values for m. The STC value for



(a) estimation of $I_{SC,STC}$ and α for the module B



(b) estimation of $V_{OC,STC}$ and β for the module B



(c) estimation of $P_{max,STC}$ and γ for the module B

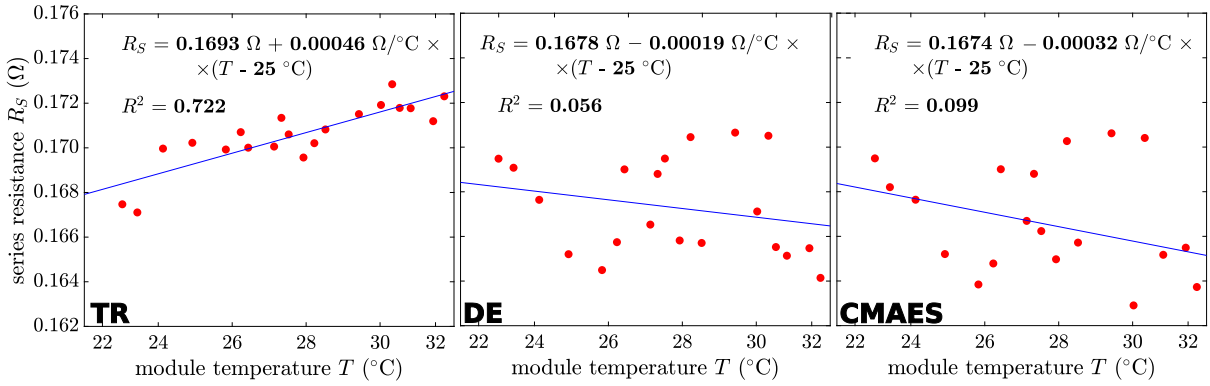
Fig. 5. Main electrical parameters and temperature coefficients of module B.

this parameter for amorphous silicon is also different with respect to crystalline silicon (where the theory [73] states that $m \in [1, 2]$). In fact, we have estimated a value $m_{STC} = 3.018$ for this a-Si specimen. From the results reported by Cotfas et al. [14], very close values for m and μ can be derived. Finally, Meyer [74] performed a study where during the initial exposure period of a amorphous silicon specimen this parameter has changed significantly: from 1.71 with 0 Wh/m^2 until 2.96 with 130 Wh/m^2.

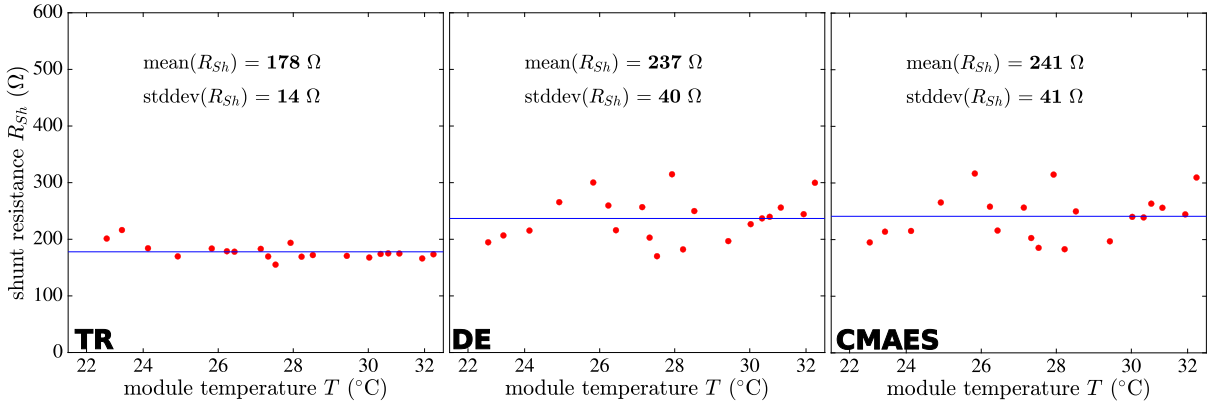
3.3. Module D (a-Si/μc-Si)

The module D is a tandem of amorphous silicon and microcrystalline silicon (also called micromorph) and noted as a-Si/μc-Si. As it can be seen in Fig. 9, our experimental estimation of the main electrical parameters at STC is close enough to the values provided by the manufacturer. We estimated $I_{SC} = 3.052$ A (versus a nominal value of 3.34 A), whereas our experimental value of α is +0.021 A/°C (while the its nominal value is +0.023 A/°C). In relative terms this temperature coefficient is +0.069 %/°C, higher than +0.05 %/°C reported by Virtuani et al. [11], but significantly lower than +0.15 %/° estimated by Mitterhofer et al. [75] for another module of the same technology (but with a nominal value of $\alpha = +0.07$ %/°C).

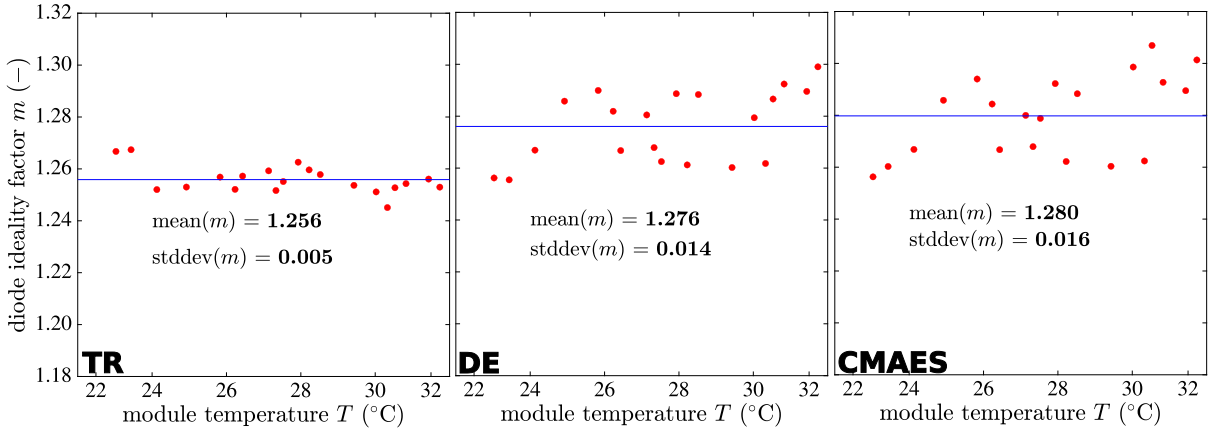
With respect the estimation of $V_{OC,STC}$ and β, the results can be seen in Fig. 9(b). A value of $V_{OC,STC}$ is = 58.50 V versus a nominal value of 59.20 V, whereas we have estimated a $\beta = -0.197$ V/°C (with a nominal value of −0.178 V/°C). This means a relative value of β around −0.34 %/°C, between the estimations given by Virtuani et al. [11] (−0.37 %/°C) and Mitterhofer et al. [75] (−0.30 %/°C). However,



(a) estimation of $R_{S,\mathrm{STC}}$ and κ using trust-region, differential evolution and covariance matrix adaptation evolution strategies



(b) estimation of $R_{Sh,\mathrm{STC}}$ using trust-region, differential evolution and covariance matrix adaptation evolution strategies

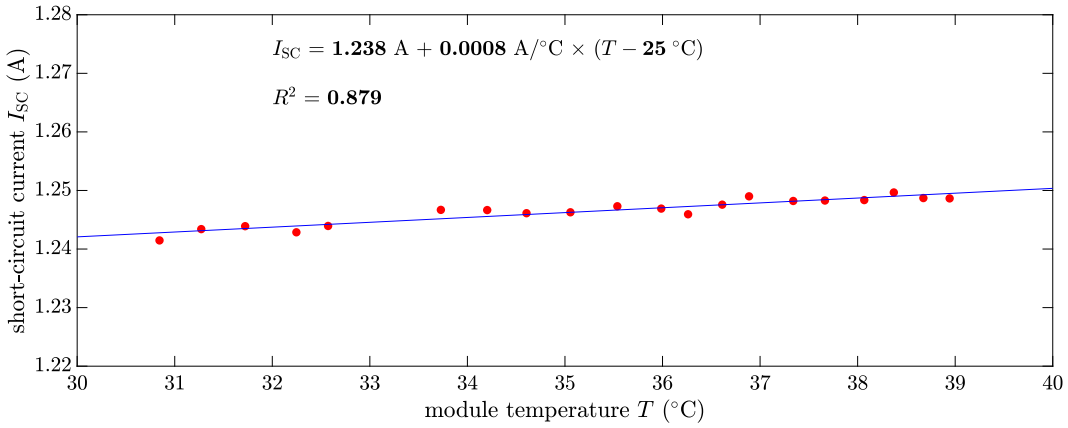


(c) estimation of the ideality factor using trust-region, differential evolution and covariance matrix adaptation evolution strategies

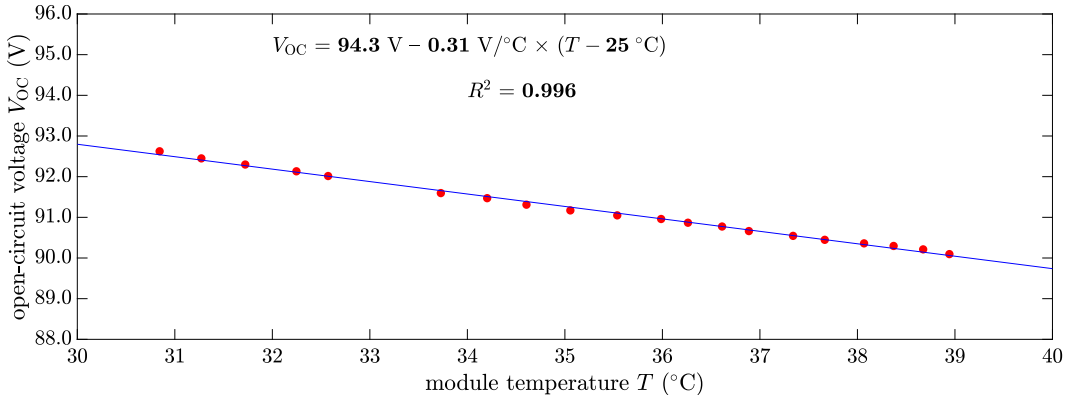
Fig. 6. Parasitic resistances and ideality factor of module *B* using different methods of parameter identification.

other authors reported values that imply a smaller influence of T on V_{OC}, such as Meflah et al. [18] who reported −0.254 %/°C. In line with that, Kata et al. [76] provided a linear formula for V_{OC} from which a value β = −0.27 %/°C can be derived. Fig. 9(c) provides an estimation for $P_{\mathrm{max,STC}}$ = 116.7 W, not so far from the value $P_{\mathrm{max,STC}}$ = 121 W provided by the manufacturer. The corresponding temperature coefficient γ is −0.37 W/°C, that is significantly different to the nominal value −0.29 W/°C. Therefore the relative γ estimated from our results is −0.32 %/°C, that is in agreement to the value −0.36 %/°C provided by Virtuani et al. [11] for a-Si/μc-Si. Contrary, Mitterhofer et al. [75] reported a very different estimate (−0.11 %/°C).

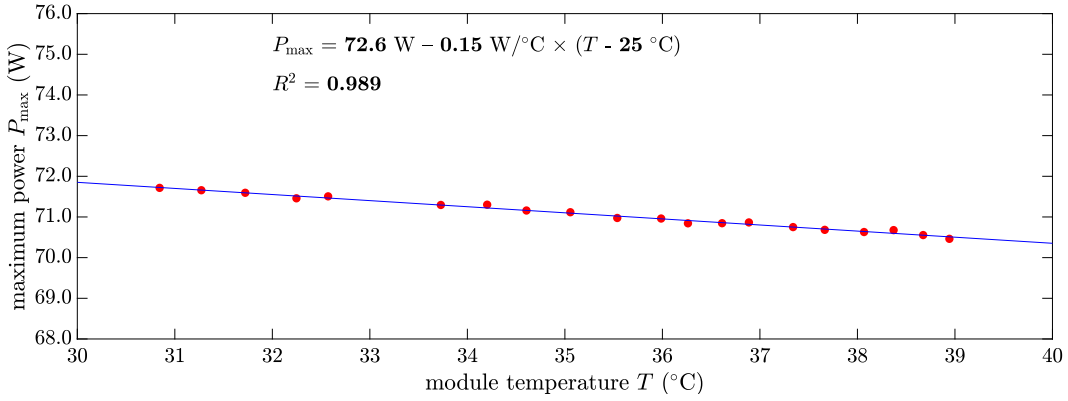
On the one hand, our estimation of the series resistance in STC for module *D* ($R_{S,\mathrm{STC}}$ = 0.409 Ω in Fig. 10(a)) is obtained with a positive influence of T quantified by κ = +0.0026Ω/°C (for this PV module the results obtained using DE or CMAES should be discarded due to their R^2 value near 0). This value of R_S is much greater than the values obtained for modules *A* and *B* (≈ 0.15 Ω) but of the same order of magnitude (but significantly lower than the value estimated for module *C*). On the other hand, from Fig. 10(b) it is possible to derive an estimation $R_{Sh,\mathrm{STC}}$ = 288 Ω (all the methods TR, DE and CMAES obtain very similar results). Similarly than for the previous PV modules, it is not possible to appreciate a dependency of R_{Sh} on the device temperature T. Finally, the diode ideality factor of module *D* (see Fig. 10(c)) can be estimated as m = 2.301 in STC with a negative derivative μ with respect T equal to −0.012 1/°C (always using TR as identification method that is the only one with R^2 near 1).



(a) estimation of $I_{SC,STC}$ and α for the module C



(b) estimation of $V_{OC,STC}$ and β for the module C



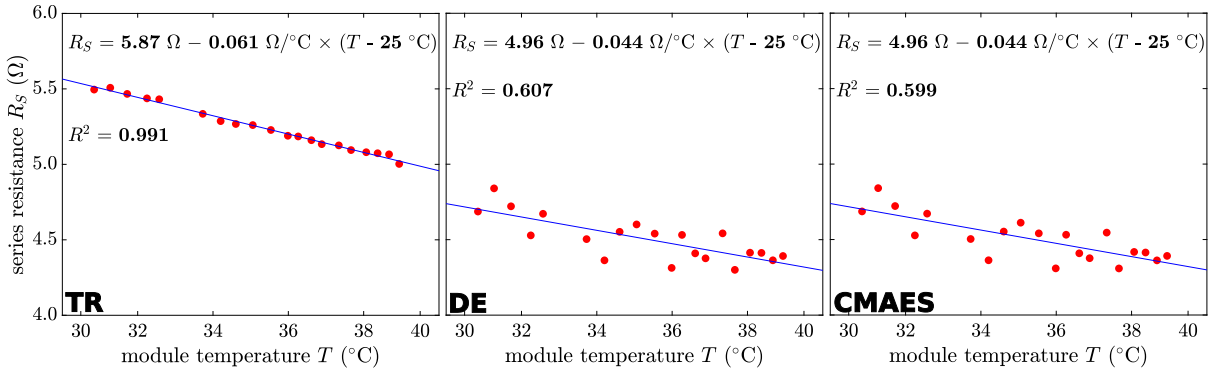
(c) estimation of $P_{max,STC}$ and γ for the module C

Fig. 7. Main electrical parameters and temperature coefficients of module C.

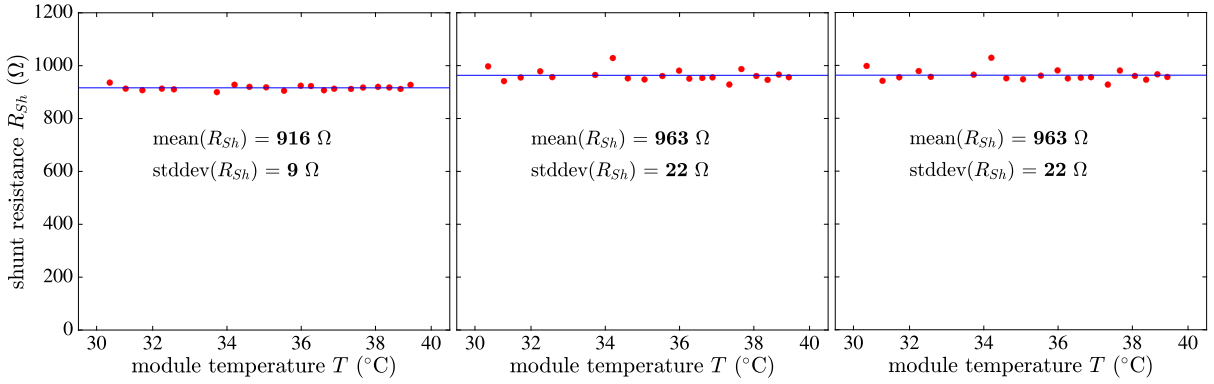
3.4. Module E (CdS/CdTe)

The main electrical parameters and temperature coefficients obtained for module E are presented in Fig. 11. For $I_{SC,STC}$ a value of 1.324 A was obtained that is a bit higher than the nominal value (1.23 A). The estimated α is +0.0007 A/°C (versus a nominal value +0.0005 A/°C). This means a relative α = +0.053 %/°C, that is between +0.034 %/°C and +0.071 %/°C, both estimations given by Dash and Gupta [13] for two different specimens. However, other authors provided lower α values, such as King et al. [8] (+0.019 %/°C), or much higher values, for example Mitterhofer et al. [75] (+0.11 %/°C). Regarding $V_{OC,STC}$ and β (see Fig. 11(b)), we achieved 86.84 V and −0.109 V/°C, in contrast to the values given by the manufacturer: 88.7 V and −0.222 V/°C. There is a high discrepancy in β and the relative value of this coefficient (−0.13 %/°C) is lower than the range given in previous literature (−0.44, −0.17) %/°C [8,13,75]. Finally, Fig. 11(c) shows us to a value γ = −0.09 W/°C, also very different to the nominal value −0.18 W/°C, although our estimation $P_{max,STC}$ = 66.9 W is only a bit higher than the nominal value 66.6 W.

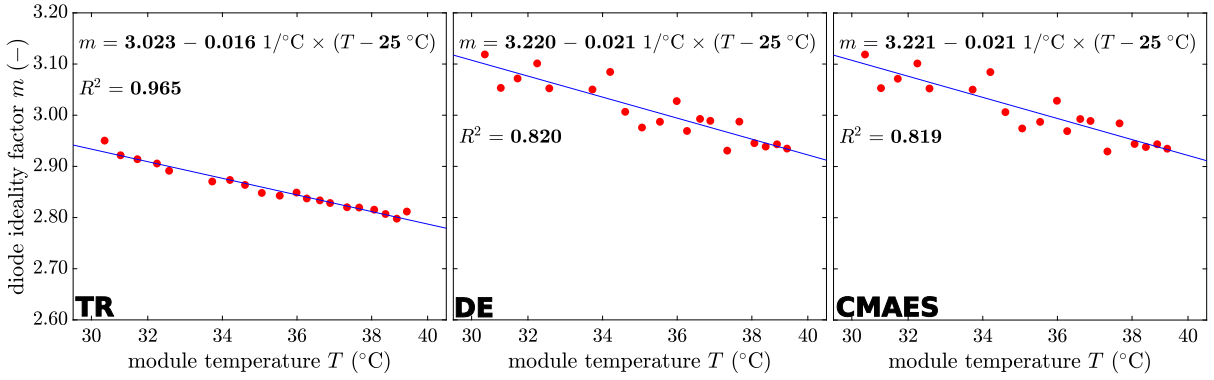
Fig. 12 shows the estimated parasitic resistances and ideality factor for module E. Again, the estimation provided by TR is taken into account due to its higher R^2. A value of 9.596 Ω was derived for $R_{S,STC}$. This value is the highest among all the modules under study. The corresponding value for temperature coefficient κ is −0.0686 Ω/°C. Comparing these two results with the values obtained for the module C, we can conclude that the series resistance of a CdS/CdTe module has



(a) estimation of $R_{S,\mathrm{STC}}$ and κ using trust-region, differential evolution and covariance matrix adaptation evolution strategies



(b) estimation of $R_{Sh,\mathrm{STC}}$ using trust-region, differential evolution and covariance matrix adaptation evolution strategies



(c) estimation of the ideality factor using trust-region, differential evolution and covariance matrix adaptation evolution strategies

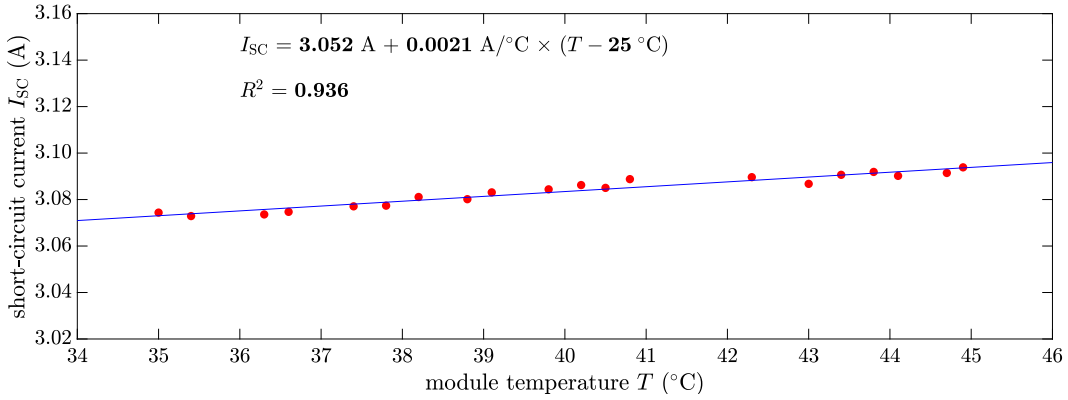
Fig. 8. Parasitic resistances and ideality factor of module *C* using different methods of parameter identification.

a thermal behavior similar to an amorphous module (very high R_S but decreasing with rising T). As for R_{Sh}, according to our experiments, the influence of T is not significant. We obtained a mean value of 1382 Ω (that is also the highest among all the modules). It can be seen that the identification methods DE and CMAES overestimate R_{Sh} with respect TR that reports a smaller standard deviation. The value obtained for the diode ideality factor m is also very high (3.24) with a very low positive slope with respect to T ($\mu = +0.006$ 1/°C).

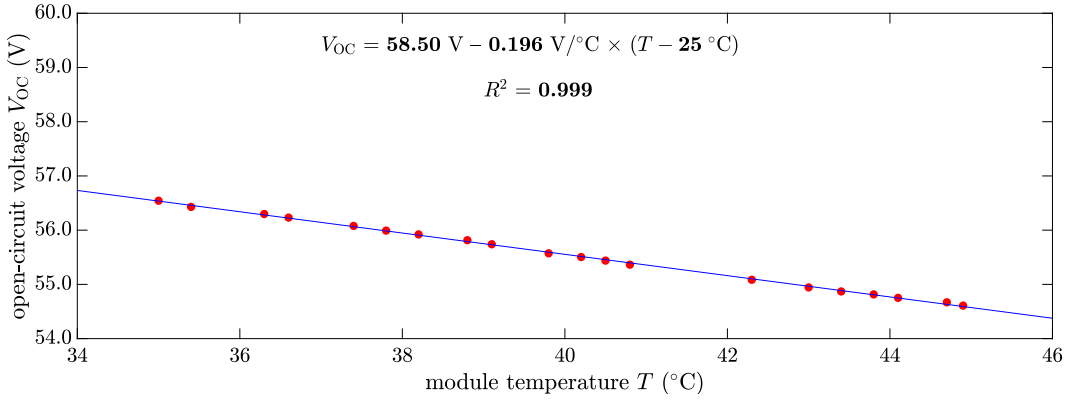
3.5. Module F (CIS)

Fig. 13 presents the results obtained for the main electrical parameters and temperature coefficients of module F which is a CIS module. We found that, I_{SC} is almost constant with respect T, in such a way we can assume $\alpha \approx 0.00$ A/°C obtaining a mean value $I_{\mathrm{SC,STC}} = 2.965$ A which is a bit lower than the nominal one 3.18 A. In fact, the manufacturer provided a very low α (+0.001 A/°C). This agrees with most of the previous authors [11,12,75,77], which report values under +0.02%/°C (possibly it is required a temperature spam higher than 10 °C to observe more variation of I_{SC}). The estimates obtained for$V_{\mathrm{OC,STC}}$ and β (see Fig. 13(b)) are 55.22 V and −0.142 V/°C, respectively (versus nominal values 59.7 V and −0.220 V/°C), resulting a great discrepancy between our estimation of β and the one provided by the manufacturer (as happens with module *D*). In addition (see Fig. 13(c)), our estimate of $P_{\mathrm{max,STC}} = 100.2$ W is significantly lower than its nominal value (120 W) with also a high discrepancy between the values of γ (−0.35 W/°C experimental versus −0.6 W/°C nominal). The relative value of γ is −0.35 %/°C, that is very close to the value provided by Virtuani et al. [11] (−0.36 %/°C) or by Mitterhofer et al. [75] (−0.33 %/°C) for other modules of the same technology.

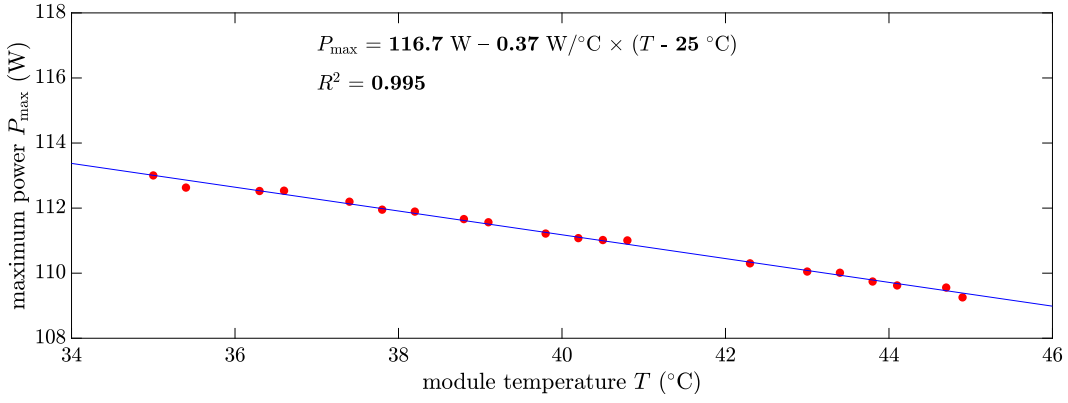
The parasitic resistances and ideality factor obtained for module F are shown in Fig. 14. Analyzing Fig. 14(a), it is not possible to see a relationship between the device temperature T and the series resistance R_S, so we only provide the mean value $R_{S,\mathrm{STC}} = 2.22$ Ω



(a) estimation of $I_{SC,STC}$ and α



(b) estimation of $V_{OC,STC}$ and β

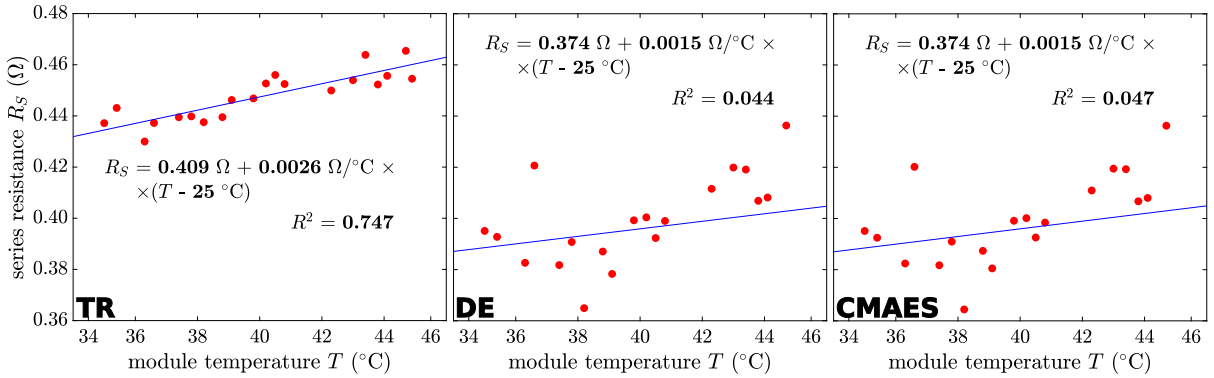


(c) estimation of $P_{max,STC}$ and γ

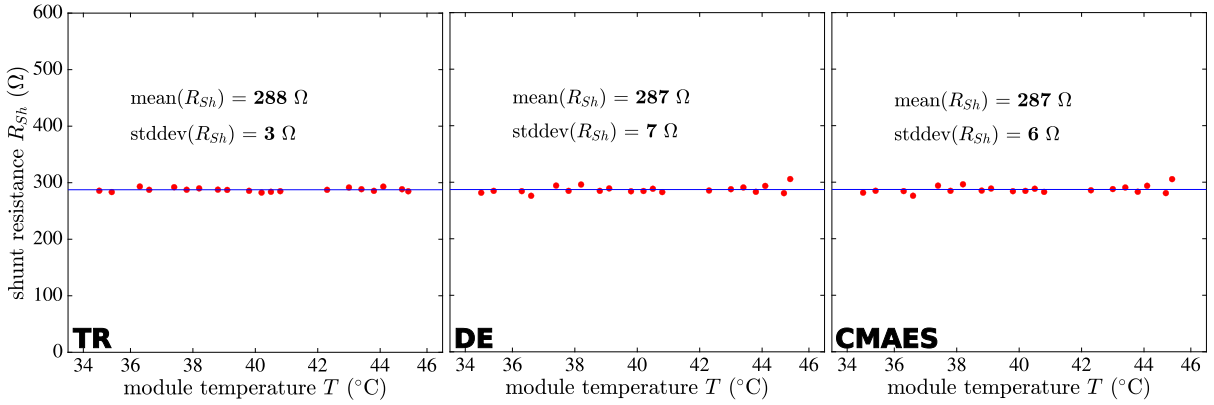
Fig. 9. Main electrical parameters and temperature coefficients of module *D*.

throughout the studied temperature range (the three parameter identification methods report very similar figures). The intrinsic parameters of a CIS module of the same manufacturer and similar specifications were identified by Ibrahim et al. [78] based on triple diode model and different evolutionary algorithms, and the mean value of R_S among all the specimens was between 1.067 Ω and 1.951 Ω, depending on the identification method (the method proposed by those authors estimated R_S = 1.697 Ω). This previous work also provided values for R_{Sh}, but in that case the gaps between the different estimates were very large (from 345 Ω and 2 788 Ω, being 1 192 Ω the value obtained by the proposed approach [78]). Our experimental result for R_{Sh}, shown in Fig. 14(b), is $R_{Sh,STC}$ = 503 Ω. Regarding the variability of R_{Sh} with respect T, the conclusion is similar to the one obtained with the other modules in this paper: R_{Sh} of this CIS module is not influenced by the increment of T. Finally, from Fig. 14(c), the diode ideality factor m for this CIS module can be expressed through a linear equation with m_{STC} = 1.753 and a negative slope with respect to T of μ = −0.0049 1/°C. This variation of m is less significant than that observed in other thin-film modules (such as modules *C*, *D* or *E*).

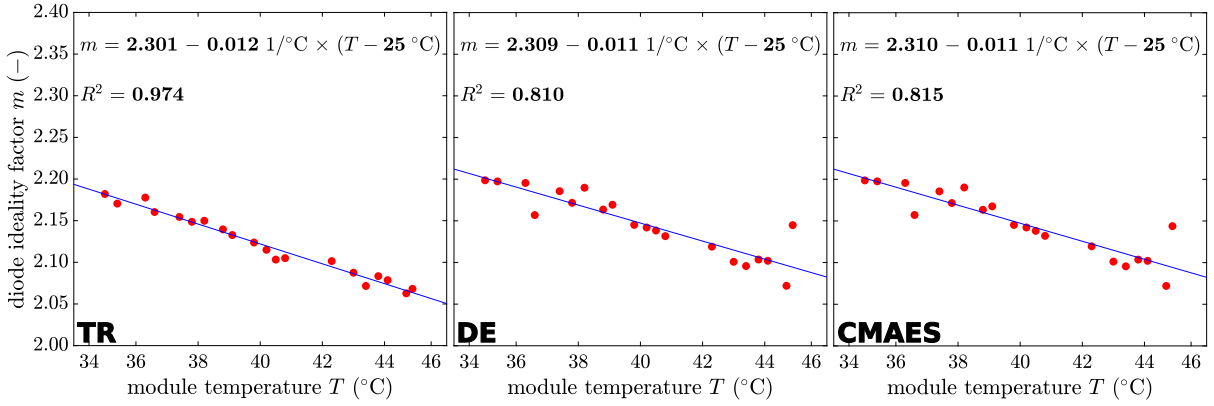
According to these results, for none of the technologies under study it is possible to derive a dependence of the shunt resistance R_{Sh} with respect the temperature. However, there are few papers in the literature that contradict this conclusion [2,14,23,41,43,79]. A possible reason is that the authors of those studies consider a range of temperature (for example from +10 °C until +70 °C) that is significantly wider than the ones used in this paper. In fact, in all the cases discussed herein, the temperature range spans about 10 °C (for example from +34 °C until +44 °C in the case of *Module A*). In such a narrow range, the



(a) estimation of $R_{S,\mathrm{STC}}$ and κ using trust-region, differential evolution and covariance matrix adaptation evolution strategies



(b) estimation of $R_{Sh,\mathrm{STC}}$ using trust-region, differential evolution and covariance matrix adaptation evolution strategies

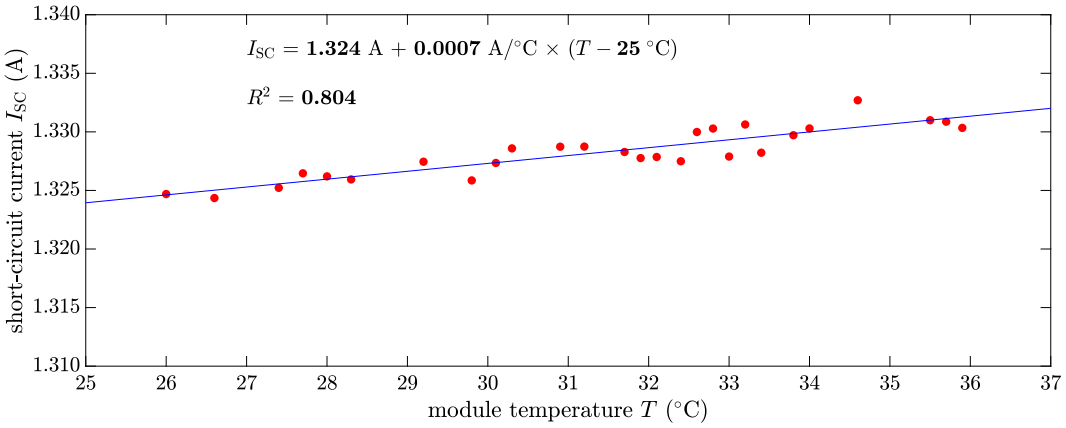


(c) estimation of the ideality factor using trust-region, differential evolution and covariance matrix adaptation evolution strategies

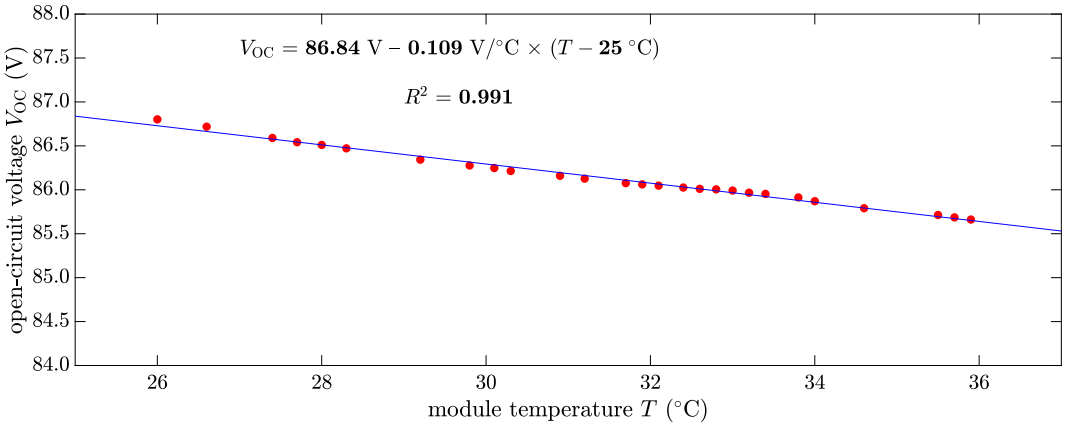
Fig. 10. Parasitic resistances and ideality factor of module *D* using different methods of parameter identification.

Table 5
Summary of the experimental values of the main parameters and temperature coefficients.

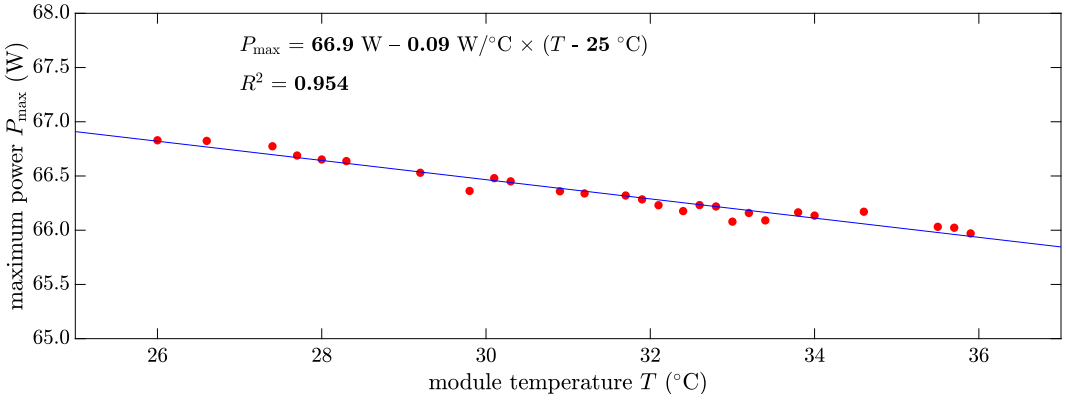
	A	*B*	*C*	*D*	*E*	*F*
Technology - a-	sc-Si	mc-Si	a-Si	a-Si/μc-Si	CdS/CdTe	CIS
$I_{\mathrm{SC,STC}}$ [A]	8.546	8.546	1.238	3.052	1.324	2.965
$V_{\mathrm{OC,STC}}$ [V]	22.03	21.84	94.3	58.50	86.84	55.22
$P_{\mathrm{max,STC}}$ [W]	142.0	137.4	72.6	116.7	66.9	100.2
$R_{S,\mathrm{STC}}$ [Ω]	0.1476	0.1693	5.87	0.409	9.60	2.22
$R_{Sh,\mathrm{STC}}$ [Ω]	459	178	916	288	1382	503
m_{STC} [−]	1.199	1.256	3.023	2.301	3.24	1.753
α [A/°C]	+0.0032	+0.0050	+0.0008	+0.0021	+0.0007	≈ 0.00
β [V/°C]	−0.074	−0.063	−0.31	−0.196	−0.109	−0.142
γ [W/°C]	−0.65	−0.52	−0.15	−0.37	−0.09	−0.35
κ [Ω/°C]	+0.00047	+0.00046	−0.061	+0.0026	−0.069	≈ 0.00
μ [1/°C]	≈ 0.00	≈ 0.00	−0.016	−0.012	+0.006	−0.0049



(a) estimation of $I_{SC,STC}$ and α



(b) estimation of $V_{OC,STC}$ and β



(c) estimation of $P_{max,STC}$ and γ

Fig. 11. Main electrical parameters and temperature coefficients of module *E*.

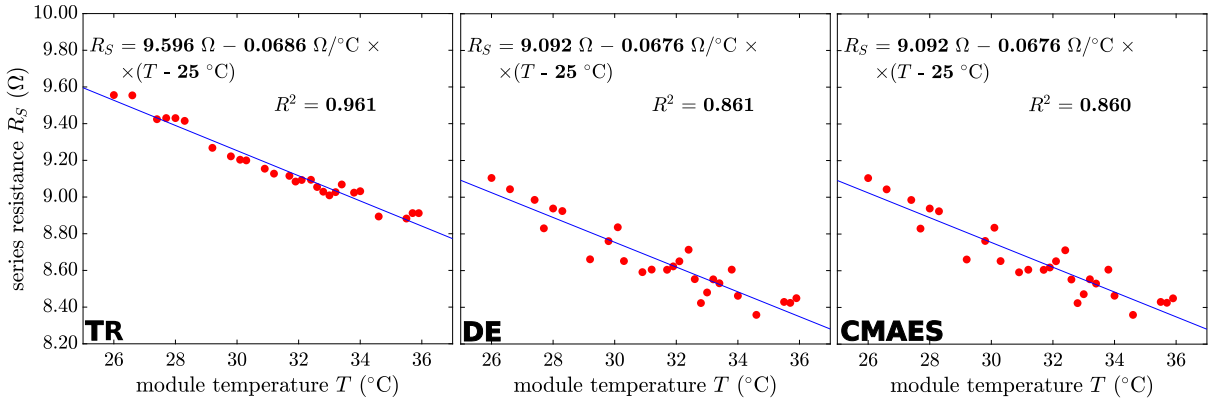
dependence on the temperature is confused with the dispersion due to noise. This is even more true if the temperature dependency is weak.

It is worth to note that the coefficient of determination R^2 obtained for some regression plots assumes a low value. This is critical when studying the dependence on the temperature of the ideality factor m or the series resistance R_S, because some values of R^2 are around 0.7 or even lower. This is due to the high sensitivity to the noise of the measured *I–V* curve [61] of the methods used for identification of the parameters.

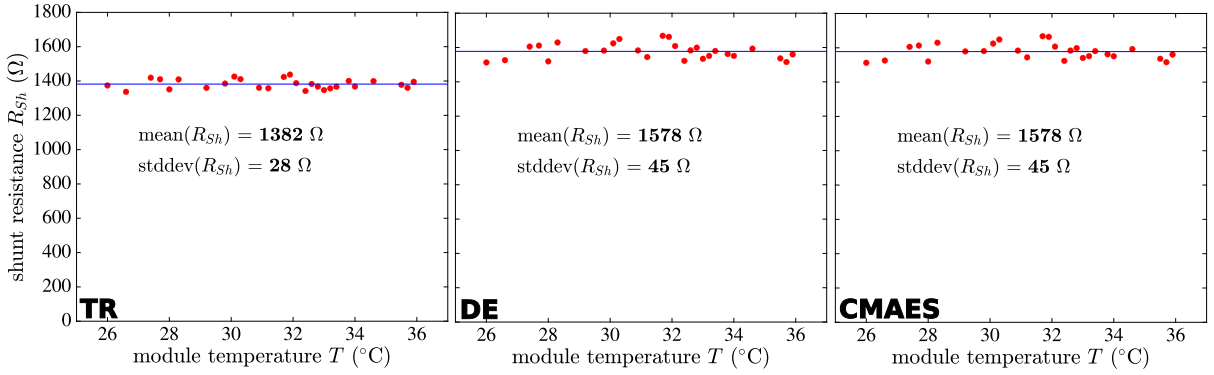
4. Conclusions

The first general conclusion is that for the crystalline silicon modules the values estimated from our experiments are closer to the nominal ones than in the case of the thin-film modules. The estimated values in this article can change over time, especially in thin-film technologies, due to degradation of the specimens or spectral variations of the sunlight throughout the year [80].

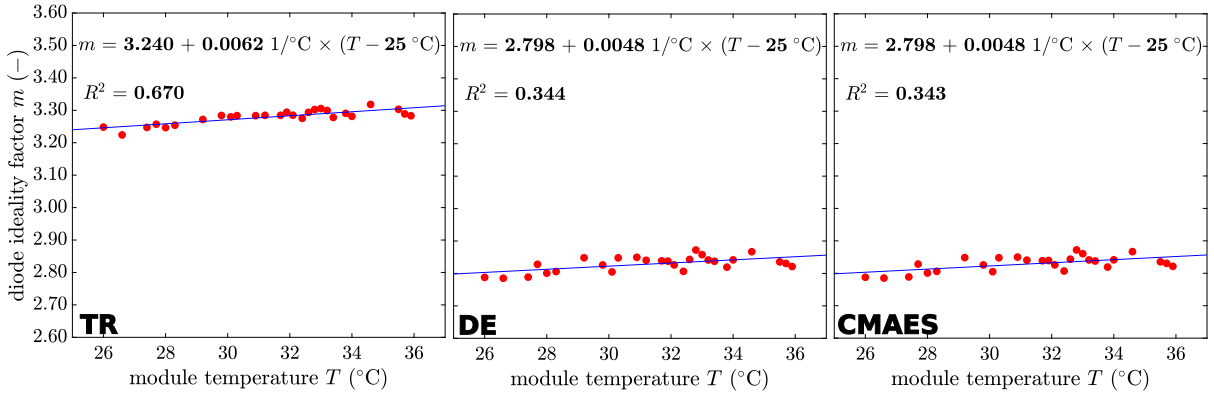
For all the specimens, the temperature coefficients α, β, and γ obtain estimations as expected and according to previous literature, being



(a) estimation of $R_{S,\mathrm{STC}}$ and κ using trust-region, differential evolution and covariance matrix adaptation evolution strategies



(b) estimation of $R_{Sh,\mathrm{STC}}$ using trust-region, differential evolution and covariance matrix adaptation evolution strategies



(c) estimation of the ideality factor using trust-region, differential evolution and covariance matrix adaptation evolution strategies

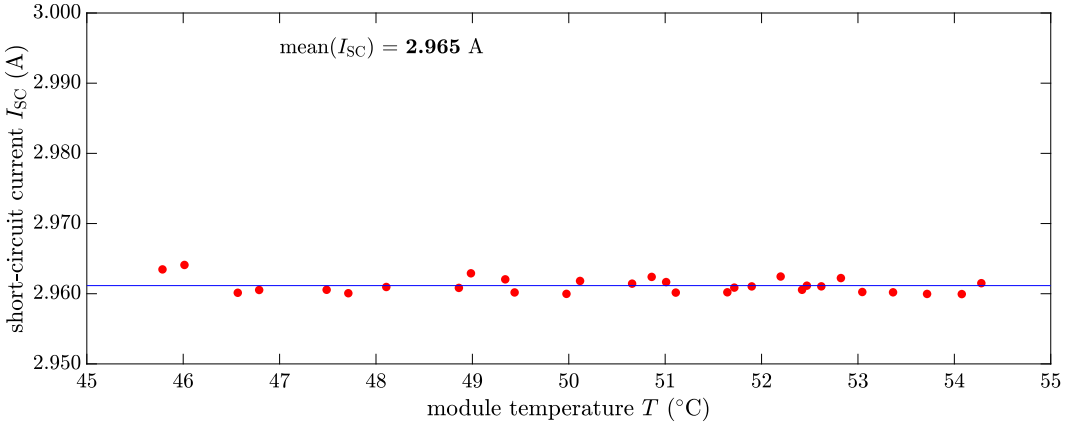
Fig. 12. Parasitic resistances and ideality factor of module E using different methods of parameter identification.

the thin-film technologies less sensitive to temperature changes. The obtained results using the different parameter identification methods imply that the TR approach is the most suitable for the SDM model. In addition, the series resistance R_S values of the thin-film modules have also higher values than the crystalline silicon ones, especially the modules a-Si and CdS/CdTe. Regarding its temperature coefficient κ we have observed a significant influence of the temperature on R_S for all the technologies except for the CIS module. In case of a-Si and CdS/CdTe, a value of $\kappa < 0$ is obtained, which means a higher fill factor for rising temperatures. Contrary, we found that for all the other technologies $\kappa > 0$, meaning a negative effect of the temperature over the fill factor and P_{max}.

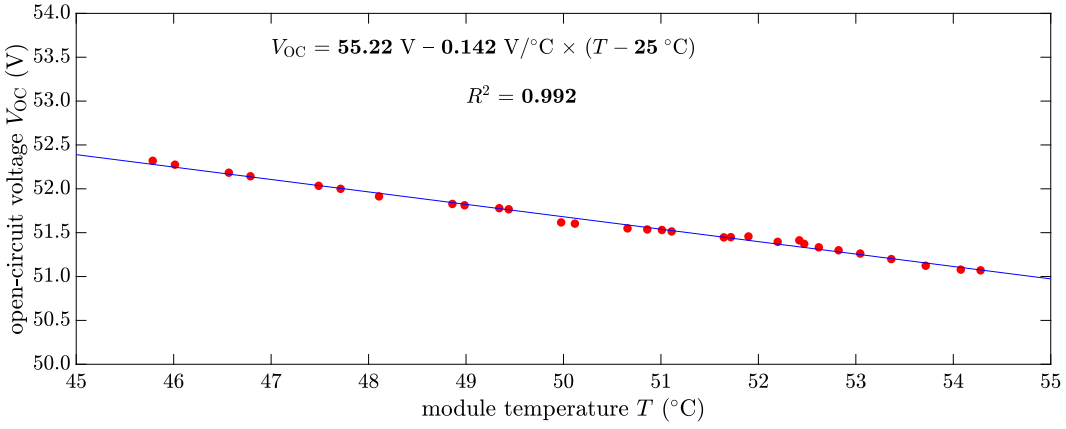
From our experience during these experiments (and from a previous paper [61]), we can state that the most difficult parameter to identify is the shunt resistance R_{Sh} because it is very sensitive to the measurement noise and the identification method.

Finally, in the crystalline silicon cases, the value of m can be assumed as constant, in theory between 1 and 2, but for high-top manufacturers, values lower than 1.3 are very common. However, that is not true for the thin-film modules. On the one hand, the value of m under STC could be greater than 2 or more (with the exception of the CIS technology). On the other hand, higher temperature means lower value of m (except with CdS/CdTe), and that should have a positive effect on the fill factor and P_{max}.

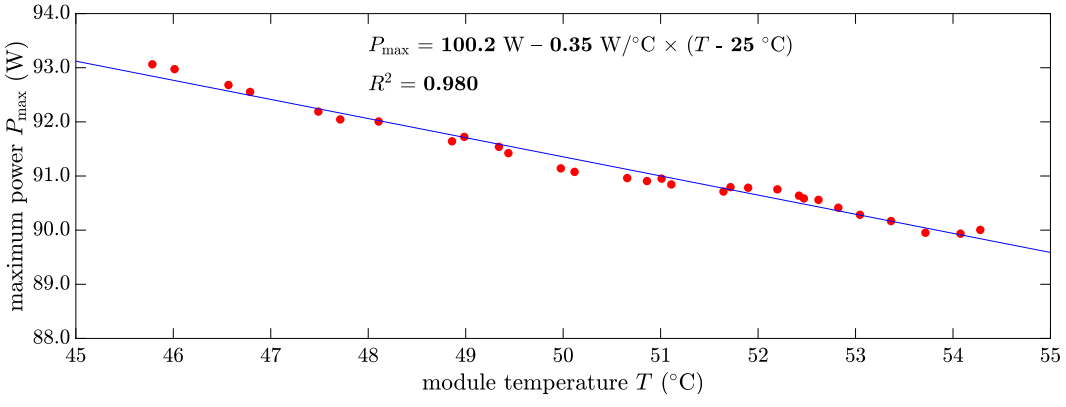
It is worth to note that the experimental results presented in this article have been obtained under outdoor conditions. As the temperature of the PV modules cannot be controlled, the available temperature range and the size of the data set are limited in order to ensure the validity of the obtained results. In a further work, the results of a similar experiment under indoor conditions will be presented; they will be obtained by using a temperature control system allowing to range the



(a) estimation of $I_{SC,STC}$ (assuming $\alpha \approx 0.0$ A/°C)

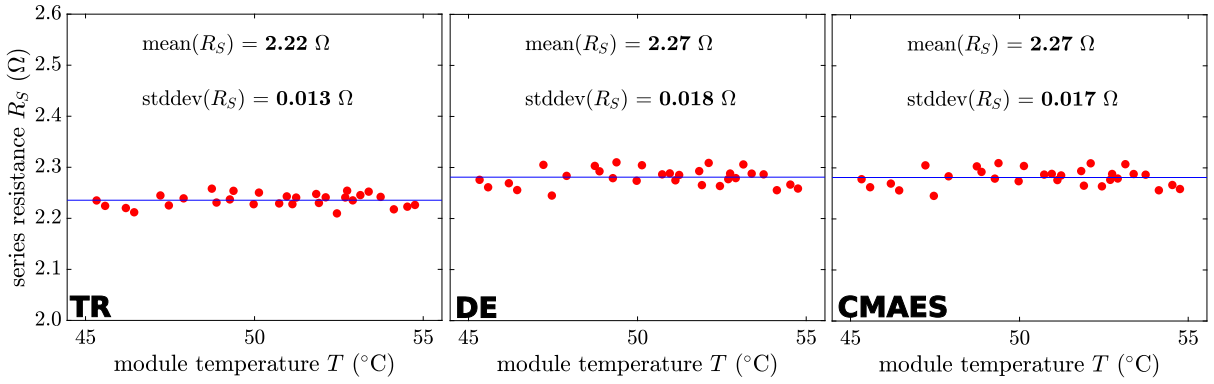


(b) estimation of $V_{OC,STC}$ and β

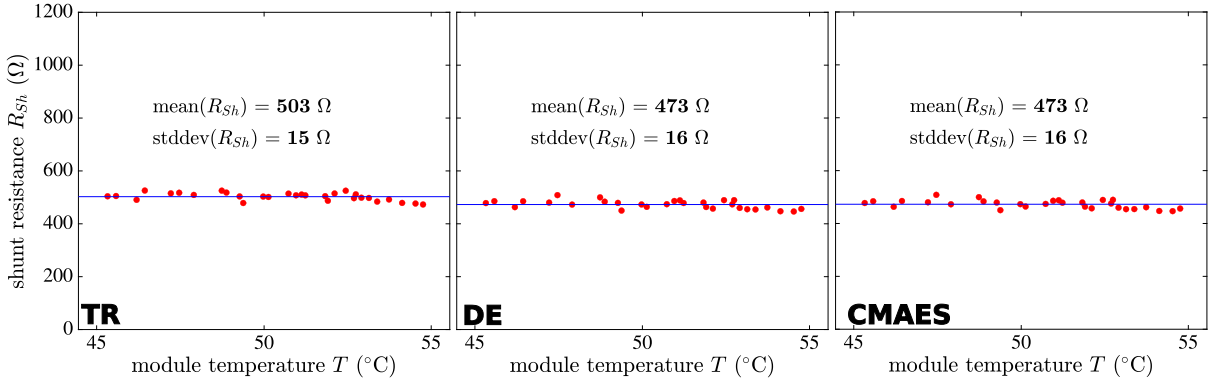


(c) estimation of $P_{max,STC}$ and γ

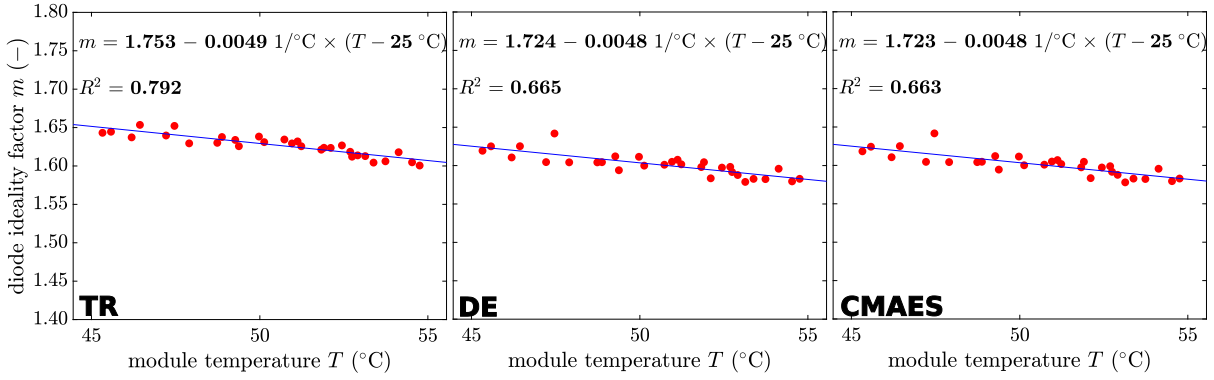
Fig. 13. Main electrical parameters and temperature coefficients of module F.



(a) estimation of $R_{S,\mathrm{STC}}$ and κ using trust-region, differential evolution and covariance matrix adaptation evolution strategies



(b) estimation of $R_{Sh,\mathrm{STC}}$ using trust-region, differential evolution and covariance matrix adaptation evolution strategies



(c) estimation of the ideality factor using trust-region, differential evolution and covariance matrix adaptation evolution strategies

Fig. 14. Parasitic resistances and ideality factor of module F using different methods of parameter identification.

temperature from +10 °C until +70 °C and by acquiring hundreds of I–V curves between these two values. Then, the present results obtained outdoors will be compared with the new indoor measurements in a future paper.

CRediT authorship contribution statement

Michel Piliougine: Writing – review & editing, Writing – original draft, Visualization, Validation, Software, Methodology, Investigation, Data curation, Conceptualization. **Luis Enrique Garcia-Marrero:** Software, Validation, Visualization, Writing – review & editing. **Kari Lappalainen:** Writing – review & editing, Writing – original draft, Methodology, Investigation. **Giovanni Spagnuolo:** Writing – review & editing, Writing – original draft, Supervision, Project administration, Methodology, Investigation, Funding acquisition.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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digital twin for mismatched photovoltaic arrays control and diagnosis" (funded by the European Union – Next Generation EU, Mission 4 Component 1, CUP D53D23016000001), the Marie Skłodowska–Curie grant agreement No 955614 (funded by European Union – Horizon 2020 Research and Innovation Program), and the Research Council of Finland (funding decision 348701).

Data availability

The raw data supporting the conclusions of this article will be made available by the authors on request.

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