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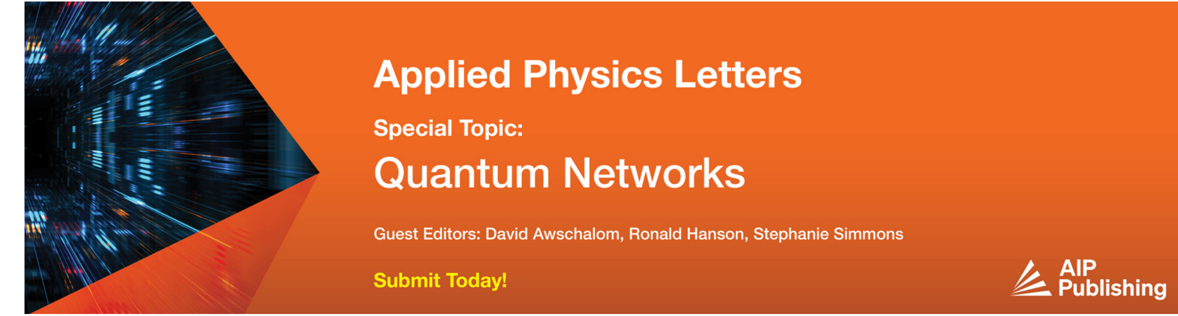

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ABSTRACT

We report on the realization of Nb-based *all-metallic* Dayem nano-bridge gate-controlled transistors (Nb-GCTs). These Josephson devices operate up to a temperature of ∼3 K and exhibit full suppression of the supercurrent thanks to the application of a control gate voltage. The dependence of the kinetic inductance and of the transconductance on gate voltage promises a performance already on par with so far realized metallic Josephson transistors and leads us to foresee the implementation of a superconducting digital logic based on the Nb-GCT. We conclude by showing the practical realization of a scheme implementing an all-metallic gate-tunable *half-wave* rectifier to be used for either superconducting electronics or photon detection applications.

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Superconductor electronics (SCE) deals with electronic circuits based on elements that are superconducting below their critical temperature (T_c) and exhibits unique characteristics and performances, which are unrivaled by conventional semiconductor counterparts.[1,2] SCE relies on the quantum properties of superconductors such as Josephson effects,[3,4] magnetic flux quantization,[5,6] and extremely low-power absorption in both DC and AC fields up to the superconducting gap frequency ($f_\Delta = 2\Delta/h$, where Δ and h are the superconducting gap and Planck's constant, respectively). For practical SCE, the superconducting material of choice is niobium (Nb): a Bardeen–Cooper–Schrieffer (BCS) metal that has the highest T_c (∼9.2 K) and f_Δ (∼770 GHz) among elemental superconductors,[1] which is therefore suitable for circuit operation at temperatures around ∼4 K. Other elemental superconducting metals with sizable T_c, such as vanadium (V) or lead (Pb), are scarcely exploited[7–9] for SCE. Furthermore, despite the fact that other low-temperature superconductors with lower T_c are widely exploited in radiation detection and for quantum computation architectures, compound superconductors with T_c higher than that of Nb such as NbN, carbonitrides and cuprate high-T_c superconductors have limited SCE applications, mostly due to complex and expensive film deposition techniques, to the extremely short coherence length and to the anisotropy of their electronic properties.[1]

In this Letter, we report on the realization of Nb-based *all-metallic* Dayem nano-bridge (DB) gate-controlled transistors (Nb-GCTs). Different from supercurrent[10–14] and Josephson field-effects (SuFETs and JoFETs),[15,16] where the critical current of a proximitized semiconductor is controlled via conventional field-effect-driven charge depletion/accumulation, *all-metallic* superconducting transistors (S-GCTs) represent a recently demonstrated class of devices entirely fabricated with BCS metals. In these transistors, the supercurrent flow can be significantly manipulated via electro-static gating[17–21] without any variation of the charge density. The most relevant phenomenology observed in S-GCTs is the bipolar reduction, down to full-suppression, of the critical supercurrent (I_C) for both positive and negative gate polarizations. Furthermore, the dependence of the phase on an externally applied electrostatic field was recently demonstrated in gated Ti-based superconducting quantum interference devices (SQUIDs)[21] and in the evolution of the switching current probability distributions in Ti DBs.[22]

The microscopic origin of these effects is, at this time, not clear yet, and only a few theoretical models have attempted to explain the above experiments.[23] The involvement of voltage-driven polarization of the surface orbital of the superconductor has been proposed.[24,25] Furthermore, a quasi-particle injection due to a field-emitted current between the gate and the superconductor has been claimed to have a major role in the critical supercurrent suppression.[26,27] Nonetheless, regardless of the definitive interpretation of the aforementioned phenomena, the implementation of digital logic gates based on

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superconducting S-GCTs has already been proposed such as AND, COPY, and NOT circuits.[19] All these ports are based on the so-called EF-Tron, i.e., the electrostatically gated counterpart of the nano-cryotron (nTron).[6,28,29] The latter is a device where an injection current is used to control the supercurrent flowing in a metallic channel. S-GCTs based on Al,[25] Ti,[17] and V[19] have already been demonstrated, but no implementation with Nb was reported so far. The results presented here fill this gap and make Nb-GCTs the enabling technology to implement a SCE platform, which is naturally compatible with both the rapid single flux quantum (RSFQ)[5,6] and the complementary metal-oxide-semiconductor (CMOS) approaches. At the same time, Nb-GCTs could be used to implement a complete and independent computation platform (see, e.g., Ref. 19), providing a viable fully superconducting alternative to already established technologies. Finally, it is worthwhile to emphasize that, although there exist compound metals with higher critical temperature (for instance, NbN), most of the present-time superconducting electronics is based on Nb. This make our devices compatible with established industrial protocols and fabrication lines. We believe the latter points to be crucial in order to imagine real-world applications of our devices.

Our Nb-GCTs were fabricated by single-step electron-beam lithography (EBL) to pattern a polymethyl-methacrylate (PMMA)/Al (thickness: 250 nm/11 nm) bi-layer mask on a sapphire substrate. A 10-nm-thick Ti adhesion layer was then dc-sputtered, followed by 40 nm of Nb and a final metal lift-off procedure in acetone bath. Since Nb is a refractory material, its evaporative deposition is usually not performed to avoid high crucible temperatures and the following outgassing of the organic mask, which results in a reduction of the film quality.[30–34] Usual nano-patterning of Nb films relies on sputter deposition followed by EBL and etching, but, to avoid residues originating from the reaction between the etching gases and the PMMA, we opted for an EBL procedure followed by sputter deposition and lift-off.

Figures 1(b) and 1(c) show false-color scanning electron micrographs taken with different magnifications of a representative Nb-GCT. The Nb DBs [colored in blue in Figs. 1(b) and 1(c)] are about ~90 nm wide and 100 nm long and have a normal-state resistance $R_{DB} \sim 30\ \Omega$. The gate [shown in green in Figs. 1(b) and 1(c)] is separated from the weak link by an ~70-nm-wide gap. The results presented in the following were obtained on the same device, measured in a filtered cryogen-free dilution refrigerator at temperatures down to 30 mK. The biasing scheme of the Nb-GCT is depicted in Fig. 1(b).

From the measurement of the resistance (R) vs temperature T [see Fig. 1(a)], we extracted the critical temperature of the Nb film, $T_{Nb} \simeq 7.9$ K, corresponding to a zero-temperature BCS energy gap $\Delta_0 = 1.764 k_B T_{Nb} \simeq 1.2$ meV, where k_B is the Boltzmann constant. T_{Nb} is ~15% lower than Nb bulk critical temperature likely due to the inverse proximity effect from the Ti sticking layer. Due to its lateral size, the critical temperature of the DB (T_{DB}) turns out to be approximately one half of that of the pristine film. Below T_{DB}, dissipationless charge transport occurs: the current–voltage (I–V) characteristics, recorded at temperatures ranging between 30 mK and 6.9 K, are shown in Fig. 1(d). A switching critical current $I_S \sim 30\ \mu$A was observed at 30 mK, displaying the usual hysteretic behavior that stems from heating dissipated within the wire while switching from the resistive to the superconducting state.[35,36] The decay of I_S vs T is shown in Fig. 1(e) along with a fit of the Bardeen equation (black dotted line),

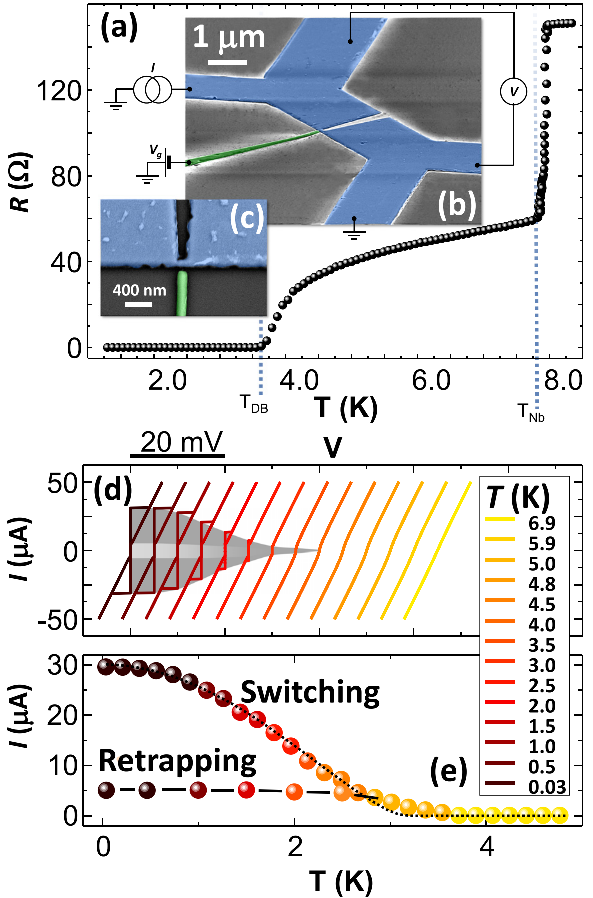

FIG. 1. (a) Resistance R vs temperature T characteristics of a representative Nb-GCT device. The measurement was performed via a standard four-wire lock-in technique in a filtered dilution refrigerator. Two transitions were observed, highlighted by black dashed lines corresponding to the superconductor-to-normal state transition of the Nb-leads (T_{Nb}) and of the DB (T_{DB}). (b) False color scanning electron micrograph (SEM) of a Nb-GCT. The blue area corresponds to the Nb leads and the DB. The Nb gate is colored in green. The biasing scheme used for four-wire dc characterization of our devices is also shown. (c) False color SEM blow-up of the DB region. (d) Current I vs voltage V characteristics at several bath temperatures T of a representative Nb-GCT. Curves are horizontally offset for clarity. (e) Switching (I_S) and retrapping (I_R) currents vs T of the same device of (d). The black dotted line shows the best-fit of the decay of I_S as a function of T with the Bardeen formula. A guide for the eye is also drawn to highlight the decay of I_R with temperature.

$I_S(T) = I_{0c}[1 - (\frac{T}{T_{DB}})^2]^{3/2}$, where $I_{0c} = (30.0 \pm 0.1)\ \mu$A and $T_{DB} = (3.16 \pm 0.01)$ K are the zero-temperature DB critical current and temperature derived from the fitting procedure,[37] respectively. The behavior of the retrapping current (I_R) is also shown. Above the threshold temperature, $T_h \sim 2.5$ K, the hysteretic behavior disappears, and I_R coincides with I_S.

The investigation of the gating effect in Nb-GCTs was performed by measuring I_S vs gate voltage V_G (see Fig. 1).[17–22,25,38] Figure 2(a) displays the DB transistor I–V characteristics measured at 30 mK for the selected values of $|V_G|$ increasing up to 40 V. The critical current I_S displays a plateau at low V_G values and then monotonically decays by

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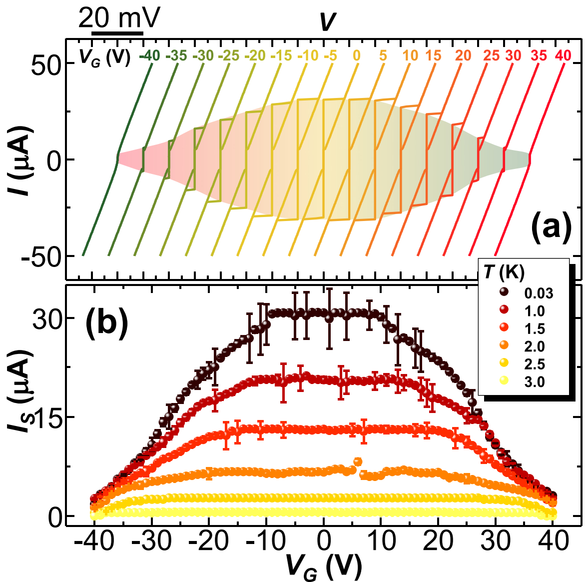

FIG. 2. (a) Current I vs voltage V characteristics at several gate voltages V_G for the same Nb-GCT of Fig. 1. Curves are horizontally offset for clarity. A clear bi-polar suppression of the switching current is visible as $|V_G|$ is increased. (b) I_S vs V_G for different temperatures T ranging between 30 mK and 3 K. I_S values were collected by measuring 50 repetitions of the $I(V)$ characteristics. Error bars represent the standard deviation of the samples.

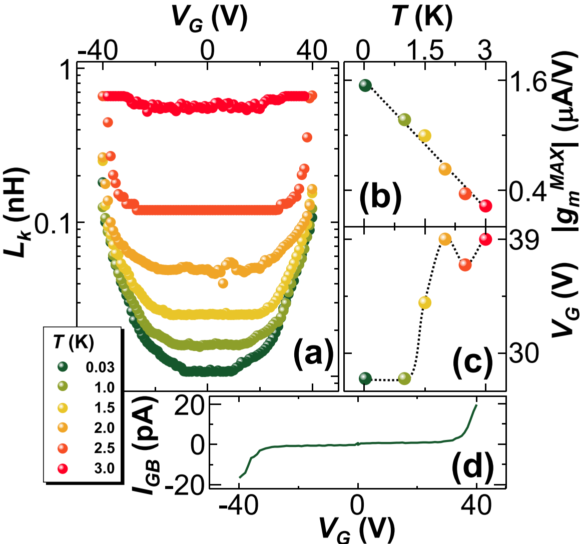

FIG. 3. (a) Kinetic inductance L_k vs gate voltage V_G for a Nb-GCT at several temperatures T. Data were deduced from the expression $L_k = \hbar/2eI_S$. (b) Maximum of the absolute value (g_m^{MAX}) of the transconductance $g_m = dI_s/dV_G$ vs T. Data were determined from the numerical derivative of the data shown in Fig. 2(b). (c) Value of gate V_G at which the maximum of transconductance $|g_m^{MAX}|$ occurs as a function of T. (d) Gate-DB current I_{GB} vs V_G at 30 mK.

increasing $|V_G|$ reaching, at 30 mK, a suppression of about 90% with respect to the unperturbed value. Yet, as already reported on similar setups,[17–22,25,38] the electric field does not affect the transistor normal-state resistance R_{DB}. The full temperature dependence of the gating effect is shown in Fig. 2(b), which displays the I_S vs V_G characteristics for selected bath temperatures up to 3 K. By increasing T, the I_S plateau widens, but its suppression is still visible up to 3 K. Notably, when $T \gtrsim 2$ K, full suppression of I_S was observed for $V_G > 40$ V. Moreover, I_R is not affected by V_G until it coincides with I_S due to the action of either gate voltage or temperature.[17–22,25,38] The latter consideration is relevant in view of a possible implementation of Nb-based EF-Trons operating at 3 K, where the absence of the hysteretic behavior might allow for fast gate-driven switching between the normal and the superconducting state.

We now turn to discuss some figures of merit, which are relevant for possible applications of the Nb-GCTs. The kinetic inductance $L_k = \hbar/2eI_S$ (where $\hbar$ is the Planck constant and e the unitary charge) is the quantity usually analyzed in Josephson junctions and plays a fundamental role in applications requiring non-galvanic readout of the junction state. Figure 3(a) shows the L_k vs V_G characteristics, determined from the I_S measurements, at several different temperatures. The maximum value of zero-gate kinetic inductance is $L_k \sim 0.7$ nH obtained at 3 K, while for a fixed temperature, gate-dependent modulations of L_k range from $\sim$1 nH at 30 mK up to $\sim$200 pH at 3 K. Such a behavior originates from the lower gate-dependent variation of I_S at higher temperatures and reflects also in the evolution in temperature of the gate-channel transconductance, which is defined for a S-GCT as $g_m = dI_S/dV_G$. This quantity is a figure of merit, relevant mainly for technological applications, which quantifies how large is the current modulation as a function of the gate voltage. In fact, devices with a larger transconductance have a better sensitivity to the gate and, therefore, operate at lower gate voltages. To highlight the temperature dependence of the transconductance, the absolute value of its maximum ($|g_m^{MAX}|$) is plotted as a function of the temperature in Fig. 3(b). $|g_m^{MAX}|$ linearly decreases as a function of T. By contrast, stemming from the widening of the I_S vs V_G plateau, the gate voltage at which the maximum occurs V_G^{MAX} increases vs T [see Fig. 3(c)]. The maximum value of $|g_m^{MAX}| \simeq 1.6$ μA/V was obtained at 30 mK. Remarkably, at 3 K, i.e., just below T_{DB}, $|g_m^{MAX}|$ is still equal to 0.3 μA/V. To provide the reader with a term of comparison, we remind that such values are a few orders of magnitude larger than those achievable in semiconductor nano-wire Josephson transistors,[16] which in turn operate below $\sim$100 mK.

As the last figure of merit, we discuss the gate-DB current I_{GB} as a function of gate voltage V_G. It provides information on the quality of insulation between the gate and the weak link and allows us to exclude direct injection of hot electrons into the superconducting DB. Current injection, indeed, could result detrimental for the performance of the device, leading to a substantial reduction of input–output isolation of the FET. $I_{GB}(V_G)$ was acquired at 30 mK with a two-wire technique, by using a low-noise voltage source and a 10^{-11} A/V-gain current preamplifier [see Fig. 3(d)]. I_{GB} is an odd function of V_G exhibiting a clear threshold ($\sim$35 V) behavior, reaching a maximum value of $\sim$20 pA at $V_G = 40$ V, which corresponds to $\sim 10^{-7} I_S(V_G = 0)$. Furthermore, the gate-channel transimpedance at $V_G = 27$ V, i.e., where $I_S(V_G) \sim 0.5 I_S(V_G = 0)$, is approximately $\sim$24 TΩ. As discussed also elsewhere (see, e.g., the supplementary material of Ref. 17 and the Appendix of Ref. 22), such a behavior is hardly compatible with a conventional hot-electron injection into the DB and, at the same time,

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confirms the good electrical insulation between the transistor channel and the gate. In addition, we measured the variation of $I_{GB}(V_G)$ on temperature and found basically no dependence up to 4 K. The above result suggests that at least some fraction of the measured current might originate from dispersion in the lines of our measurement setup since electron injection either through vacuum or the substrate is expected to be strongly enhanced as the bath temperature is increased by two orders of magnitude.

In this last section, we show the practical realization of a scheme based on a Nb-GCT, which realizes a possible building block to implement a superconducting diode. We begin our discussion by highlighting the sharp dependence of the DB resistance R on V_G. Figure 4(a) shows a color plot of the derivative of the four-wire transistor resistance $\frac{dR}{dV_G}$ as a function of bias current I and gate voltage V_G at 3 K. The green and red stripes correspond to the transition to the normal state as I_S was lowered below I_B due to the action of the gate voltage. The sharpness of the super-to-normal state transition is a typical feature of superconducting devices that are usually and widely exploited, for instance, in transition-edge sensors (TESs) to reveal a tiny incoming radiation heating the superconductor above its T_C. By contrast, in our devices, the transition events are triggered and controlled by an electrical gate signal. In Fig. 4(b), we schematize how to exploit gate-driven state-transitions to rectify an alternate voltage signal V_{AC} applied to the gate electrode. V_{AC} [green curve in Fig. 4(b)] is summed to the direct-current (dc) V_G signal, and I_S [red curve in Fig. 4(b)] is thereby modulated in time according to V_{AC} above and below $I_S(V_G)$. Therefore, depending on the constant current $I_B > 0$ [see the dashed black line in Figs. 4(a) and 4(b)], I_S oscillates above and below I_B, resulting in periodic normal-to-super and super-to-normal transitions. The resulting voltage signal $V(t)$ across the DB [see the blue curve in Fig. 4(b)] has the *same* period P of $V_{AC}(t)$ and a duty cycle τ/P given by the time for which $I_S < I_B$. $V(t)$ oscillates between a *low-state*, where $V(t) = 0$ (superconducting state), and a *high-state*, where $V(t) = R \cdot I_B > 0$. We note that, due to the dependence of the device resistance on the gate voltage,[18] the output DC voltage is expected to directly depend on the amplitude of the AC signal. Such a circuit, sketched in Fig. 4(c), realizes a *half-wave* rectifier, which could be exploited in a superconducting diode, for instance, to rectify the radiation picked up by an antenna coupled to the gate electrode. In the latter case, the sensitivity depends on the width of the switching current probability distribution of the DB (see Ref. 22), while the amplitude of $V(t)$ can be enhanced by increasing I_B. With respect to the cutoff frequency of the Nb-GCT-based rectifier, we note that the upper limiting frequency set by f_Δ might be reduced by the typical timescale of the electrically driven phase transition in S-GCTs, which is currently totally unknown and demands for a future investigation. Yet, the DB-gate capacitance is low enough (~0.1 fF) not to play any role.

To provide a preliminary demonstration of the rectifying behavior of the DB, we biased the gate of our Nb-GCTs according to the scheme of Fig. 4(c). V_{AC} was provided by the sinusoidal reference of a lock-in amplifier (the frequency and amplitude of V_{AC} were ~17 Hz and 10 mV, respectively), while I_B was kept equal to 2.5 μA. The voltage V was measured in-phase as a function of V_G. As shown in Fig. 4(d), V is almost 0 until $I_S(V_G) < I_B$. When $I_S(V_G)$ crosses I_B, at $V_G \sim 24$ V, sharp peaks appear, corresponding to the differential resistance peaks, and demonstrate the occurrence of a rectified in-phase voltage signal across the DB. The difference in the height of the peaks is due to the slight asymmetry of $I_S(V_G)$. By further increasing V_G, V drops to lower values since $I_S(V_G)$ is constantly lower than I_B. In this V_G configuration, nonetheless, V is never equal to zero due to the gate-dependent DB resistance.[18]

In summary, we have demonstrated Nb-based *all-metallic* Josephson gate-controlled transistors operating up to ~3 K, which

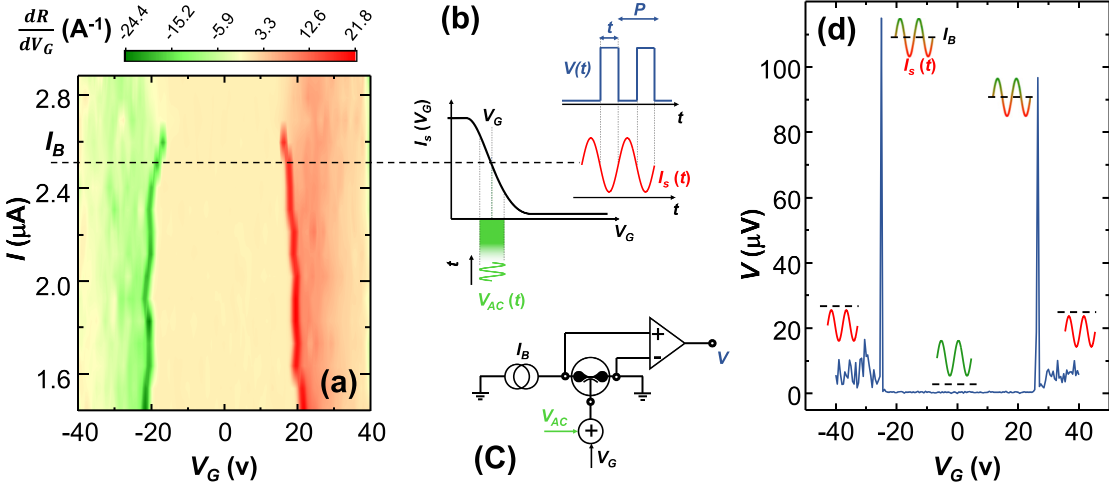

FIG. 4. (a) Color plot of the differential resistance dR/dV_G vs V_G and I of a Nb-GCT measured at 3 K. Green and red stripes correspond to the gate-driven superconducting-to-normal transitions of the DB. (b) Scheme of the operation principle of the Nb-GCT half-wave rectifier. The device is operated at constant current bias I_B [black dashed line in panels (a) and (b)], whereas the gate electrode is biased with a signal composed of an ac component V_{AC} (green line) and a dc component V_G. This results in a time-dependent switching current $I_S(t)$ (red line), which, depending on the amplitude of V_{AC} and on the set point of V_G, yields periodic normal-to-super and super-to-normal state transitions. In the latter condition, the voltage drop V at the ends of the DB oscillates between a low and a high state (blue line) with periodicity P equal to that of V_{AC} and duty cycle τ/P. (c) Biasing scheme used to implement a *half-wave* rectifier based on a Nb-GCT. (d) Voltage drop V across the DB measured in a four-wire configuration with a lock-in amplifier vs V_G. V_{AC} is the reference signal of the lock-in amplifier. I_B was set to 2.5 μA. As shown in (d), V is almost zero until $I_S(V_G) < I_B$. The peaks correspond to the rectification of the ac gate signal.

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could be pivotal for the implementation of superconducting digital logic ports. Our nano-bridge showed full quench of the Josephson current due to the application of a gate-voltage V_G. The dependence of the kinetic inductance and of the transconductance on V_G suggests that these nano-devices are competitive with respect to conventional semiconductor nano-wire-based Josephson transistors. We have finally also demonstrated the operation of a superconducting half-wave rectifier to be exploited either in SCE or for photon detection applications.[39]

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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